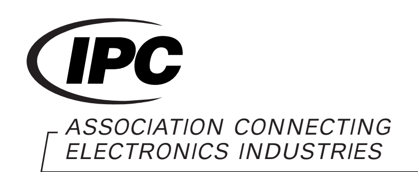


IPC-SM-782A

Includes: Amendment 1 and 2

Surface Mount Design and Land Pattern Standard

IPC-SM-782A

August 1993

A standard developed by IPC

Amendment 1
October 1996

Amendment 2
April 1999

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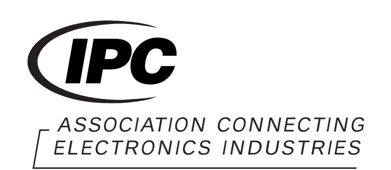
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IPC-SM-782A

Surface Mount Design and Land Pattern Standard

Developed by the Surface Mount Land Patterns Subcommittee (1-13) of the Printed Board Design Committee (1-10) of IPC

Users of this standard are encouraged to participate in the development of future revisions.

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Acknowledgment

Any Standard involving a complex technology draws material from a vast number of sources. While the principal members of the IPC Surface Mount Land Patterns Subcommittee of the Printed Board Design Committee are shown below, it is not possible to include all of those who assisted in the evolution of this Standard. To each of them, the members of the IPC extend their gratitude.

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Surface Mount Design and Land Pattern Standard

1.0 SCOPE

This document provides information on land pattern geometries used for the surface attachment of electronic components. The intent of the information presented herein is to provide the appropriate size, shape and tolerance of surface mount land patterns to insure sufficient area for the appropriate solder fillet, and also to allow for inspection and testing of those solder joints.

1.1 Purpose Although, in many instances, the land pattern geometries can be slightly different based on the type of soldering used to attach the electronic part, wherever possible, land patterns are defined in such a manner that they are transparent to the attachment process being used. Designers should be able to use the information contained herein to establish standard configurations not only for manual designs but also for computer aided design systems. Whether parts are mounted on one or both sides of the board, subjected to wave, reflow, or other type of soldering, the land pattern and part dimensions should be optimized to insure proper solder joint and inspection criteria.

Although patterns are standardized, since they are a part of the printed board circuitry geometry, they are subject to the producibility levels and tolerances associated with plating, etching, or other conditions. The producibility aspects also pertain to the use of solder mask and the registration required between the solder mask and the conductor patterns. (See paragraph 1.2.2).

1.2 Performance Classification Three general end-product classes have been established in associated IPC standards and specifications to reflect progressive increases in sophistication, functional performance requirements and testing/inspection frequency. It should be recognized that there may be an overlap of equipment between classes.

Design requirements determine class. Class definitions are useful for identifying degrees of precision needed to meet design/performance requirements of packaging and interconnecting structures, and establish communication media between design and manufacture and disciplines.

The printed board user has the responsibility to determine the class to which his product belongs. The contract shall specify the performance class required and indicate any exceptions to specific parameters, where appropriate. In the event of conflict between the design requirements and the classes defined herein, the former shall take precedence and be reflected in the master drawing.

These classes are:

CLASS 1 General Electronic Products

Includes consumer products, some computer and computer peripherals, as well as general military hardware suitable for applications where cosmetic imperfections are not important and the major requirement is function of the completed printed board or printed board assembly.

CLASS 2 Dedicated Service Electronic Products

Includes communications equipment, sophisticated business machines, instruments and military equipment where high performance and extended life is required, and for which uninterrupted service is desired but is not critical. Certain cosmetic imperfections are allowed.

CLASS 3 High Reliability Electronic Products

Includes the equipment for commercial and military products where continued performance or performance on demand is critical. Equipment downtime cannot be tolerated, and functionality is required for such applications as life support items, or missile systems. Printed boards and printed board assemblies in this class are suitable for applications where high levels of assurance are required and service is essential.

The land patterns in this standard have the capability of accommodating all three performance classifications.

1.2.1 End-Use Applications In addition to the three performance classifications, the Surface Mount Council has established end use applications for electronic products. These are:

1. *Consumer products* including games, toys, audio and video electronics. In general, convenient size and maximum functionality are important but product cost is extremely important.
2. *General purpose computers*, as used in businesses and personal applications. Compared to consumer products, customers expect longer life and more consistent service.
3. *Telecom products* including telephone, switching systems, PBXs, and exchanges. These products are used in applications expecting long service life and enduring relatively harsh environments.
4. *Commercial aircraft* requiring small size, light weight and high reliability.
5. *Industrial products and passenger compartment automotive applications*. Size and function is a byword of these products. Cost is very important, provided that reducing product cost doesn't forfeit the highest achievable product quality, performance, and function.

6. *High performance products* consisting of ground-based and shipbound military products, high speed and high capacity computers, critical process controllers, and life supporting medical systems. Quality, reliability and performance are paramount, closely followed by size and function. Cost is optimized based on these requirements but is less important.
7. *Space products* include all of the products above which are built to meet harsh outer space conditions. This implies high quality and performance over a wide range of environmental and physical extremes.
8. *Military avionics products* built to meet demanding mechanical and thermal changes. Size, weight, performance and reliability are paramount.
9. *Under the hood automotive electronics products* endure the harshest of all use environments. These products face extreme temperatures and mechanical variations. Adding to this is the pressure of achieving the lowest cost and optimum manufacturability in high volumes.

1.2.2 Producibility Levels When appropriate this standard will provide three design complexity levels of features, tolerances, measurements, assembly, testing of completion or verification of the manufacturing process that reflect progressive increases in sophistication of tooling, materials or processing and, therefore progressive increases in fabrication cost. These levels are:

Level A General Design Complexity—Preferred

Level B Moderate Design Complexity—Standard

Level C High Design Complexity—Reduced Producibility

Producibility levels also pertain to the assembly. The three component mounting complexity levels which reflect progressive increases in sophistication of tooling, assembly and joining techniques and therefore progressive increases in cost are:

Level A simple assembly techniques used to describe through the board component mounting;

Level B moderate assembly techniques used to describe surface component mounting and

Level C complex assembly techniques used to describe intermixing of through-the-board and surface mounting on the same assembly.

Classification of complexity should not be confused with the performance classification of end-item use described in paragraph 1.2.

1.3 Assembly Types A type designation signifies further sophistication describing whether components are mounted on one or both sides of the packaging and interconnecting structure. Type 1 defines an assembly that has components mounted on only one side; type 2 is an assembly with components on both sides. Type 2 is limited to only class B or C assemblies.

Figure 1–1 shows the relationship of two types of assemblies.

The need to apply certain design concepts should depend on the complexity and precision required to produce a particular land pattern or P&I structure. Any design class may be applied to any of the end-product equipment categories; therefore, a moderate complexity (Type 1B) would define components mounted on one side (all surface mounted) and when used in a Class 2 product (dedicated service electronics) is referred to as Type 1B, Class 2. The product described as a Type 1B, Class 2 might be used in any of the end-use applications; the selection of class being dependent on the requirements of the customers using the application.

1.4 Presentation Dimensions and tolerances are expressed in millimeters (mm) or microns (mn) as appropriate. When no unit of measurement is shown, the unit shall be assumed to be ‘‘mm.’’ Reference information for inch conversion is shown in the appendix.

1.5 Profile Tolerances Profile tolerances are used in the dimensioning system for determining the relationship between component outlines and land pattern geometries. The details are described in Section 3.3, and follow the principles set forth in ANSI Y14.5. All dimensions are considered maximum or minimum material condition (depending on the features being analyzed), thus the profile tolerances are unilateral (one-direction—maximum to minimum, or minimum to maximum) as opposed to bilateral (plus or minus) from a nominal characteristic.

1.6 Land Pattern Determination This document discusses two methods of providing information on land patterns:

(1) exact details based on industry component specifications, board manufacturing and component placement accuracy capabilities. These land patterns are registered to a specific component, and have a registered land pattern number, see Table 3.5 and paragraph 3.3.3.4.

(2) equations that can be used to alter the given information to achieve a more robust solder connection, when used in particular situations where the equipment for placement or attachment are more or less precise than the assumptions made when determining the exact land pattern details.

1.6.1 General Usage of SMT In general, a product is a good candidate for SMT if it needs to be:

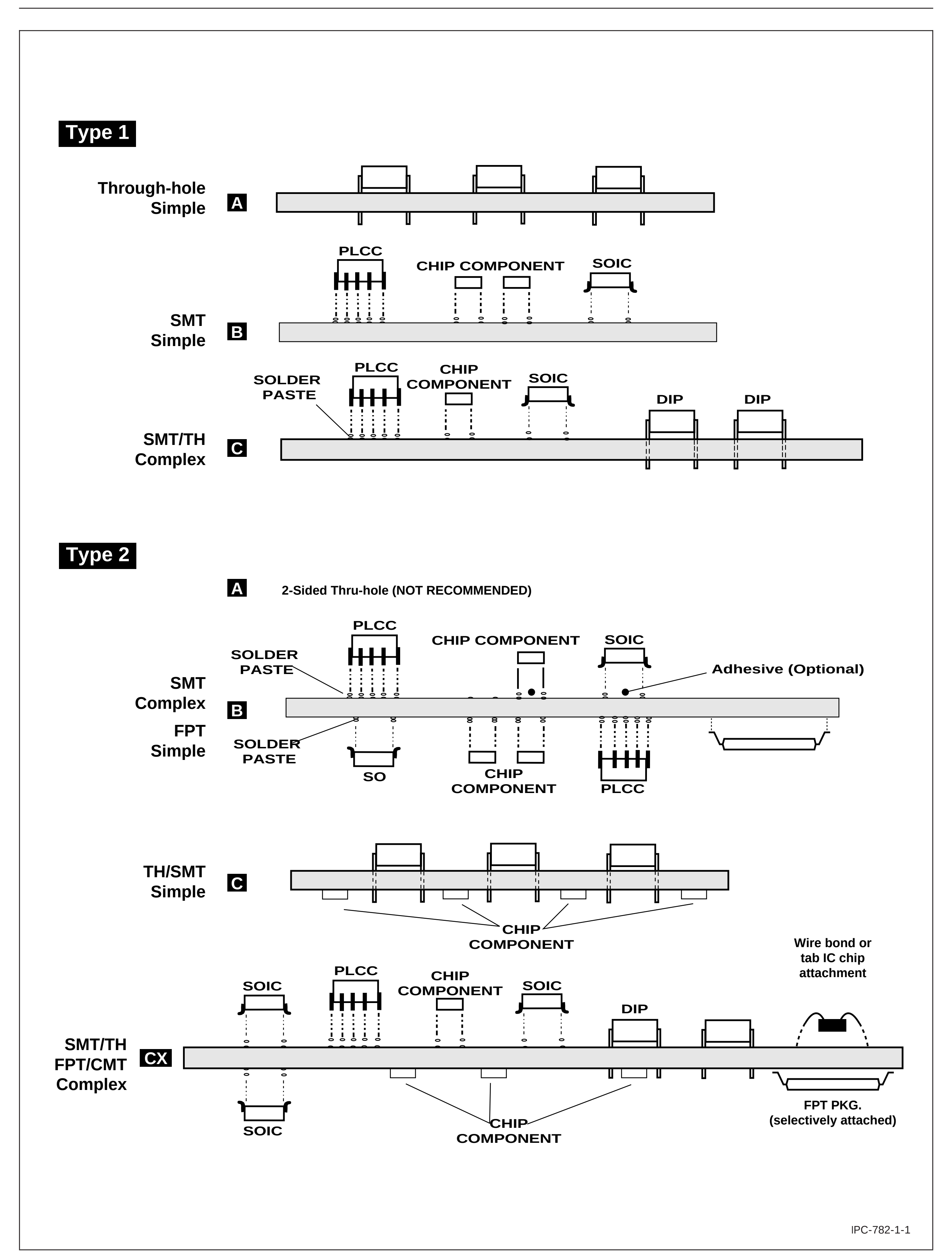


Figure 1–1 Electrical assembly types

- Small in size, real estate constrained
- Able to accommodate large amounts of memory
- Light in weight
- Able to accommodate several large, high lead count complex ICs, such as ASICs and silicon arrays
- Able to function at high frequencies and speeds
- Able to transmit little or no noise, EMI and RFI resistant
- Able to be built in large volumes using automation

Currently, most SMT boards that have 50 or more components use a combination of SMT and through-hole technologies. The mix is a function of component availability, multiplicity of vendors, and cost. A mix of 80 percent SMT and 20 percent through-hole parts is very common. However, the number of 100% SMT assemblies is increasing.

Fine Pitch Technology (FPT) involves a process change as well as a packaging family, because the package to board assembly steps are different than SMT. For example, several commercially available FPT parts require lead excise and forming prior to placement. They are encapsulated or molded with plastic and delivered to users as a separate packaged device, and these parts may be shipped with a molded guard-ring or a slide carrier securing the leads in place. The full encapsulated device will be used for direct board mounting.

FPT packages are available under package names such as PQFP (Plastic Quad Flat Pack), CQFP (Ceramic Quad Flat Pack), QFP (Quad Flat Pack) and VSOIC (Very Small Outline Integrated Circuits).

2.0 APPLICABLE DOCUMENTS

The following documents, of the issue currently in effect form a part of this document to the extend specified herein. Other documents listed are for reference purposes to assist the user.

2.1 IPC[1]

IPC-A-48 Surface Mount Land Pattern Artwork (Mantech)

IPC-A-49 Surface Mount Land Pattern Artwork (IPC-SM-782A)

IPC-T-50 Terms and Definitions

IPC-SC-60 Post Solder Solvent Cleaning Handbook

IPC-AC-62 Post Solder Aqueous Cleaning Handbook

IPC-2221 Generic Standard on Printed Board Design

IPC-6012 Qualification and Performance Standard for Rigid Printed Boards

IPC-D-330 Printed Wiring Design Guide

IPC-A-610 Acceptability of Printed Board Assemblies

IPC-7711 Rework of Electronic Assemblies

IPC-SM-780 Guidelines for Component Packaging and Interconnection with Emphasis on Surface Mounting

IPC-SM-784 Guidelines for Chip-on-Board Technology Implementation

IPC-SM-785 Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments

IPC-SM-786 Recommended Procedures for Handling of Moisture Sensitive Plastic IC Packages

IPC-AJ-820 Assembly and Joining Handbook

IPC-CC-830 Electrical Insulating Compounds for Printed Board Assemblies

IPC-SM-840 Qualification and Performance of Permanent Polymer Coating (Solder Mask) for Printed Boards

IPC-1902/IEC 60097 Grid System for Printed Circuits

2.2 Electronic Industries Association[2]

IS-30 Surface Mount Resistors

JEDEC-95 JEDEC Registered and Standard Outlines for Solid State Products

EIA-PDP-100 Registered and Standard Mechanical Outlines for Electronic Parts

RS-198 Ceramic Dielectric Capacitors

RS-228 Fixed Electrolytic Tantalum Capacitors

RS-367 Dimensional and Electrical Characteristics Defining Receiver Type Sockets

RS-376 Fixed Film Dielectric Capacitors in Metallic and Non- Metallic Cases for D.C. Application

RS-415 Dimensional and Electrical Characteristic Defining Dual-In-Line-Type Sockets

RS-428 Type Designation System for Microelectronic Devices

1. IPC, 2215 Sanders Road, Northbrook, IL 60062-6135
2. Electronic Industries Association, 2001 Eye Street N.W., Washington, DC 20006

RS-471 Symbol and Label for Electrostatic Sensitive Devices

RS-481 Tape and Reel Specification

2.3 Joint Industry Standards (IPC)[1]

J-STD-001 Requirements for Soldered Electrical and Electronic Assemblies

J-STD-002 Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires

J-STD-003 Solderability Tests for Printed Boards

2.4 American Society of Mechanical Engineers[3]

ANSI Y14.5M—1982 Dimensioning and Tolerancing

3.0 DESIGN REQUIREMENTS

3.1 Terms and Definitions Terms and definitions used herein are in accordance with IPC-T-50 except as otherwise specified. ***Note:*** Any definition denoted with an asterisk (*) is a reprint of the definition defined in IPC-T-50.

***Assembly** – A number of parts of subassemblies or any combination thereof joined together.

Note: When this term is used in conjunction with other terms listed herein, the following definitions shall prevail.

Assembly, double-sided – A packaging and interconnecting structure with components mounted on both the primary and secondary sides.

Assembly, multilayer printed circuit – a multilayer printed circuit board on which separately manufactured components and parts have been added.

Assembly, multilayer printed wiring – a multilayer printed wiring board on which separately manufactured components and parts have been added.

Assembly, packaging and interconnecting (P&IA) – The generic term for an assembly that has electronic components mounted on either one or both sides of a packaging and interconnecting structure.

Assembly, printed board – an assembly of several printed circuit assemblies or printed wiring assemblies, or both.

Assembly, printed circuit – a printed circuit board on which
separately manufactured components and parts have been added.

Assembly, printed wiring – a printed wiring board on which
separately manufactured components and parts have been added.

Assembly, single-sided – A packaging and interconnecting structure with components mounted only on the primary side.

***Base material** – The insulating material upon which the conductor pattern may be formed. The base material may be rigid or flexible. It may be a dielectric sheet or insulated metal sheet.

Basic dimension – Theoretically exact location of a component feature, indicated by a symbol or a number in a box. (The tolerance on a basic dimension provides the limits of the variation from the basic dimension location.)

Castellation – Metallized features that are recessed on the edges of a chip carrier which are used to interconnect conducting surfaces or planes within or on the chip carrier.

Chip carrier – A low-profile rectangular component package, usually square, whose semiconductor chip cavity or mounting area is a large fraction of the package size and whose external connections are usually on all four sides of the package.

Chip-on-board (COB) – Integrated circuit device mounted directly to the printed board and interconnected with wire bonds.

Coefficient of thermal expansion (CTE) – The linear thermal expansion per unit change in temperature.

Component – A separable part of a printed board assembly which performs a circuit function (e.g., a resistor, capacitor, transistor, etc.)

Component mounting site – A location on a P&I structure that consists of a land pattern and conductor fan-out to additional lands for testing or vias that are associated with the mounting of a single component.

***Conductive pattern** – The configuration or design of the conductive material on the base material. (Includes conductors, lands, and through connections when these connections are in integral part of the manufacturing process.)

***Conductor** – A single conductive path in a conductive pattern.

Constraining core – A supporting plane that is internal to a packaging and interconnecting structure.

***Dual in-line package (DIP)** – A component which terminates in two straight and parallel rows of pins or lead wires.

Fine-pitch technology (FPT) – Surface mounted components with a lead or termination pitchof 0.63 mm or less.

Fiducial – A feature of the PB used to provide common measurable points for all steps in the assembly process.

Flat pack – A component with two straight rows of leads (normally on 1.27 mm centers) which are parallel to the component body.

3. Publications are available from the American Society of Mechanical Engineers, 345 East 47th St., New York, NY 10017

Footprint **–** (see preferred term ''Land Pattern'')

****Grid*** **–** An orthogonal network of two sets of parallel equidistant lines used for locating points on a printed board. (Note: Connections should be located on the cross-points of the gridlines. The position of conductors may be independent of the grid, i.e., not necessarily following the gridlines.)

Integrated circuit (IC) **–** An assembly of miniature electronic components simultaneously produced in batch processing, on or within a single substrate to perform an electronic circuit function.

****Jumper wire*** **–** An electrical connection that is a part of the original design, added between two points on a printed wiring board after the intended conductive pattern is formed.

****Land*** **–** A portion of a conductive pattern usually, but not exclusively, used for the connection, or attachment, or both of components.

Land pattern **–** A combination of lands intended for the mounting, interconnection and testing of a particular component.

Leadless chip carrier **–** An electronic component whose external connections consist of metallized terminations containing a single integrated circuit chip.

Leaded chip carrier **–** An electronic component whose external connections consist of leads eminating from the sides of the package, which contains a single circuit chip.

****Master drawing*** **–** A document that shows the dimensional limits or grid locations applicable to any or all parts of a printed board (rigid or flexible), including the arrangement of conductive and nonconductive patterns or elements; size, type, and location of holes; and any other information necessary to describe the product to be fabricated.

Mixed mounting technology **–** A component mounting technology that uses both through-hole and surface mounting technologies on the same packaging and interconnecting structure.

****Module*** **–** A separable unit in a packaging scheme

Nominal **–** Design dimension for the size of a feature. (The tolerance on a nominal dimension gives the limits of variation of a feature size.)

Packaging and interconnecting structure (P&IS) **–** The generic term for a completely processed combination of substrates, metal planes or constraining cores, and interconnection wiring used for the purpose of mounting components.

****Plated-through hole (PTH)*** **–** A hole in which electrical connection is made between internal or external conductive patterns, or both, by the plating of metal on the wall of the hole.

Primary side **–** That side of the packaging and interconnecting structure that contains the most or more complex components. The primary side establishes layer one of the P/I structure. (The same as the ''component side'' in through-hole component mounting technology.)

****Printed board*** **–** The general term for completely process printed circuit or printed wiring configurations. It includes rigid or flexible, single, double and multilayer boards.

****Printed wiring*** **–** The conductive pattern intended to be formed on a common base, to provide point-to-point connection of discrete components, but not to contain printed components.

****Registration*** **–** The degree of conformity of the position of a pattern, or a portion thereof, with its intended position or with that of any other conductor layer of a board.

Secondary side **–** That side of the packaging and interconnecting structure that is opposite of the primary side. (The same as the ''solder side'' in through-hole component mounting technology.)

Single in-Line package (SIP) **–** A component which terminates in one straight row of pins and lead wires.

Static electricity **–** An electrical charge that has accumulated or built up on the surface of a material.

Static electricity control **–** A technique where materials and systems are employed to eliminate/discharge static electricity buildup by providing continuous discharge paths.

****Supported hole*** **–** A hole in a printed board that has its inside surface plated or otherwise reinforced.

Supporting plane **–** A planar structure that is a part of a packaging and interconnecting structure to provide mechanical support, thermo-mechanical constraint, thermal conduction and/or electrical characteristics. (It may be either internal or external to the packaging and interconnecting structure.)

Surface mount technology (SMT) **–** The technology where electrical connection of components is made to the surface of a conductive pattern of a printed board and does not utilize component lead holes.

Thermal expansion mismatch **–** The absolute difference in thermal expansion of two components.

****Through connection*** **–** An electrical connection between conductive patterns on opposite sides of an insulating base, e.g., plated-through hole or clinched jumper wire.

Through-hole technology (THT) **–** An assembly process for mounting component packages where leads are passed through supported (plated through) or unsupported (bare) holes in an interconnection substrate.

****Tooling feature*** **–** A specified physical feature on a printed board or a panel such as a marking, hole, cut- out, notch,

slot or edge, used exclusively to position the board or panel or to mount components accurately. (See Fiducial)

***Via** – A plated-through hole used as a through connection, but in which there is no intention to insert a component lead or other reinforcing material.

Blind via – A via that is connected to either the primary side or secondary side and one or more internal layers of a multilayer packaging and interconnecting structure, but not to both sides.

Buried via – A via that is connected to neither the primary side nor the secondary side of a multilayer packaging and interconnecting structure, i.e., it connects only between inner layers.

Tented via – A blind or through-hole via that has the exposed surface of the primary or secondary or both sides of a packaging and interconnecting structure fully covered by a masking material, such as a dry film polymer coating (solder mask), preimpregnated glass cloth (prepreg), etc., in order to prevent hole access by process solutions, solder, or contamination.

3.2 Component Acronyms In an attempt to standardize on component characteristics the Joint Electronic Device Engineering Council (JEDEC) of the Electronic Industries Association (EIA) has developed a set of recommended acronyms that can be used to describe the shape, material, lead position, package style, lead form and lead count. These details are defined in JEDEC Publication JESD1C and have been circulated and approved as an international document published by the International Electrotechnical Commission (IEC) as IEC Publication 30. These concepts are supported and adopted in this land pattern document to facilitate communication between design, component manufacturer, board manufacturer, quality assurance etc.

Some of the information from the JEDEC publication is presented to assist the reader. The acronym systems is divided into six parts. They are:

- SHAPE – A single-letter prefix that identifies the mechanical package profile (round, rectangular, square, etc.)
- MATERIAL – A single-letter prefix that identifies the predominant package body material (glass, metal, plastic, etc.)
- POSITION – A single-letter prefix that identifies terminal or lead position related to the package profile (see 3.2.1)
- PACKAGE – A double-letter designation that identifies the package-outline style (see 3.2.2)
- FORM – A single letter suffix that identifies the terminal or lead form (see 3.2.3)
- COUNT – A one, two, or three-digit suffix that identifies the number of leads or terminations (12, 84, 160, etc.)

The minimum acronym consists of the position, package, form and count identifiers. Shape and material prefixes are optional acronym designations. As an example the designation R-PDIP-T14 describes a rectangular part (R), made of plastic (P), with dual terminals or leads (D), coming from an in-line package style (IP) with through-hole leads (T) and a lead count of 14.

3.2.1 Position Designation The single-letter prefix for terminal position shall be identified in accordance with Table 3–1. The position definition ‘‘terminal’’ applies to either lead or leadless. The descriptions assume that the seating plane is the bottom of the package. Reference to package shape does not take into account flanges, notches or irregularities.

3.2.2 Package-Outline Style Designators The package double-letter designator shall be in accordance with Table 3–2. Figure 3–1 provides some examples of the compulsory package outline style acronyms.

3.2.3 Form Designation The single-letter suffix that defines the terminal form (termination or lead) configuration shall be in accordance with Table 3–3. Figure 3–2 shows a few diagrams of various package lead configurations.

3.3 Dimensioning Systems There are many methods of dimensioning and tolerancing mechanical parts, all of which are defined in ANSI Y14.5. All the methods work, but it must be recognized that some methods work better than others and some methods cost less to inspect or evaluate product than others. This section describes a set of dimensional criteria for components, land patterns, positional accuracy of the component placement capability and the opportunity to create a certain size solder joint commensurate with reliability or product performance analysis.

Sections 8.0 through section 13.0 define the specific details of various electronic and electromechanical component families. Each section describes the mounting dimensions for the component and the specific land pattern that may be used to surface mount that particular component or component family. In addition, an analysis is made to establish the land pattern sizes that take into account the accuracy of the placement operation and requirements for the solder joint.

Profile tolerances are used in the dimensioning system to control the size range between maximum and minimum component/lead dimensions without ambiguity. The profile tolerance is intended to control both size and position of the land. Figure 3–3 shows the profile tolerancing method.

The use of the profile dimensioning system requires an understanding of the concepts detailed in ANSI Y14.5. The use of a set of requirements are adopted and invoke the following rules, unless otherwise modified:

Table 3–1 Terminal Position Prefixes

Code	Name	Position (see notes 1 and 2)
A	Axial	Terminal extend from both ends in the direction of the major axis of a cylindrical or elliptical package.
B	Bottom	Terminals beneath the seating plan of the package.
D	Dual	Terminals on opposite sides of a square or rectangular package or located in two parallel rows.
E	End	Terminals are package endcaps having circular or elliptical cross section.
L	Lateral	Terminals are on the four sides of a square or rectangular package. The preferred name is ‘‘Quad,’’ code Q.
P	Perpendicular	Pins are perpendicular to seating plan on a square or rectangular package. Restrict to PGA family.
Q	Quad	Terminals are on the four sides of a square or rectangular package or located in four parallel rows.
R	Radial	Terminals extend radially from the periphery of a cylindrical or spherical package
S	Single	Terminals are on one surface of a square or rectangular package in a single row.
T	Triple	Terminals are on three sides of a square or rectangular package.
U	Upper	Terminals are perpendicular to and opposite the seating plane, and are on one surface of a package.
X	Other	Terminal positions other than those described.
Z	Zig-zag	Terminals are on one surface of a square or rectangular package arranged in a staggered configuration. Restrict to ZIP family.

NOTE 1: These descriptions assume the seating plane is the bottom of the package.
NOTE 2: Reference to package shape does not take into account flanges, notches, or irregularities.

Table 3–2 Package-Outline-Style Codes

Code	Outline Style
CC	Chip-carrier package
CY	Cylinder or can package
DB	Disc-button package
FM	Flange-mount package
FO	Fiber-optic-device package
FP	Flatpack package
GA	Grid-array package
IL	In-line package. The preferred designator is IP
IP	In-line package or inserted package. Restrict to DIP/SIP/ZIP.
LF	Long-form horizontal package.
MA	Microelectronic assembly.
MW	Microwave package
PF	Press-fit package
PM	Post-/stud-mount package
SO	Small-outline package
SS	Special-shape package
UC	Uncased chip
XA-XZ	Nondefiend family; vendor or user option.

a. All dimensions are basic (nominal)

b. Limits of size control form as well as size.

c. Perfect form is required at maximum dimensions.

d. Datum references and position tolerances apply at maximum dimensions, and are dependent on feature size.

e. Position dimensions originate from maximum dimensions.

f. Tolerances and their datum references other than size and position apply regardless of feature size (RFS).

g. Interpretations are per ANSI Y14.5.

The dimensioning concepts used for this system of analysis consider the assembly/attachment requirements as their major goal. Specification (data) sheets for components or dimensions for land patterns on boards may use different dimensioning concepts, however, the goal is to combine all concepts into a single system. Users are encouraged to establish the appropriate relationship between their dimensioning system(s) and the profile dimensioning system and analysis concepts described herein to allow for ease of tailoring these concepts for robust process performance. As an example, if the tolerance used for positioning is larger than the machine tolerance used in production, a single dimensional change in a ‘‘spread sheet’’ program could modify the land pattern dimensions shown in sections 8.0 through 13.0 in order to optimize the process for a given facility.

3.3.1 Component Tolerancing The component manufacturers and the Electronic Industries Association (EIA) are responsible for the dimensioning and tolerancing of electronic components. Their concepts have been converted to a functional equivalent using the profile tolerancing method with all components shown with their basic dimensions as limit dimensions (maximum or minimum size).

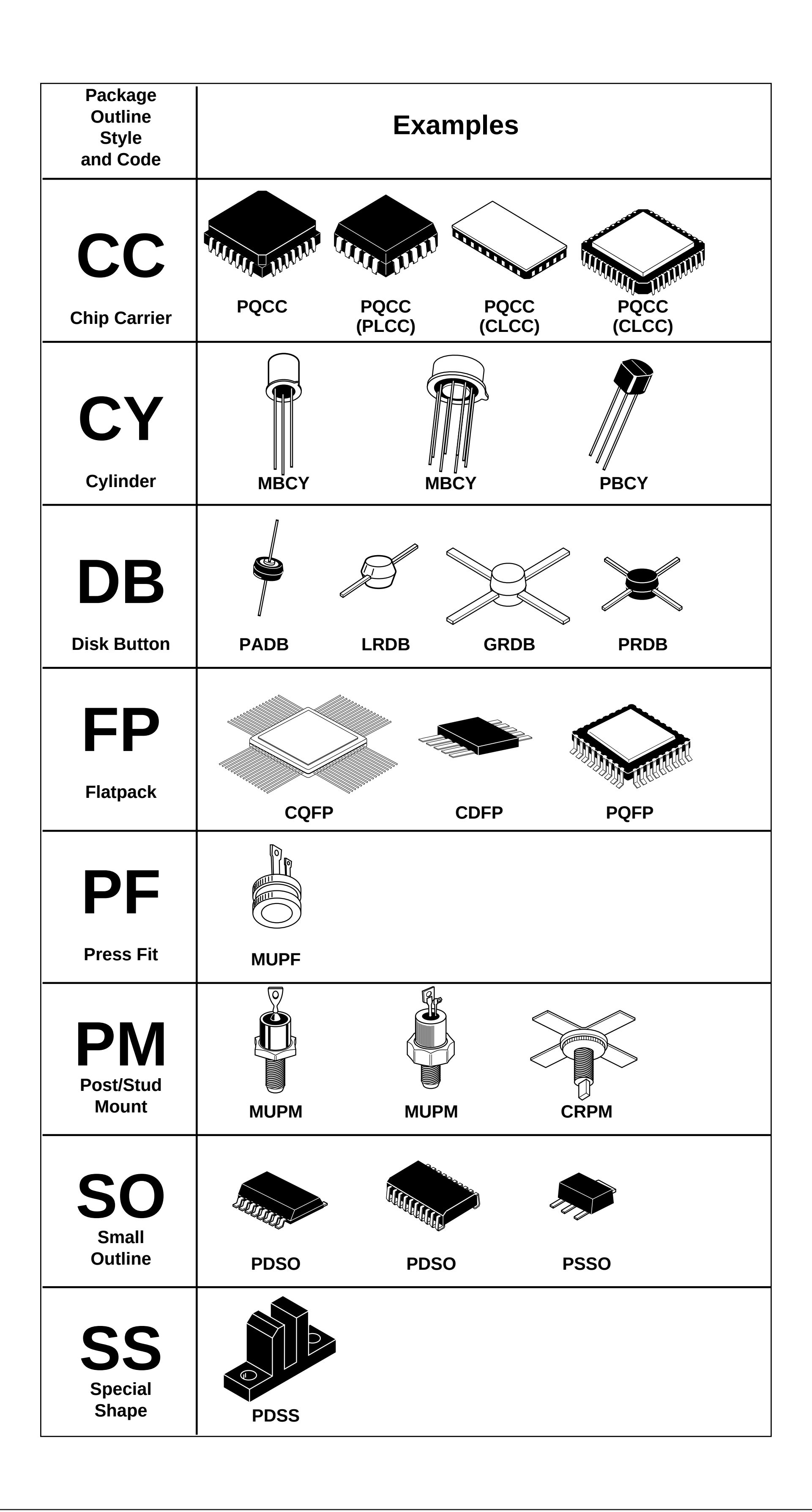


Figure 3–1 Examples of typical package styles and package descriptive designators

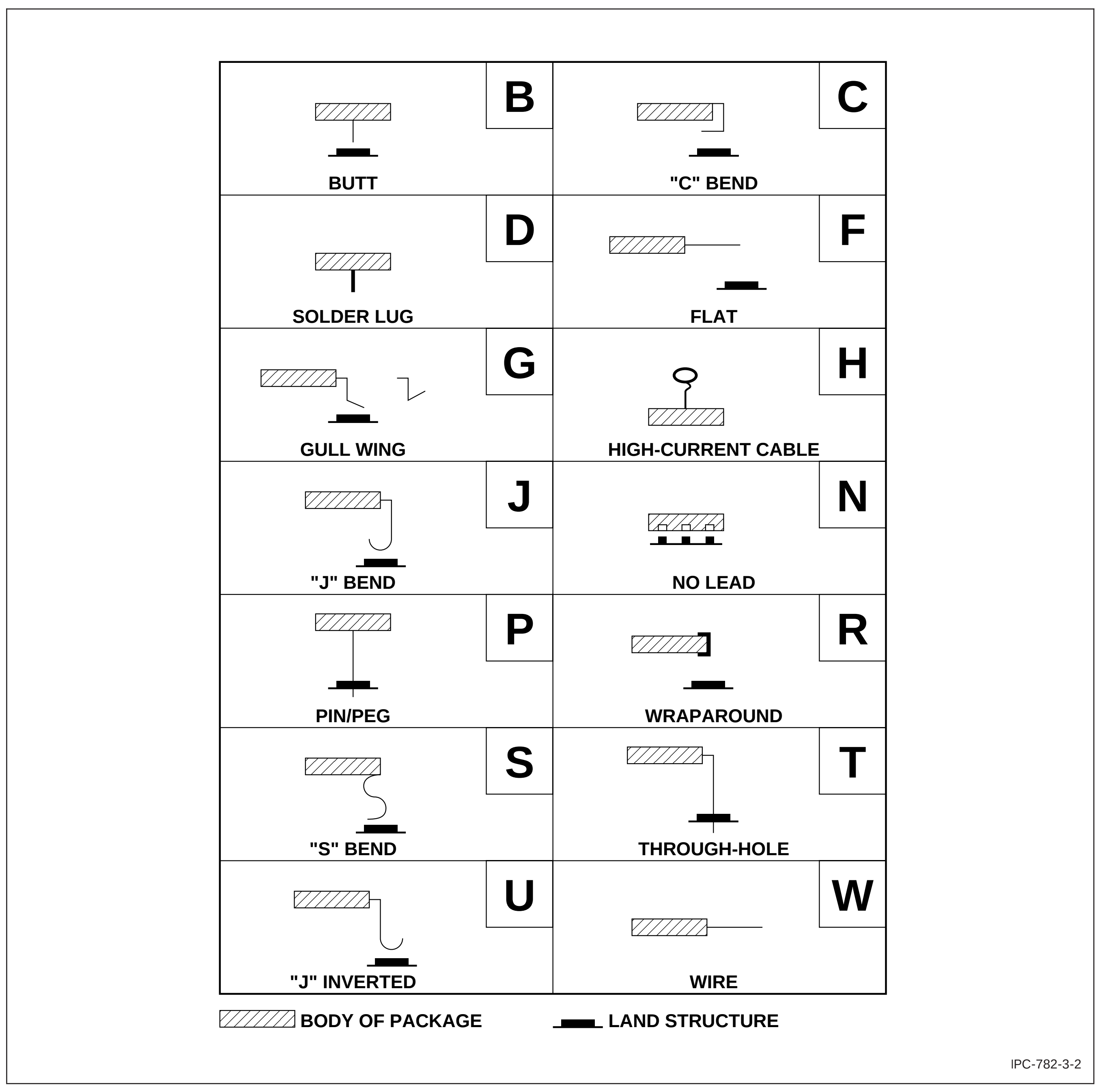


Figure 3–2 Lead-form (or terminal-shape) examples

Profile tolerances are unilateral, and are described to reflect the best condition for solder joint formation usually at minimum component size. As the profile tolerance moves in this unilateral direction toward maximum component size, the opportunity for a robust solder joint decreases.

The concept for component dimension evaluations is based on evaluating the surfaces of the component termination and component lead that are involved in the formation of the acceptable solder joint. Component manufacturers usually provide dimensions for their parts with a nominal size and then put a tolerance on that nominal dimension. Inorder to facilitate the dimensioning system, these dimensions and their associated tolerances are converted to minimum and maximum size.

As an example, capacitor C1206 has a manufactured nominal dimension for its length (L) of 3.2 mm. The tolerance described by the manufacturer is ~ 0.2 mm. Thus, the minimum dimension of ‘‘L’’ is 3.0 mm with a unilateral tolerance of 0.4 mm, resulting in its maximum dimension being 3.4 mm.

Figure 3–4 shows the characteristics for the C1206. Figure 3–4a shows the component manufacturers dimensions for

Table 3–3 Lead-Form (or Terminal-Shape) Suffixes

Code	Form/Shape	Description (see Figure A2)
B	Butt	A noncompliant lead intended for attachment perpendicular to the land structure.
C	“C” bend	A “C” shaped noncompliant lead bent down and under the body of the package.
D	Solder lug	A lug terminal on the package
F	Flat	A noncompliant, nonformed flat lead that extends away form the body of the package.
G	Gull wing	A compliant lead bent down from the body of the package with a foot at the end pointing away from the package.
H	High-current cable	A lug terminal at the end of a flexible lead.
J	“J” bend	A “J” shaped compliant or noncompliant lead bent down and back under the body of the package.
N	No lead	Metallized terminal pads located on the body of the package.
P	Pin/Peg	A tempered lead extending from the body of the package and intended for attachment to a plated through-hole in the land structure.
R	Wraparound	A metallized noncompliant terminal wrapped around the package body.
S	“S” bend	An “S” shaped compliant lead bent under the body of the package.
T	Through-hole	A terminal with flat or V-shaped cross section intended for attachment to a plated through-hole in the land structure.
U	“J” inverted	A “J” shaped compliant or noncompliant lead bent down form the doby of the package with the curved end pointing away from the package.
W	Wire	An untempered wire lead extending from the body of the package.
X	Other	A lead form or terminal shape other than those defined.

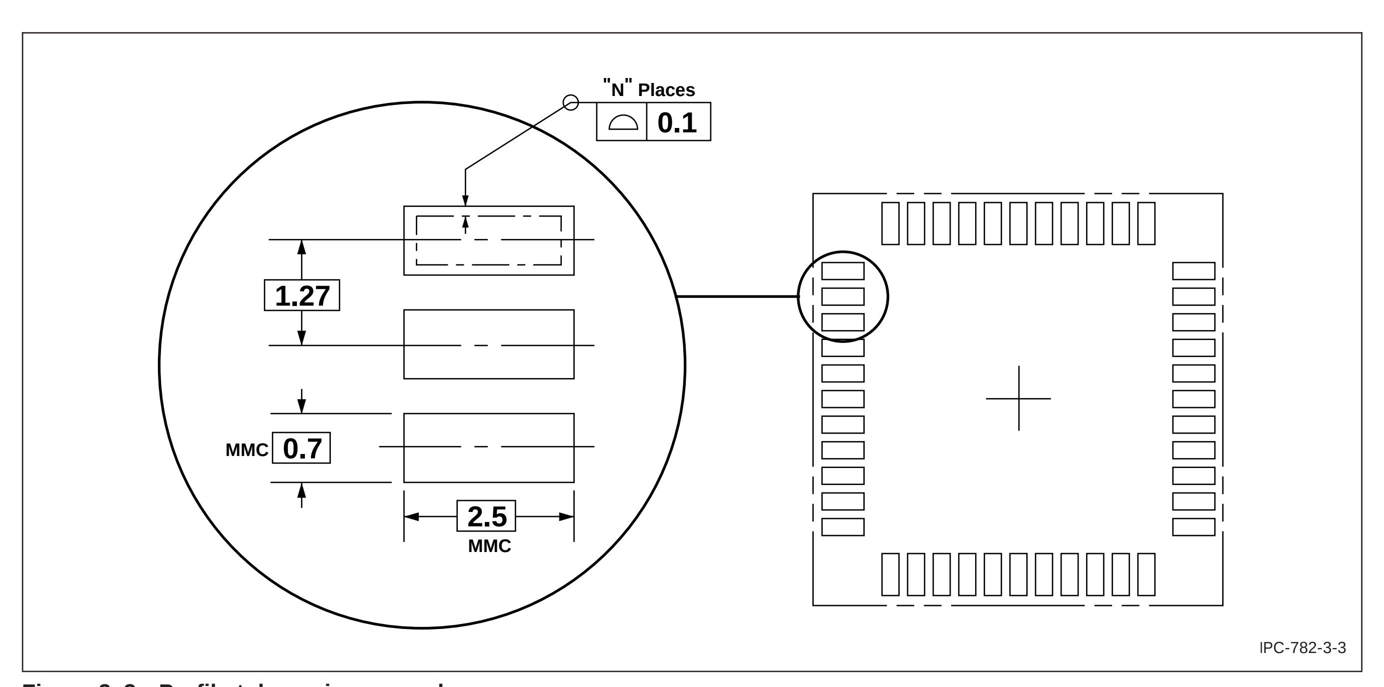


Figure 3–3 Profile tolerancing examples

the length of the capacitor. Figure 3–4b shows the component length at its minimum size in the converted dimensions of the new system using profile tolerancing. Figure 3–4c shows the land pattern at its maximum size. These conditions provide for an optimum toe fillet. For optimum heel fillet the component basic dimensions are at the maximum and the land pattern is at its minimum.

Similar concepts are applied to leaded surface mount parts. The critical dimensional characteristics identified are those that relate to the formation of the toe and heel solder fillet.

For components with gull wing leads the basic dimensions apply across the outer extremities of the part for toe solder fillet formation; and within the inside of the formed radius of opposing leads for heel solder fillet formation.

The outer dimensions of leaded or even leadless chip carriers are usually easy to determine since these are readily available from the component manufacturer. The inner (heel-to-heel) dimensions are not provided in industry standards or manufacturer’s specifications, and are more difficult to determine, not only because of the form of the lead,

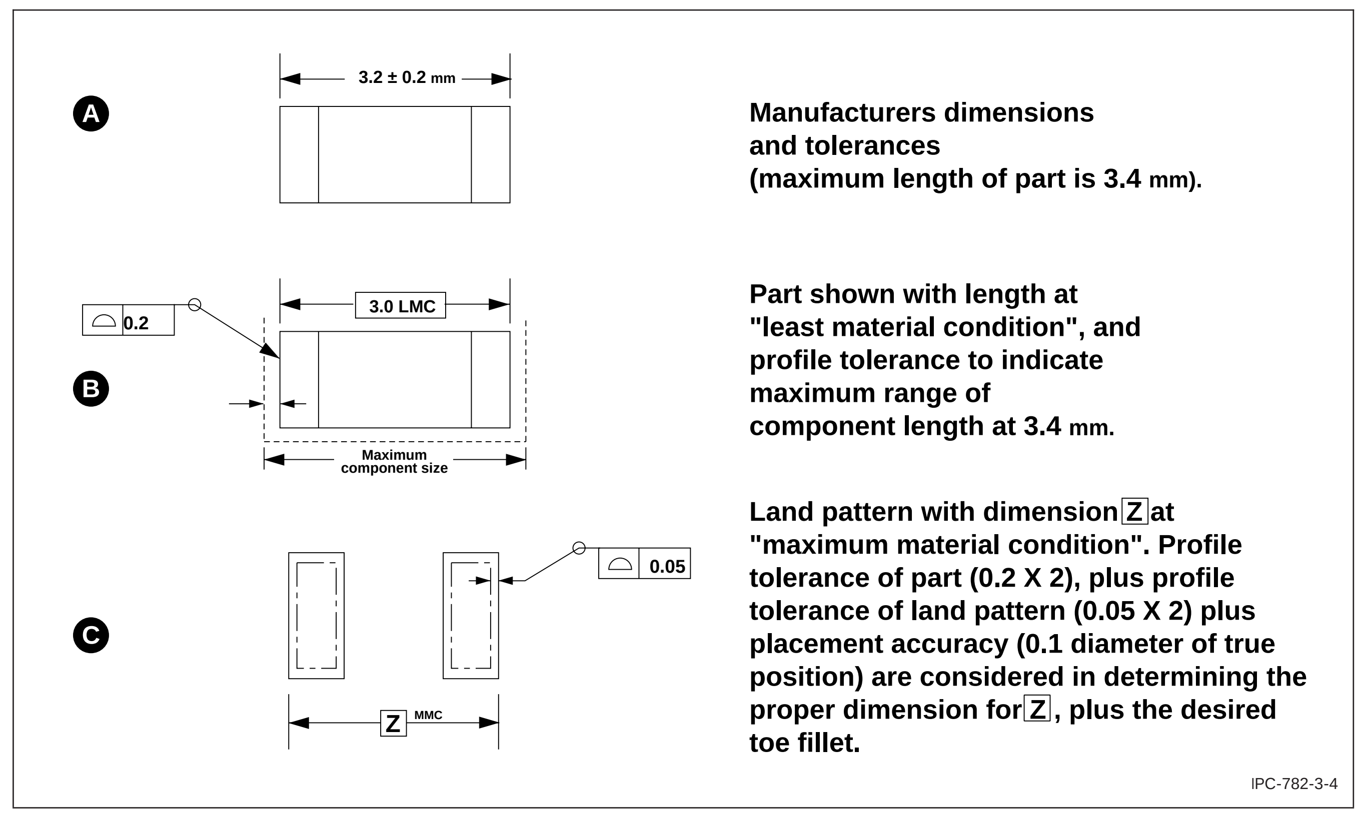


Figure 3–4 Example of C1206 capacitor dimensioning for optimum solder fillet conditions

termination, or castellation; but also because the inner dimensions must be derived by subtracting the sum of the dimensions of the leads (with all their inherent tolerances) from the overall dimensions of the part.

Figure 3–5a shows the concept for the manufacturers dimensions and tolerances for a gull-wing SOIC. Figure 3–5b shows the converted dimensions to be considered in the overall mounting system requirements. Figure 3–5c shows the land pattern dimensions. The basic dimensions define the minimum length as measured across the two outer extremities. Tolerances increase this dimension to the maximum width, reducing toe fillet opportunity. The inner dimensions between heel fillets on opposing sides are the most important. Inner dimensions are derived by:

a. Establishing the maximum width of the component as measured from lead termination to lead termination. (This dimension is shown as ''L,'' and is provided by the manufacturer).

b. Establishing the minimum amount of the lead length as measured across the ''footprint'' (from heel to toe for gull-wing leads). (This dimension is ''T,'' and is provided by the manufacturer).

c. Subtracting twice the minimum lead length of (b) from the maximum overall component length of (a) to arrive at the maximum length inside the leads across the length of the component (the inner dimension between opposing heel fillets). Including the tolerances on dimensions (a) and (b) will yield the minimum dimension between opposing heels. This signifies worst case tolerance analysis.

d. Three sets of tolerances are involved in the analysis described in (c.); tolerances on the overall component, plus the tolerances for the lead on each end. Since not all three tolerances are considered at their worse case, a recommended method for determining the statistical impact is to summarize the squares of the tolerances and take the square-root of their sum as the rms (root-mean-square) tolerance difference.

For example:

RMS tolerance accumulation $= \sqrt{(L_{tol})^2 + 2(T_{tol})^2}$

Where:

$L_{tol} = L_{max} - L_{min}$

$T_{tol} = T_{max} - T_{min}$

As an example, the SOIC with 16 leads has the following limits for the ''L'' (component length) and ''T'' (terminal length) dimensions:

L_{min} = 5.8 mm, L_{max} = 6.2 mm

$L_{tol} = L_{max} - L_{min}$ = 6.2 – 5.8 = 0.4 mm

T_{min} = 0.4 mm, T_{max} = 1.27 mm

$T_{tol} = T_{max} - T_{min}$ = 1.27 – 0.4 = 0.87 mm

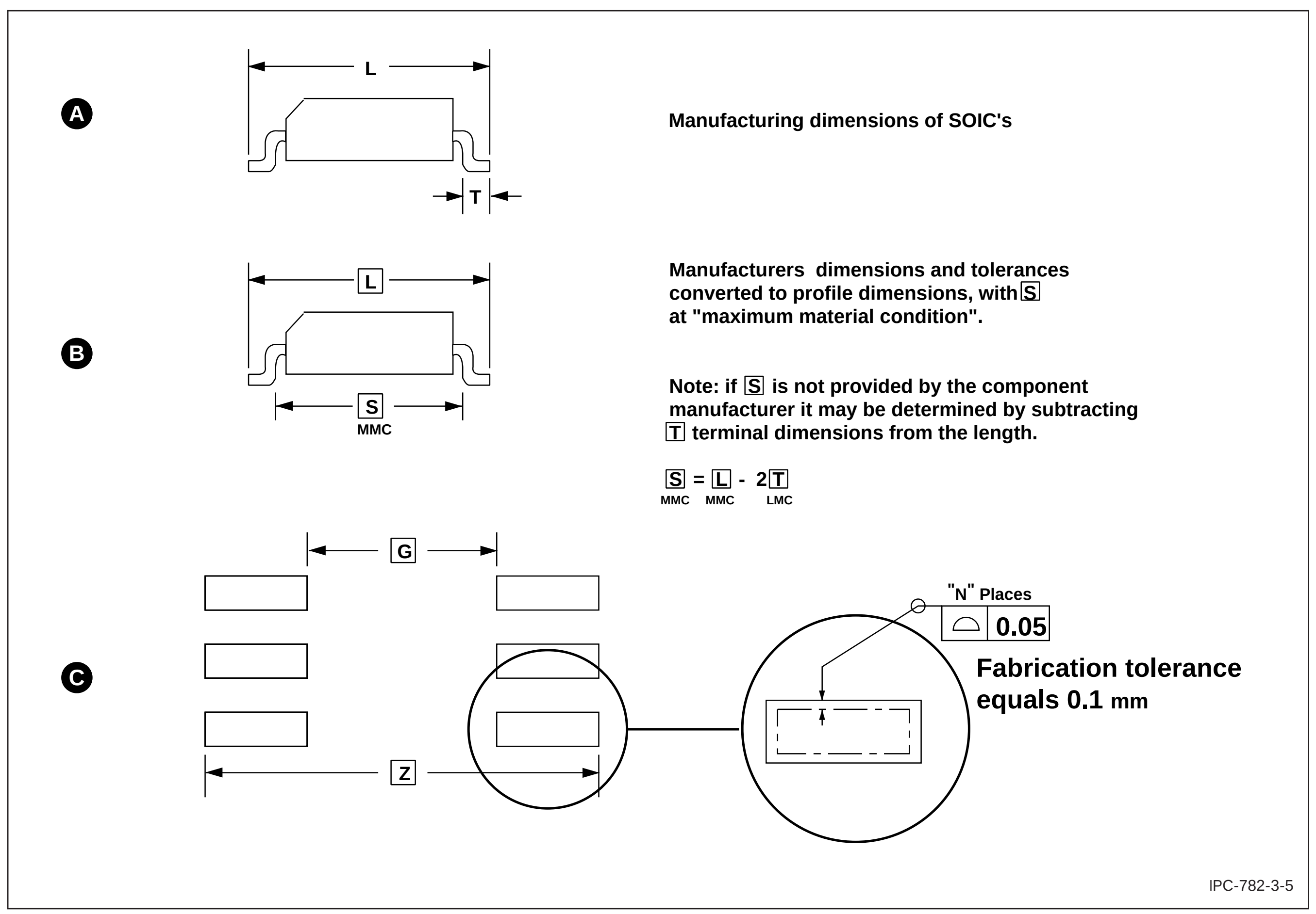


Figure 3–5 Profile dimensioning of a gullwing leaded SOIC

Therefore, the calculations for ''S'' minimum and maximum dimensions are as follows:

$S_{min} = L_{min} - 2T_{max} = 5.8 - 2(1.27) = 3.26$

$S_{max} = L_{max} - 2T_{min} = 6.2 - 2(0.4) = 5.4$ mm

$S_{tol} = S_{max} - S_{min} = 5.4 - 3.26 = 2.14$ mm

The difference between S_{min} and S_{max} is 2.14 mm, which is probably a larger tolerance range than the actual range within which these components are manufactured. This worst-cast scenario for the tolerance range for ''S'' can also be calculated by adding the tolerances for the component length and the two terminals:

$S_{tol} = L_{tol} + 2T_{tol} = 0.4 + 2(0.87) = 2.14$ mm

In order to arrive at a more realistic tolerance range, the RMS (root-mean-square) value is calculated using the tolerances on the dimensions involved (''L'' and ''T''):

$$S_{tol}\text{ (rms)} = (L_{tol})^2 + 2(T_{tol})^2 = \sqrt{0.4^2 + 2(0.87)^2} = 1.29\text{mm}$$

S_{tol} (rms) is added to S_{min} to arrive at a maximum ''S'' dimension. This technique is used so that a more realistic S_{max} dimension is used in the land pattern equations for calculating G_{min} (minimum land pattern gap between heel fillets). In this example, the following calculation is used for S_{max}:

S_{max} (rms) = S_{min} + S_{tol} (rms) = 3.26 + 1.29 = 4.55 mm

To determine the G_{min} dimension for the land pattern, S_{tol} (rms) is used for the component tolerance (i.e., S_{tol} (rms) = ''C''). The calculations for G_{min} are as follows:

$$G_{min} = S_{max} - 2J - \sqrt{C^2 + F^2 + P^2}$$

Where:

J = 0.5 mm (target heel fillet)

C = S_{tol} (rms) = 1.29 mm (see above calculations from component dimensions)

F = 0.1 mm (assumed fabrication tolerance)

P = 0.1 mm (assumed assembly equipment placement tolerance)

Therefore:

$$G_{min} = 4.55 - 2(0.5) - \sqrt{(1.29)^2 + (0.1)^2 + (0.1)^2} = 2.25\text{ mm}$$

Another major condition for multiple-leaded components that must be considered in land pattern design is lead, termination, or castellation pitch. The pitch describes the

basic dimension of the spacing of one component lead termination or castellation to its adjacent counterpart(s). No tolerance is assigned to pitch in the profile dimensioning concept. Differences in pitch shall be included in the width dimensions of the lead, termination, or castellation which are dimensioned as basic at the minimum size.

3.3.2 Land Tolerancing Profile tolerancing is used for lands in a manner similar to that of the components. All tolerances for lands are intended to provide a projected land pattern with individual lands at maximum size. Unilateral tolerances intend to reduce the land size and thus result in a smaller area for solder joint formation. In order to facilitate companion dimension systems the land pattern is dimensioned across outer and inner extremities.

The dimensioning concept in this standard uses limiting dimensions and geometric tolerancing to describe the allowable maximum and minimum dimensions of the land pattern. When lands are at their maximum size, the result is a minimum acceptable space between conductors; conversely when lands are at their minimum size, the result is the minimum acceptable land pattern necessary to achieve reliable solder joints. These thresholds allow for gauging of the land pattern for go/no-go conditions. The whole concept of the dimensioning system described in this document is based on these principles and extends to component mounting dimensions, land pattern dimensions, positioning dimensions etc., so that the requirements may be examined using optical gauges at any time in the process in order to insure compliance with the tolerance analysis.

Figure 3–5 shows the land pattern for an SOIC with gullwing leads intended to be a companion to the chip component dimensioning concepts shown in Figure 3–4. The basic dimension is across the outer extremities.

Dimension ''Z'' is at maximum size, while the inner extremities (dimension ''G'') are dimensioned at minimum size. Unilateral tolerances decreased the basic dimension for ''Z'' while increasing the basic ''G'' dimension. This action results in a reduced land pattern, thus processing target values should be as close to the basic ''Z'' and ''G'' dimensions as possible. This concept also holds true for the width (X) of the land dimension which is specified at maximum size.

3.3.3 Dimension and Tolerance Analysis In analyzing the design of a component/land pattern system, several things come into play. The size and position tolerances of the component lead or termination, the tolerances of the land pattern, the placement accuracy of the man/machine to center the part to the land pattern, and finally the amount of solder area available for a solder joint for formation of a toe, heel or side fillet.

System equations have been developed for chip components and multiple leaded parts. These concepts assume that the target values of parts and land patterns are maximized to reflect solder joint formation (i.e., outer dimensions of components at minimum size with outer dimensions of land patterns at maximum size). The equations use the following symbols:

C = the unilateral profile tolerance(s) for the component

F = The unilateral profile tolerance(s) for the board land pattern

P = the diameter of true position placement accuracy to the center of the land pattern

With the assumption that a particular solder joint or solder volume is desired for every component, some methods use the worst case criteria for determining a dimension. This would require that ''C,'' ''F,'' & ''P'' be added to the minimum dimension of the component length plus the solder joint requirements, in order to determine the maximum dimension of the outer land pattern.

Experience shows that the worst case analysis is not always necessary, therefore statistical methods are used by taking the square root of the sum of the squares of the tolerances. This method assumes that all features will not reach their worst case. The equations for determining chip component land pattern requirements are as follows:

$$Z\,max = L\,min + 2J_T + \sqrt{C_L^2 + F^2 + P^2}$$

$$G\,min = S\,max - 2J_H - \sqrt{C_S^2 + F^2 + P^2}$$

$$X\,max = W\,min + 2J_S + \sqrt{C_W^2 + F^2 + P^2}$$

Where:
Z = Overall length of land pattern
G = Distance between lands of the pattern
X = Width of land pattern

L = Overall length of component
S = Distance between component terminations
W = Width of component

J = Horizontal dimension of solder fillet
- J_t = Solder fillet at toe
- J_h = Solder fillet at heel
- J_s = Solder fillet at side

C = Component tolerances
- C_L = Tolerance on component length
- C_S = Tolerance on distance between component terminations
- C_W = Tolerance on component width

F = Printed board fabrication (land pattern geometric) tolerances

P = Part placement tolerance (placement equipment accuracy)

The formula (the square root of the sum of the squares) is identical for both toe and heel solder joint formation (different tolerances are used, however). However, the desired

solder joint dimension and the square root of the sum of the squares are added for outer land pattern dimensions and subtracted for inner land pattern dimensions. The result provides the final land pattern dimensions (Z, G, and X) for chips.

The same concept is true for multiple leaded or leadless components. Additionally, pitch with land-to-lead overlap (M) can be evaluated as well as the space (N) to reflect the clearance between a lead, termination, or castellation and the adjacent land(s). These latter values are not used in the equations to determine the land pattern sizes, but may be used to limit lead-to-adjacent land proximity and to adjust lead-to-land overlap. See Figure 3–6.

The equation for determining if the clearance ''N'' or the attachment overlap ''M'' are sufficient is as follows:

$$M = \left[\frac{W + X}{2}\right] - \sqrt{C^2 + F^2 + P^2}$$

$$N = E - \left[\frac{W + X}{2}\right] + \sqrt{C^2 + F^2 + P^2}$$

3.3.3.1 Tolerance Analysis The following tolerance concepts are used to determine the land patterns for all electronic components. These concepts are detailed in Table 3-4, and reflect the tolerances on the component, the tolerances on the land pattern (on the interconnecting substrate), and the accuracy of the equipment used for placing components.

Solder joint minimums are shown for toe, heel and side fillets. These conditions are minimum, since the equations in 3.3 address the tolerance of component, board, and placement accuracy tolerances (sum of the squares). The minimum solder joint is increased by the amount that the tolerances are not used up.

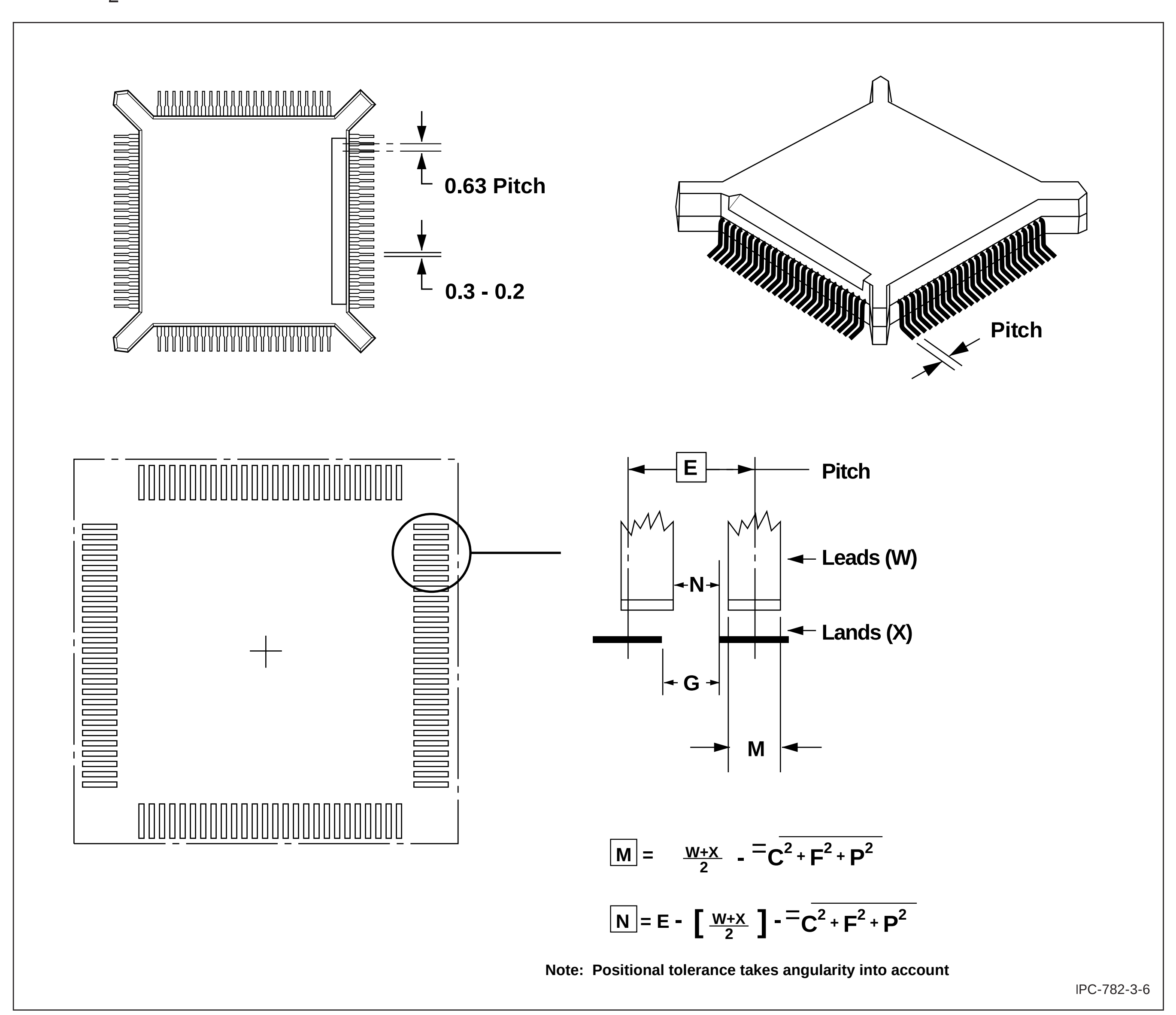


Figure 3–6 Pitch for multiple-leaded components

If the user of these land patterns desires a more robust process condition for placement and soldering equipment, individual elements of the analysis may be changed to new and desired dimensional conditions. This includes component, board or placement accuracy spread as well as minimum solder joint expectations.

Table 3–4 Tolerance Analysis Elements for Chip Devices

Tolerance Element	Detailed Description
Component Tolerance	The difference between the MMC and the LMC of each component dimension, length, width and distance between electrodes or leads. This number is the "C" tolerance in the equations.
Board Tolerance	The difference between the MMC and the LMC of each land pattern dimension. This number is "F" tolerance in the equations.
Positional Accuracy	0.1 – 0.2 mm DTP
Toe Fillet	0.4 – 0.6 mm
Heel Fillet	0.0 – 0.2 mm
Side Fillet Width	–0.02 – 0.02 mm

3.3.3.2 Component Dimensions Illustrations of component dimensions beginning in each component section are accompanied by table of figures for each of the different part numbers, as taken from EIA-PDP-100, JEDEC-95 and other world wide component standards.

EIA-PDP-100 is a catalogue listing of outline drawings illustrating the dimensions of supplier registered passive components; JEDEC-95 as the outlining document for solid state products. At times, the component tolerances or component gauge requirements do not necessarily reflect the exact tolerance on a manufacturers data sheet. Usually, this occurs when industry component specification ranges are so broad that they defy good surface mount design principles. When this action is taken, the tolerance is indicated with an asterisk (*).

Component dimensions are provided according to the concepts of maximum and least materials condition (MMC and LMC). Both conditions are presented in the tables. The component manufacturer may not always dimension his component in accordance with the limits shown in the tables, however, these limits may be used as a gauge for go/no-go acceptance of the component. The LMC dimensions of the figure are those that have been used in the equations described in 3.3 for determining the recommended land pattern.

Dimensions that have had their tolerance spread reduced are so indicated in the tables. Parts that are available with shape characteristics or tolerance limits that fall outside the recommended norms require land patterns that must be altered slightly from those presented.

Users of these specialized parts are encouraged to develop their own land patterns which then become unique to a specific component vendor part. A dimensioning system with specific equations has been provided to facilitate unique land pattern development or enhance process usage.

3.3.3.3 Land Pattern Dimensions Land pattern dimensions are provided according to the concepts of maximum material conditions (MMC). Sometimes a dimension is presented as a minimum distance. This occurs when defining a space(s) that exists between lands at MMC. The printed board manufacturer may not always inspect his board in accordance with the limit concepts shown in the table. However, these limits may be used as a gauge for go/no-go acceptance of the printed board land pattern. The dimensions shown in each table are those that have been used in the equations described in 3.3 for determining the recommended land patterns.

All land patterns are designed to be transparent to the soldering process to be used in manufacturing. This reduces the number of land sizes in the component library, and is less confusing for the designer, but may not be the most robust for the placement or the soldering process.

3.3.3.4 Land Pattern Registration Each land pattern has received a registration number. The RLP (Registered Land Pattern) number is a three digit number with a set of numbers assigned to land patterns for a particular family of components. The original number assigned to a particular component, uses that analysis shown for the specific section (sections 8 through 16). The analyses assume certain tolerances for board fabrication, placement machine accuracy and minimum desired solder joint. Changes in the assumptions will result in a revision letter to the number. Thus the first change to RLP 106 would be identified as RLP 106A, the second change would be RLP 106B etc.

The letters x, y & z are reserved for user modifications to the standard land pattern. If a company wishes to change the approved standard land pattern the user would identify his customized version as RLP 106X, RLP 106Y or RLP 106Z. It should be recognized that X, Y & Z type RLP's reflect unique land patterns and will differ company to company. The number reservations are shown in Table 3-5.

Not every RLP is assigned in Sections 8 through 16, however all three digit number from 100 to 999 are reserved as IPC standard RLP numbers. Users of the system may enhance their computer libraries by tailoring the IPC RLP's (adding X, Y or Z), using numbers 001 to 099 or using four digit numbers to describe their custom standard land patterns. The letter ''W'' may be used to signify a special user pattern signifying that it is for wave soldered attachment application (i.e. RLP 102 defines as RLP 102W.)

Table 3-5 RLP Numbers

IPC-SM-782 Section	Component Type	Reserved Registered Land Pattern Numbers
8.1	Chip Resisters	100 to 129
8.2	Chip Capacitors	130 to 159
8.3	Inductors	160 to 179
8.4	Tantalum Capacitors	180 to 199
8.5	Metal Electrode Face Components (MELFS)	200 to 209
8.6	Small Outline Transistor (SOT) 23	210 to 214
8.7	Small Outline Transistor (SOT) 89	215 to 219
8.8	Small Outline Diode (SOD) 123	220 to 224
8.9	Small Outline Transistor (SOT) 143	225 to 229
8.10	Small Outline Transistor (SOT) 223	230 to 234
8.11	Modified Through-Hole Component (TO) 252	235 to 239
9.1	Small Outline Integrated Circuits (SOIC)	300 to 329
9.2	Small Outline Integrated Circuits (SSOIC)	330 to 359
9.3	Small Outline Package Integrated Circuit (SOPIC)	360 to 389
9.4	Thin Small Outline Package (TSOP)	390 to 419
9.5	Ceramic Flat Pack (CFP)	420 to 459
10.1	Small Outline with “J” Leads (SOJ)	480 to 529
11.1	Plastic Quad Flat Pack (PQFP)	530 to 549
11.2	Shrink Quad Flat Pack, Square (SQFP)	550 to 579
11.3	Shrink Quad Flat Pack, Rectangular (SQFP)	580 to 629
11.4	Ceramic Quad Flat Pack (CQFP)	630 to 649
12.1	Square Plastic Leaded Chip Carrier (PLCC)	700 to 719
12.2	Rectangular Plastic Leaded Chip Carrier (PLCC)	720 to 739
12.3	Leadless Ceramic Chip Carrier (LCC)	740 to 759
13.1	Modified Dual-In-Line Pin Components (DIP)	760 to 779
14.1	Ball Grid Arrays (BGA)	900 to 1069
14.2	Plastic Rectangular Ball Grid Arrays	1080 to 1082

3.3.4 Dimension Tailoring The concepts indicated in this section are reflected in the individual component/land pattern section of this document, sections 8.0 onward. In each instance, the tolerances used for C, F, or P are identified as well as the desired solder joints—‘‘J.’’ At times the component tolerances or component gauge requirements do not necessarily reflect the exact tolerance on a manufacturers data sheet. Usually this occurs when industry component specification ranges are so broad that they defy good surface mount design principles. When the action to modify the tolerance range is taken, the tolerance ‘‘C’’ is indicated with an asterisk (*).

In addition, solder joint formation has been considered as being transparent to the soldering process or equipment used for mass reflow solder processes. This technique facilitates a single land pattern for the computer aided design (CAD) system and allows the assembly to be processed by more than one type of assembly operation. As designs become more complex with denser component/land pattern geometries, the land patterns may have to be customized for specific components, and assembly processes, in order to make the entire process more robust and increase first pass defect-free assembly yields.

Users are encouraged to follow the equation principles defined in this section and in sections 8.0 onward. Maintaining the data in computer ‘‘spread sheet’’ formats will facilitate ease of modification to specific land pattern requirements for process yield improvements.*

Note: Electronic media (3.5 in disk) containing Lotus spreadsheets are available with instructions for use. They are identified as IPC-EM-782, ‘‘Land Pattern Data Analysis Spreadsheets for IPC-SM-782 Land Patterns.’’

3.4 Design for Producibility As part of the planning cycle of a product’s development, a concurrent engineering task group should be assembled to determine the criteria for each new design. During this planning phase, the product function and configuration is clearly defined and the

assembly process options outlined. Product size, component types, projected volume and the level of manufacturing equipment available may affect process options.

Following the substrate development, the assembly will be evaluated for many of the fundamentals necessary to insure a successful SMT process. Specific areas addressed during the evaluation will include:

- Land pattern concepts
- Component selection
- Mounting substrate design
- Need for testability
- Phototool generation

3.4.1 SMT Land Pattern The use of process proven land patterns for the solder attachment of surface mount devices will provide a benchmark to evaluate solder joint quality. Land pattern geometry and spacing utilized for each component type must accommodate all physical variables including size, material, lead contact design and plating.

3.4.2 Standard Component Selection Whenever possible, SMT devices should be selected from standard configurations. The standard components will be available from multiple sources and will usually be compatible with all assembly processes. For those devices developed to meet specific applications, standard packaging is often available. Select a package type that will be similar in materials and plating of standard device types when possible.

3.4.3 Circuit Substrate Development Design the circuit substrate to minimize excessive costs. Surface Mount Technology often pushes the leading edge of substrate technology. When estimating circuit density, allow for the greatest latitude in fabrication processes and tolerance variables. Before adopting extreme fine line and utilizing small plated holes, understand the cost impact, yield, and long-term reliability of the product.

3.4.4 Assembly Considerations Other factors that will impact manufacturing efficiency include component placement. Maintaining a consistent spacing between components, common orientation or direction of polarized devices will impact all steps of the assembly process. In addition, when common orientation is maintained, machine programming is simplified and component verification, solder inspection and repair are simplified.

3.4.5 Provide for Automated Test Testability of the assembled circuit substrate must be planned well in advance. If component level testing is necessary, one test probe contact area is required for each common node or net. Ideally, all probe contact pads are on one side. Provide grid-based test nodes to accommodate standard probes. Functional testing may also employ the same test nodes used for in-circuit test but will include all connectors that interface to cables and other assemblies.

3.4.6 Documentation for SMT Documentation used to fabricate the circuit substrate and assemble the product must be accurate and easy to understand. Details, specifications and notes will guide both the assembly processing and control the quality level of a product. Unique materials or special assembly instructions should be included on the face of the detail drawings or included in the documentation package.

3.5 Environmental Constraints

3.5.1 Handling Moisture Sensitive Components Several large plastic packages may be susceptible to absorbing moisture. The component manufacturer usually packages these parts with a desiccant, and provides instruction for use or maintaining those parts in a controlled storage environment. See J-STD-020 and J-STD-033 for instructions and proper handling and tesing procedures.

3.5.2 Usage Environments In Table 3–6, worst-case, but realistic, use environments for SM electronic assemblies are shown in nine major use categories. These use environment categories are listed in order of increasing severity, without consideration of the number of expected service years. It should be noted that the cyclic temperature range, delta T, is not the difference between the possible minimum, Tmin, and maximum, Tmax, operational temperature extremes; delta T is significantly less. It has to be recognized that these temperature extremes are possible only during different times of the year, and then only at significantly different geographic locations. The delta T values represent the temperature swings that typically can be expected during a given operating cycle.

Also given are the expected dwell durations at operating temperatures; they are significant because they determine the degree of completeness of the stress relaxation in the solder joints and thus determine the amount of cyclic fatigue damage relative to the maximum fatigue damage at complete stress relaxation. Table 3–6 also gives estimates of the number of operating cycles occurring during a service year. For some of the use categories, the use environments are described in terms of the sum of multiple use environments resulting from either significant seasonal dependence or broadly foreseeable use conditions; the military avionics category is subdivided into three subcategories reflecting differing use conditions due to type of aircraft, mission profile, geographic effects, etc. The space category contains two different environments for satellites in low-earth orbit (LEO) or geo-synchronous (stationary relative to earth) orbit (GEO).

3.5.3 Service Life The design service life, N, can vary significantly for the use categories in Table 3–6. The design service lives can range from less than one year, barely exceeding the warranty period for consumer products, to 20 years or more for telecommunications equipment and commercial aircraft. For some military applications the service life is measured in thousands of hours.

3.5.4 Acceptable Cumulative Failure Probability The acceptable cumulative failure probability, F(N), at the end of the design service life, N, can vary significantly depending on the specific purpose of the product, the complexity (number and mix of components) of the product, and perhaps the design service life. F(N) values could range from 1 ppm for products whose failure has critical consequences, e.g., cardiac pacemakers, to perhaps 10,000 ppm (1%) for consumer products or products which provide redundancy or ''limp-home capability'' in case of electrical system failure. (See IPC-SM-785).

Table 3–6 Worst-Case Environments and Appropriate Equivalent Accelerated Testing

	WORST-CASE USE ENVIRONMENT							ACCELERATED TESTING			
USE CATEGORY	Tmin °C	Tmax °C	$\Delta T^{(1)}$ °C	t_D hrs	Cycles/ year	Typical Years of Service	Approx. Accept. Failure Risk, %	Tmin °C	Tmax °C	$\Delta T^{(2)}$ °C	t_D min
1) CONSUMER	0	+60	35	12	365	1-3	1	+25	+100	75	15
2) COMPUTERS	+15	+60	20	2	1460	5	0.1	+25	+100	75	15
3) TELECOM	- 40	+85	35	12	365	7-20	0.01	0	+100	100	15
4) COMMERCIAL AIRCRAFT	-55	+95	20	12	365	20	0.001	0	+100	100	15
5) INDUSTRIAL & AUTOMOTIVE PASSENGER COMPARTMENT	-55	+95	20 &40 &60 &80	12 12 12 12	185 100 60 20	10	0.1	0	+100	100 & COLD(3)	15
6) MILITARY GROUND & SHIP	-55	+95	40 &60	12 12	100 265	10	0.1	0	+100	100 & COLD(3)	15
7) SPACE leo geo	-55	+95	3 to 100	1 12	8760 365	5-30	0.001	0	+100	100 & COLD(3)	15
8) MILITARY AVIONICS a b c	-55	+95	40 60 80 &20	2 2 2 1	365 365 365 365	10	0.01	0	+100	100 & COLD(3)	15
9) AUTOMOTIVE UNDER HOOD	-55	+125	60 &100 &140	1 1 2	1000 300 40	5	0.1	0	+100	100 & COLD(3) & LARGE $\Delta T^{(4)}$	15

& = in addition

1) ΔT represents the maximum temperature swing, but does not include power dissipation effects; for power dissipation calculate ΔT; power dissipation can make pure temperature cycling accelerated testing significantly inaccurate. It should be noted that the cyclic temperature range, ΔT, is not the difference between the possible minimum, T_{MIN}, and maximum, T_{MAX}, operational temperature extremes; ΔT is typically significantly less.

2) All accelerated test cycles shall have temperature ramps <20°C/minute and dwell times at temperature extremes shall be 15 minutes measured on the test boards. This will give ~24 test cycles/day.

3) The failure/damage mechanism for solder changes at lower temperatures; for assemblies seeing significant cold environment operations, additional ''COLD'' cycling, from perhaps –40 to 0°C, with dwell times long enough for temperature equilibration and for a number of cycles equal to the ''COLD'' °C operational cycles in actual use is recommended.

4) The failure/damage mechanism for solder is different for large cyclic temperature swings traversing the stress-to-strain –20 to +20°C transition region; for assemblies seeing such cycles in operation, additional appropriate ''LARGE ΔT'' testing with cycles similar in nature and number to actual use is recommended.

3.6 Design Rules During the component selection phase of a design, manufacturing engineering should be consulted regarding any components outside the scope of this document.

The printed board design principles are a statement of current test and manufacturing capabilities. Exceeding or changing these capabilities requires concurrence of all participants in the process including manufacturing, engineering and test technology.

Involving test and manufacturing early in the design helps to move a quality product quickly into production. Figure 3–7 shows a list of concurrent engineering team participants that should be involved.

3.6.1 Component Spacing

3.6.1.1 Component Considerations The land pattern design information discussed so far is important for reliability of surface mount assemblies. However, the designer should not lose sight of manufacturability, testability and repairability of SMT assemblies. A minimum interpackage spacing is required to satisfy all these manufacturing requirements. There is no limit on maximum interpackage spacing; the more the better. Some designs require that surface mount components are positioned as tightly as possible. Based on experience, the examples shown in Figure 3–8 meet manufacturability requirements.

The land to land spacing between adjacent components should be 1.25 mm [0.050 in] clear space all around the edges of printed boards if boards are tested off the connector or 2.5 mm [0.100 in] minimum if vacuum seal for testing is used. The requirements specified herein are recommended minimums excluding conductor geometry tolerances.

3.6.1.2 Wave Solder Component Orientation All polarized surface mount components should be placed in the same orientation, when possible. On any printed board assembly where the secondary side is to be wave soldered, the preferred orientation of devices on that side is described and shown in Figure 3–9. The preferred orientation is used in order to optimize the resulting solder joint quality as the assembly exits the solder wave.

- All passive components shall be parallel to each other.
- All SOICs shall be perpendicular to the long axis of passive components.
- The longer axis of SOICs and of passive components shall be perpendicular to each other.
- The long axis of passive components shall be perpendicular to the direction of travel of the board along the conveyer of the wave solder machine.

3.6.1.3 Component Placement Similar types of components should be aligned on the board in the same orientation for ease of component placement, inspection, and soldering. Also, similar component types should be grouped together whenever possible, with the net list or connectivity and circuit performance requirements ultimately driving the placements. See Figure 3-10. In memory boards, for example, all of the memory chips are placed in a clearly defined matrix with pin one orientation the same direction for all components. This is a good design practice to carry out on logic designs where there are many similar component types with different logic functions in each package. On the other hand, analog designs often require a large variety of component types making it understandably difficult to group similar components together. Regardless if

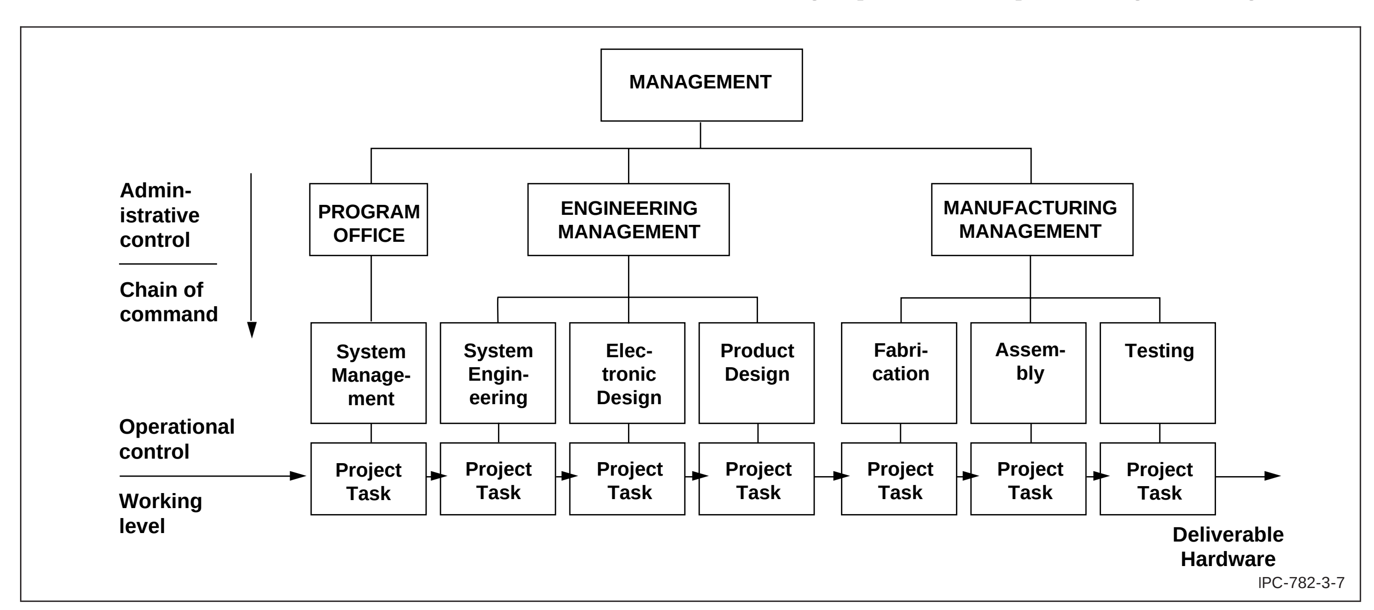


Figure 3–7 Simplified electronic development organization

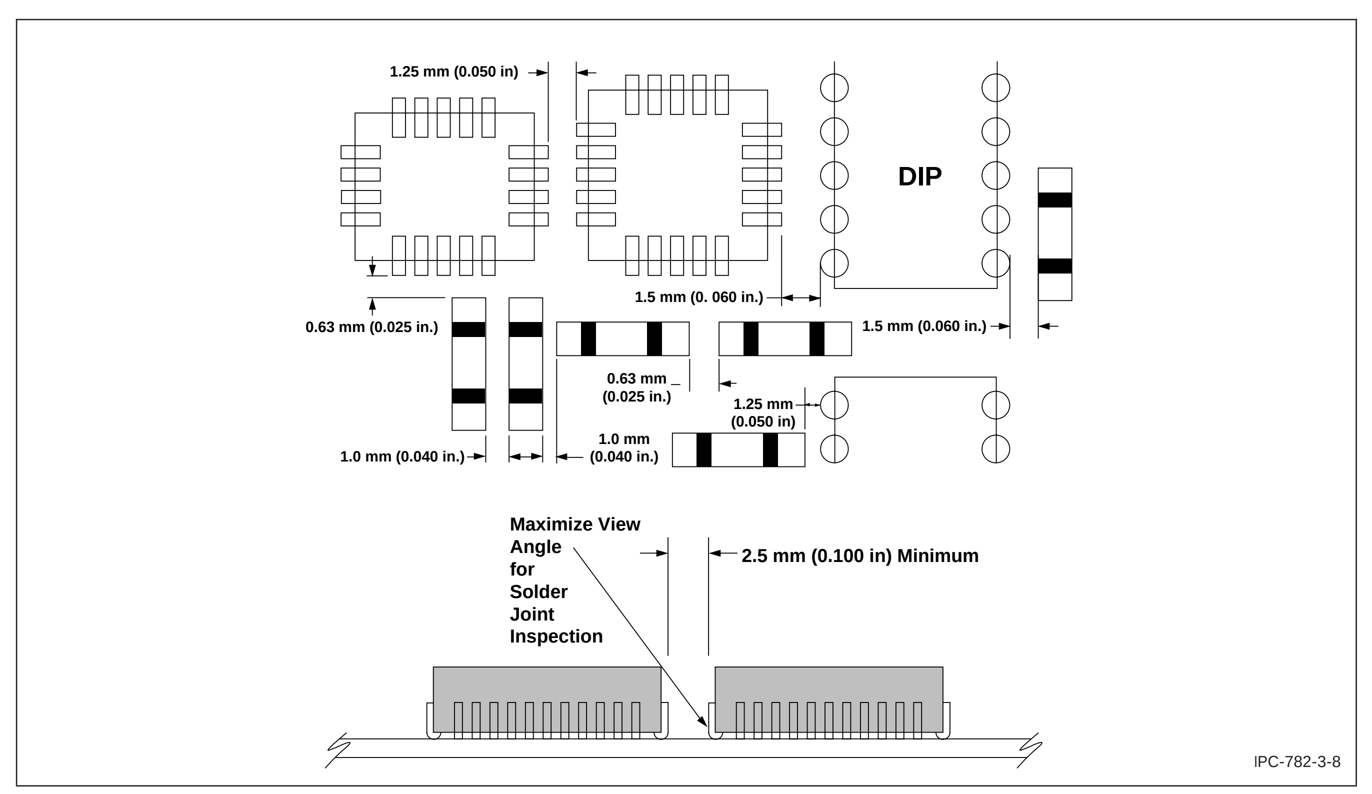


Figure 3–8 Recommended minimum land-to-land clearances

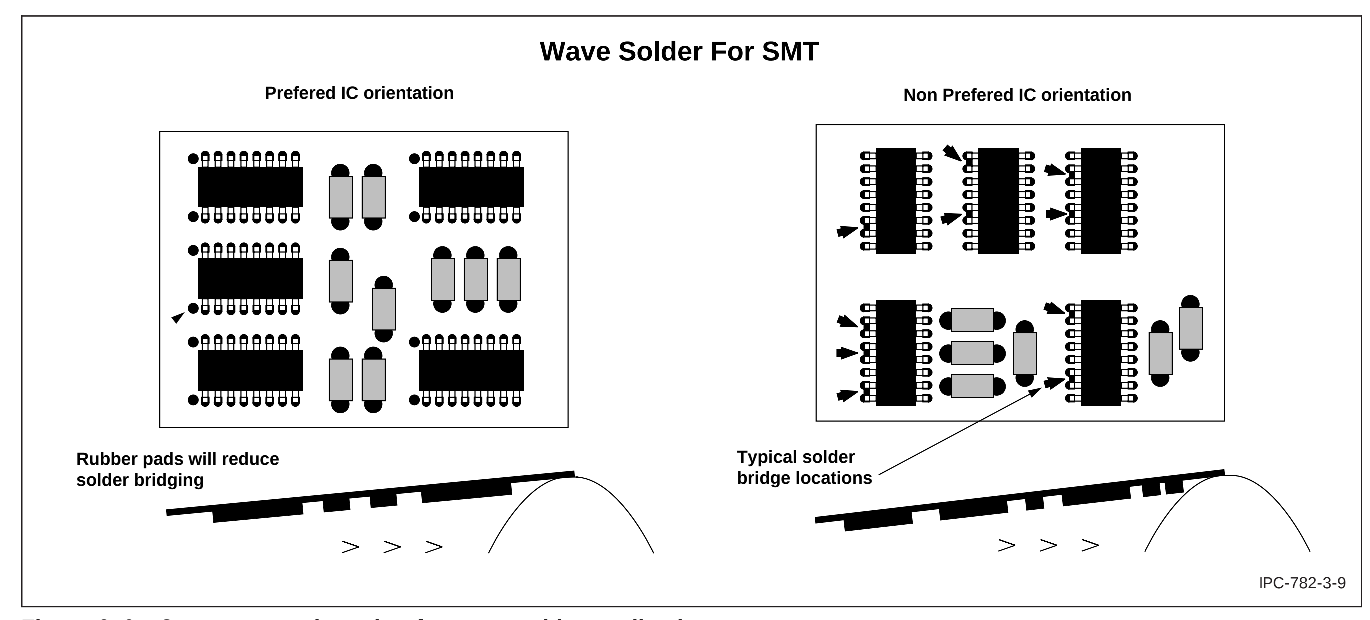


Figure 3–9 Component orientation for wave solder applications

the design is memory, general logic, or analog, it is recommended that all component orientations are such that pin one orientation is the same.

3.6.1.4 Grid-Based Component Placement SMT component placement and orientation is generally more difficult than THT printed boards for two reasons: higher component densities, and the ability to put components on both sides of the board. For THT designs, the component leads are on 2.54 mm [0.100 in] centers and, assuming 1.3 mm [0.065 in] lands, the spacing between lands would be 1.2 mm. In high density SMT designs, however, the spacing between lands is often less, down to 0.63 mm [0.025 in] and smaller. Grid based component placement (0.100 inch grid is standard with THT) is complicated by the large variety of land sizes associated with the SMT component packages now becoming available. Most SMT designs being done today have abandoned the 2.54 mm [0.100 in]

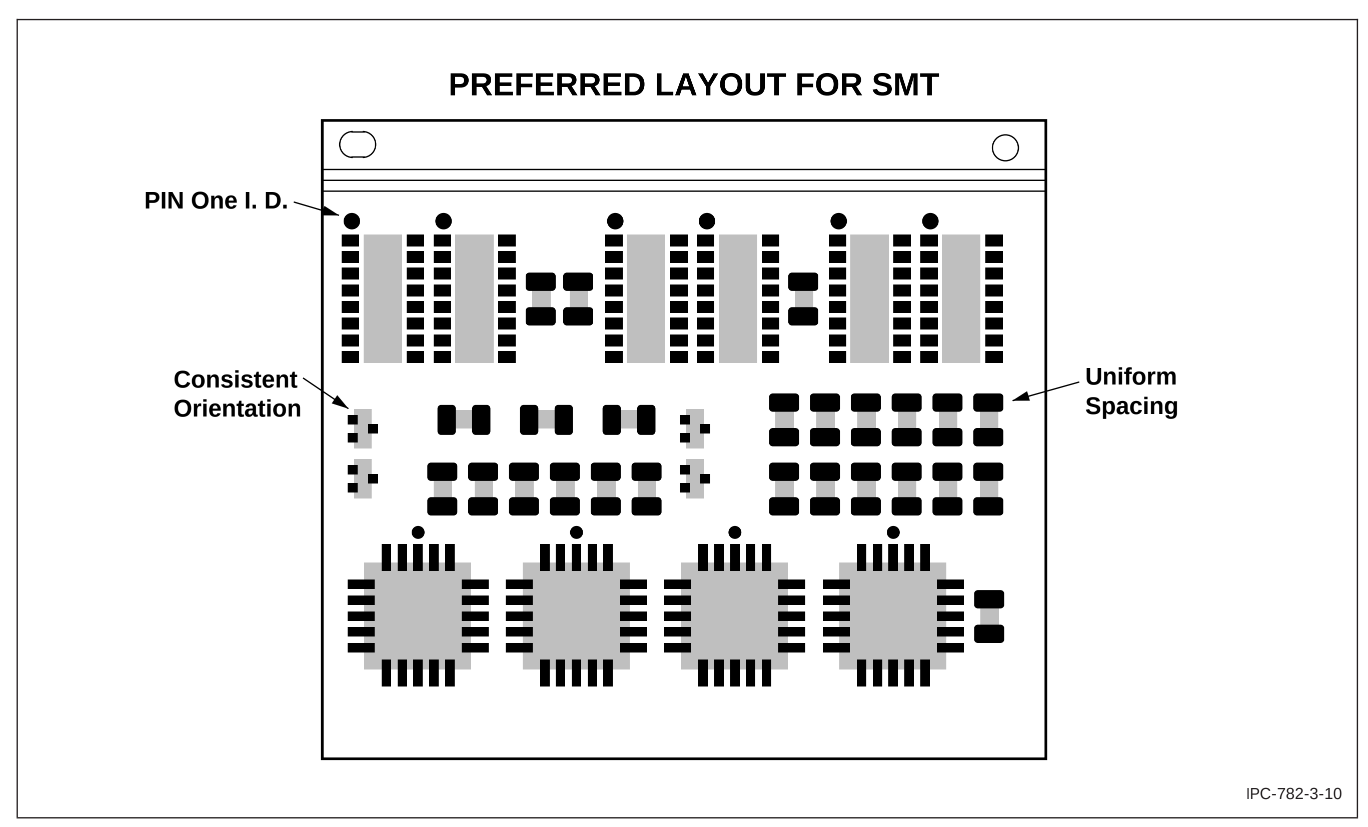


Figure 3–10 Alignment of similar components

grid based placement rules of the THT boards. This ultimately results in components being randomly placed, and vias being even more randomly placed across the board.

Two problems created by random component placement are a loss of uniform grid based test node accessibility and a loss of logical, predictable routing channels on all layers (possibly driving layer counts). In addition the accepted international grid identified in IPC-1902 states that for new designs the grid should be 0.5 mm, with a further subdivision being 0.05 mm. One solution to the problem is to build CAD libraries with all component lands connected to vias on 0.05 mm centers (or greater, based on design) to be used for testing, routing, and rework ports. Then when doing the component placement on the CAD system, simply place the components so that there is a minimum space of 0.5 mm between lands, then snap the vias of the component being placed out to the next 1.0 mm grid point. With this procedure, all of the components should have between 0.4 mm and 0.6 mm (or an average of 0.5 mm) spacing between the lands. From the assembly point of view, it is easier to process a PCB which has the component centroids on a 1.0 mm grid, with approximately equal spacing between all of the lands across the board in both directions.

3.6.1.5 Single vs Double Sided Boards The term single or double sided referred to one or two conductor layers on a printed board prior to the advent of Surface Mount. Now, however, the term single side refers to components mounted on one side (Type 1 assembly), and the term double refers to components mounted on both sides (Type 2 assembly) of the board. It has been observed that many SMT designers, especially novices, are too quick to place components on the secondary side of the PB, forcing the assembly process to be executed twice instead of once. Designers should concentrate on getting all components on the primary side of the board whenever possible without creating component spacing violations. This will result in a lower assembly cost. If double sided placement is definitely required, then grid-based placement, although more difficult, is even more crucial for accurate final component placement, circuit routability, and testability. Double sided boards using conventional SMT design rules often require double sided, or clamshell test fixtures that are 3 to 5 times the cost of single sided test fixtures. Grid based component placements have been known to improve nodal accessibility as well as eliminate the need for dual sided testing.

3.6.1.6 Solder Stencil Design The solder stencil is the primary vehicle by which solder paste is applied to the SMT printed board. With it, the exact location and volume of solder paste deposition is precisely controlled. The artwork for the stencil generally consists of the component mounting lands from the outer layers of the board with all other circuitry deleted. The openings in the stencil should be the same size as the lands on the board for all components. The printed board assembler may alter the stencil

opening size prior to manufacturing the stencil to change the volume of solder paste which is deposited on the lands.

3.6.1.7 Component Stand Off Height for Cleaning The minimum component stand off height for cleaning is based on the distance across the diagonal of the component. This dimension implies a component surface area that may trap contamination if care is not exercised. Table 3–7 shows the relationship for recommended component standoff distances.

If the minimum stand off cannot be achieved, proper cleaning under the component may not be possible. In this case it is recommended that a no clean flux be used.

3.6.1.8 Fiducial Marks A Fiducial Mark is a printed artwork feature which is created in the same process as the circuit artwork. The fiducial and a circuit pattern artwork must be etched in the same step.

Table 3–7 Component Stand Off

Component Diagonal	Component Surface Area	Component Stand Off
< = 50 mm	< = 2500 mm^2	> = 0.5 mm
< = 25 mm	< = 625 mm^2	> = 0.3 mm
< = 12 mm	< = 144 mm^2	> = 0.2 mm
< = 6 mm	< = 36 mm^2	> = 0.1 mm
< = 3 mm	< = 9 mm^2	> = 0.05 mm

The Fiducial Marks provide common measurable points for all steps in the assembly process. This allows each piece of equipment used for assembly to accurately locate the circuit pattern. There are two types of Fiducial Marks. These are:

A. Global Fiducials

Fiducial marks used to locate the position of all circuit features on an individual board. When a multi image circuit is processed in panel form, the Global Fiducials are referred to as Panel Fiducials when present for the panel. (See Figures 3–11/3–12.)

B. Local Fiducials

Fiducial marks used to locate the position of an individual component requiring more precise placement. (See Figure 3–11.)

A minimum of two global fiducial marks is required for correction of translational offsets (x and y position) and rotational offsets (theta position). These should be located diagonally opposed and as far apart as possible on the circuit or panel.

A minimum of three fiducial marks is required for correction of non linear distortions (scaling, stretch and twist).

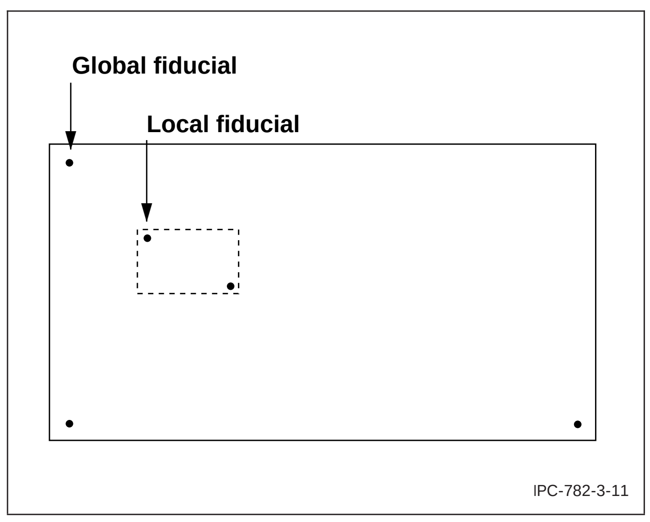


Figure 3–11 Local/global fiducials

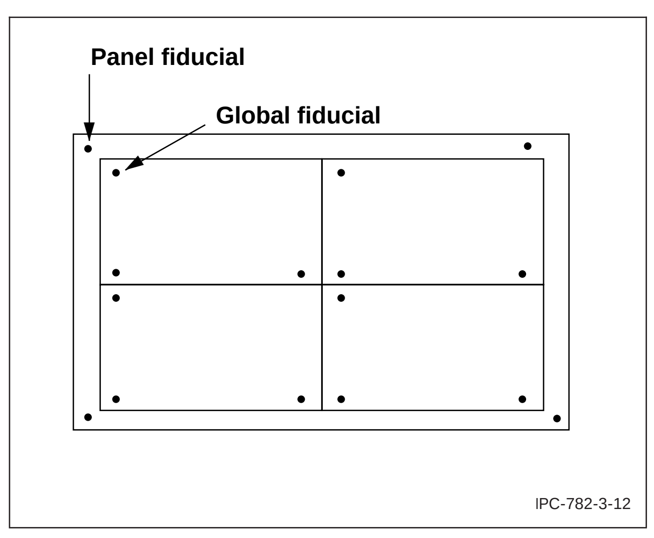


Figure 3-12 Panel/global fiducials

These should be located in a triangular position as far apart as possible on the circuit or panel.

A minimum of two local fiducial marks are required for correction of translational offsets (x and y position) and rotational offsets (theta position). This can be two marks located diagonally opposed within the perimeter of the land pattern.

If space is limited, a minimum of one local fiducial mark may be used to correct translational offsets (x and y position). The single fiducial should be located inside the perimeter of the land pattern with a preference for the center.

The minimum size for local, global or panel fiducials is 1.0 mm. Some companies have chosen a larger fiducial (up to 1.5 mm) for panel fiducials. It is a good practice to keep all fiducials the same size.

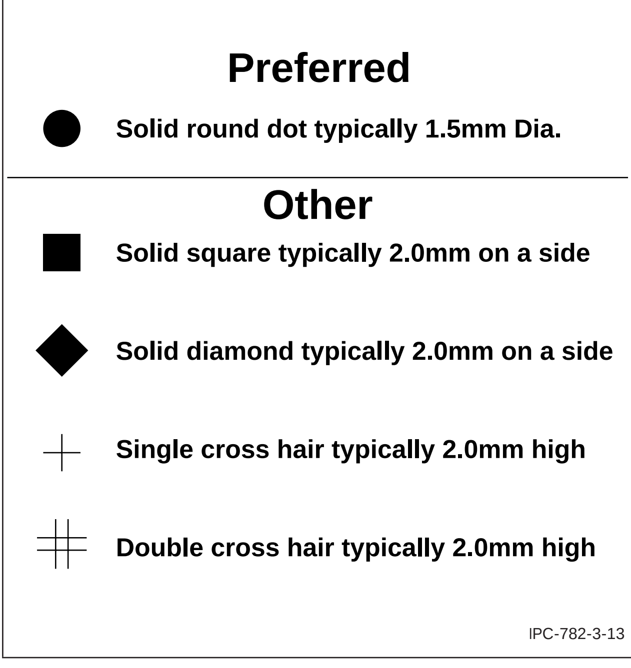


Figure 3-13 Fiducial types for vision systems

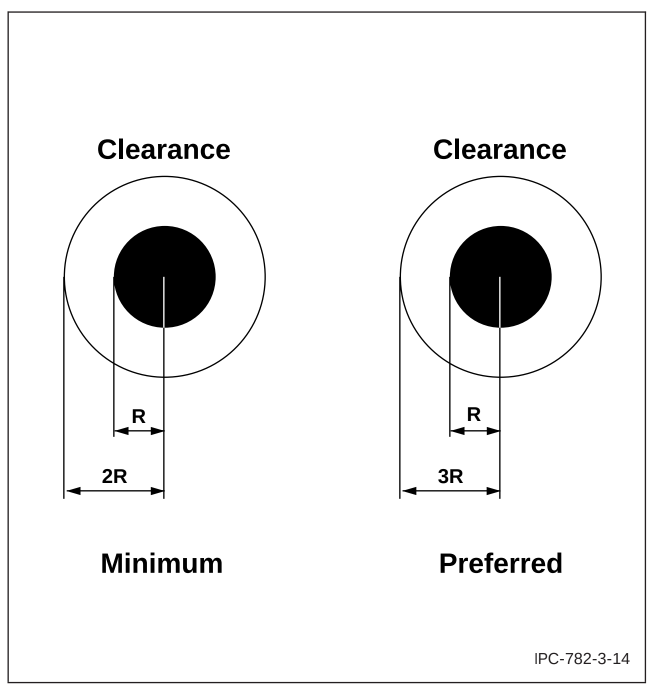


Figure 3-14 Fiducial clearance requirements

3.6.1.9 Fiducial Mark Design Specifications The Surface Mount Equipment Manufacturers Association (SMEMA) has standardized on the design rules for fiducials. These rules are supported by the IPC and consist of:

A. Shape

The optimum fiducial mark is a solid filled circle. See Figure 3–13.

B. Size

The minimum diameter of the fiducial mark is 1 mm [0.040 in]. The maximum diameter of the mark is 3 mm [0.120 in]. Fiducial marks should not vary in size on the same PB more than 25 microns [0.001 in].

C. Clearance

A clear area devoid of any other circuit features or markings shall exist around the fiducial mark. The size of the clear area shall be equal to the radius of the mark. A preferred clearance around the mark is equal to the mark diameter. (See Figure 3–14)

D. Material

The fiducial may be bare copper, bare copper protected by a clear anti oxidation coating, nickel or tin plated, or solder coated (hot air leveled).

The preferred thickness of plating or solder coating is 0.005 mm to 0.010 mm [0.0002 to 0.0004 in]. Solder coating should never exceed 0.025 mm [0.001 in].

If solder mask is used, it should not cover the fiducial or the clearance area. It should be noted that oxidation of a fiducial mark's surface may degrade its readability.

E. Flatness

The flatness of the surface of the fiducial mark should be within 0.015 mm [0.0006 in].

F. Edge Clearance

The fiducial shall be located no closer to the PB edge than the sum of 4.75 mm [0.187 in] (SMEMA Standard Transport Clearance) and the minimum fiducial clearance required.

G. Contrast

Best performance is achieved when a consistent high contrast is present between the fiducial mark and the PB base material.

It is good design practice to locate global or panel fiducials in a three point grid based datum system as shown in Figure 3–15. The first fiducial is located at the 0,0 location. The second and third fiducials are located in the X and Y directions from 0,0 in the positive quadrant. The global fiducials should be located on the top and bottom layers of all printed boards that contain Surface Mount as well as Through Hole components since even Through Hole assembly systems are beginning to utilize vision alignment systems.

All Fine Pitch components should have two local fiducials system designed into the component land pattern to insure that enough fiducials are available every time the component is placed, removed and/or replaced on the board. All fiducials should have a soldermask opening large enough to keep the optical target absolutely free of soldermask. If

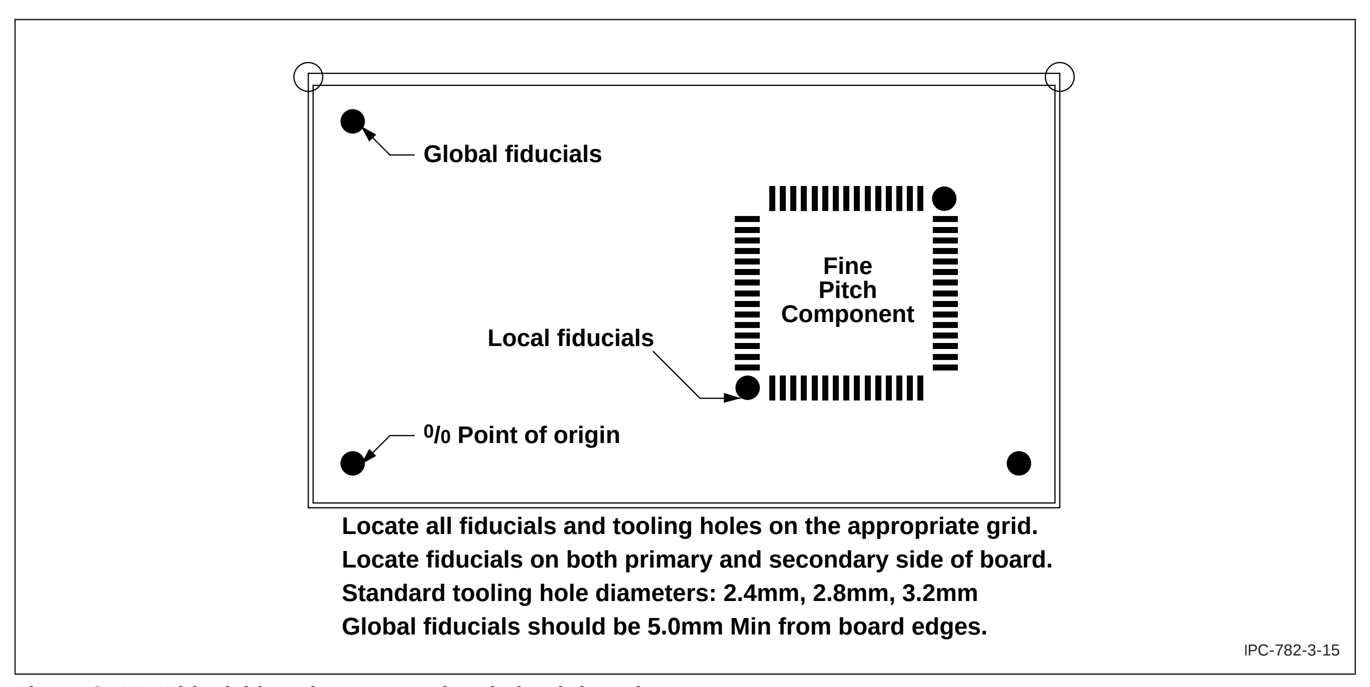


Figure 3–15 Fiducial locations on a printed circuit board

soldermask should get onto the optical target, some vision alignment systems may be rendered useless due to insufficient contrast at the target site.

The internal layer background for all fiducials must be the same. That is, if solid copper planes are retained under fiducials in the layer below the surface layer, all fiducials must have copper retained. If copper is clear under one fiducial, all must be clear.

3.6.2 Conductors

3.6.2.1 Conductor Width & Clearances Increased component density on SMT designs has mandated the use of thinner conductor density and clearance between conductors with increased PB layer counts requiring the use of more vias to make the necessary connections between the additional layers. Figure 3–16 shows the effects of SMT and Fine Pitch Technology (FPT) on printed board geometries.

Conductor width/clearances of 0.15 mm [0.006 in] have become commonplace today, and have basically replaced the 0.3 mm [0.012 in] line/ space as a commonly used geometry (see Figure 3–17). As more fine pitch (including Tape Automated Bonding) devices are used on printed boards, the 0.125 mm [0.005 in] geometry may be used in more SMT boards to reduce layer counts. Figure 3–18

GEOMETRY	2.54mm Pitch	1.25mm Pitch	0.63mm Pitch
PIN COUNTS	8 TO 64	8 TO 124	84 TO 244
PLACEMENT TOLERANCE	.25mm	0.125mm	0.05mm
CONDUCTORS/CLEARANCE	.3mm	0.15mm	0.125mm
LANDS	1.5mm	0.75mm	0.63mm
HOLES	1.0mm	0.4mm	0.40mm
ANNULAR RING	.25mm	0.2mm	0.125mm

IPC-782-3-16

Figure 3–16 Packaging and geometries

ROUTING GRIDS	MINIMUM CONDUCTORS/CLEARANCE	MANUFACTURING ALLOWANCE
.63mm	0.3/0.2mm	0.1mm
0.5mm	0.2/0.2mm	0.1mm
0.4mm	0.2/0.15mm	0.05mm
0.3mm	0.15/0.1mm	0.05mm
0.25mm	0.10/0.10mm	0.05mm

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Figure 3–17 Surface mount conductor widths/clearances vs. routing grids

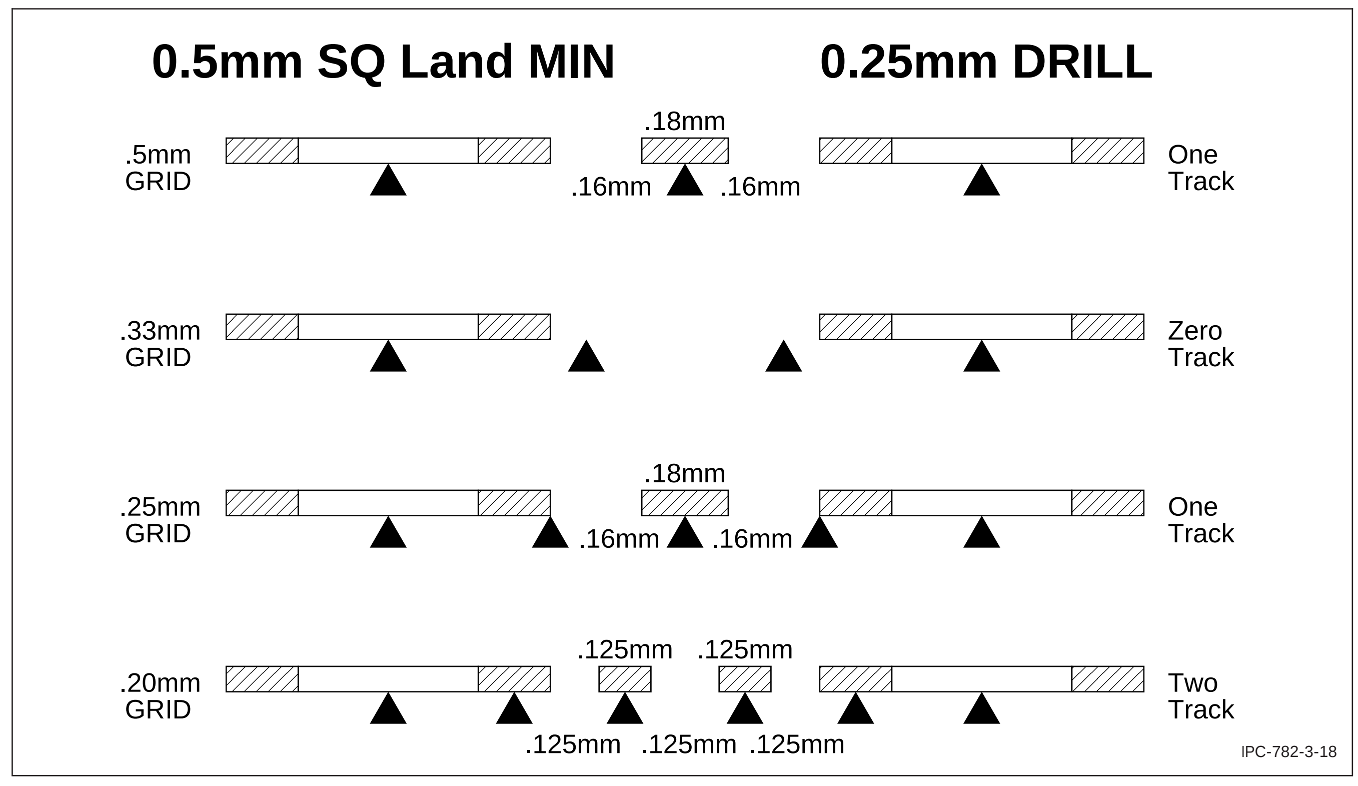


Figure 3–18 Section view of multilayer board with vias on 1.0 mm [0.040 in] centers

shows a grid routing analysis with vias on 1.0 mm [0.050 in] centers. On the left side are listed the routing grids with the actual routing channels denoted by solid triangular points. It can be seen that with SMT geometry of vias placed on 1.0 mm [0.040 in] centers, there is one routing channel between lands using a 0.3 mm [0.012 in] grid with 0.15 mm [0.006 in] conductor width/clearances. The bottom routing grid of 0.25 mm [0.010 in] with 0.125 mm [0.005 in] has two routing channels between vias.

3.6.2.2 Surface Conductors Wide conductors connecting to a land area can act as a solder thief by drawing solder away from the land and down the conductor. Furthermore, if the conductor goes to a via which is connected to an inner layer power or ground plane, the wide conductor may act as a heat sink and draw heat away from the land/lead area during reflow solder resulting in a cold solder joint.

A. Narrow the conductor as it enters the land area. Maximum conductor width should be 0.25 mm [0.010 in] (see Figure 3–19). The minimum conductor length should be 0.50 mm [0.020 in]. This neckdown provides an effective solder restriction, and may eliminate the

need to use a soldermask to prevent the migration of solder away from the component land.

B. Routing conductors into the lands as shown in Figures 3–20, 3–21 may restrict discrete component movement during reflow soldering. In the case of active IC's this routing geometry will allow the designer to use the same library shape for surface routing or pad cap (no surface routing) printed board configuration. Additionally, using this generic library shape allows ease of switching between the two configurations midstream in the design process without changing or editing component libraries. In either case, 100% test node access is retained. If wider conductors are required, the via land size may be decreased accordingly to allow sufficient spacing between the conductor and the land.

C. Use solder mask over bare copper (SMOBC) or copper that has had the solder plating selectively removed. The solder mask and bare copper provide an effective barrier to solder migration. This may provide sufficient protection even if options A and B are not possible.

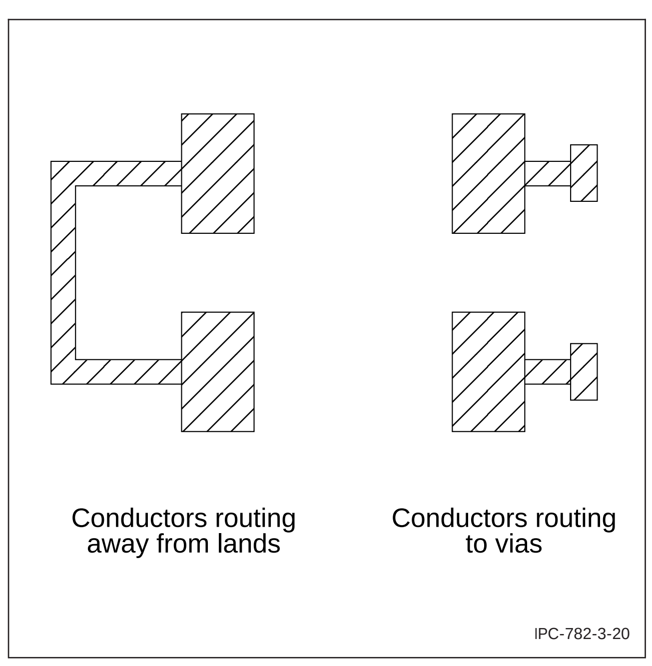


Figure 3–20 Conductor routing

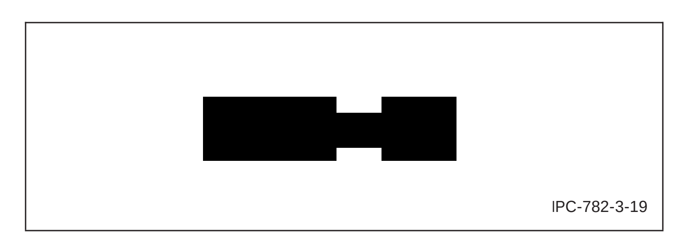


Figure 3–19 Narrowed conductor

3.6.2.3 Inner Layer Conductors The use of 0.2 mm [0.008 in] conductors and clearance often drives layer counts up because there is no routing channel available between vias on 1.27 mm [0.050 in] centers. It is for this reason that there is an increased usage of the conductors on internal layers at or less than 0.15 mm [0.006 in] for SMT designs, and 0.125 mm [0.005 in] conductors and clearances for designs with heavy usage of FPT. Figure 3–22 and 3–23 show the number of routing channels available between lands using the 0.15 and 0.125 mm [0.006 and 0.005 in] geometries. Since conductor width control is much more difficult to maintain on outer layers of the PB, it is better to keep the small geometries on the inner layers of a multilayer printed board. Doing so may reduce the need for soldermask and dramatically improve printed board fabrication yields. Generally, the option of using smaller geometries is driven by the need to reduce layer counts. Decreasing layer counts may reduce the overall board thickness and improve the aspect ratio for small hole drilling.

3.6.3 Via Location Guidelines

3.6.3.1 Via Holes Size of the via holes should be selected based upon the printed board thickness vs. hole diameter or aspect ratio limits as defined by printed board fabricator. In addition, specific via lands and holes can be accessed for automatic in-circuit test (ICT). See 5.3.1. Figure 3–24 shows the land pattern-to-via relationships.

3.6.3.2 Vias and Land Pattern Separation Vias are plated-through holes for example 0.63 mm to 1.0 mm [0.025 to 0.040 in] diameter lands. They must be located away from the component lands to prevent solder migration off the component land during reflow soldering. This migration will cause insufficient solder fillets on components. (Solder drain) The solder migration can be restricted by providing a narrow bridge between the land area and the via or prevented by using the soldermask over bare copper circuitry. (See Figures 3–19 and 3–20.)

The relationship for mounting land and via locations should consider the conductor routing requirements. Figure 3–25 provides several examples of via positioning concepts.

Specifying tented or filled vias will also reduce solder migration on assemblies manufactured with a solder reflow process. Filled or tented vias also take care of potential flux entrapment problems under components and are highly desirable for attaining good vacuum seal during in-circuit bed-of-nails testing. Tenting is done with a dry film type of soldermask, or the via may be filled with a resin prior to liquid soldermask application.

3.6.3.3 Vias Under Components If the assembly is to be wave soldered, via holes underneath zero clearance components on the primary side should be avoided on boards unless tented with soldermask. During wave soldering of the assembly, flux may potentially become trapped under

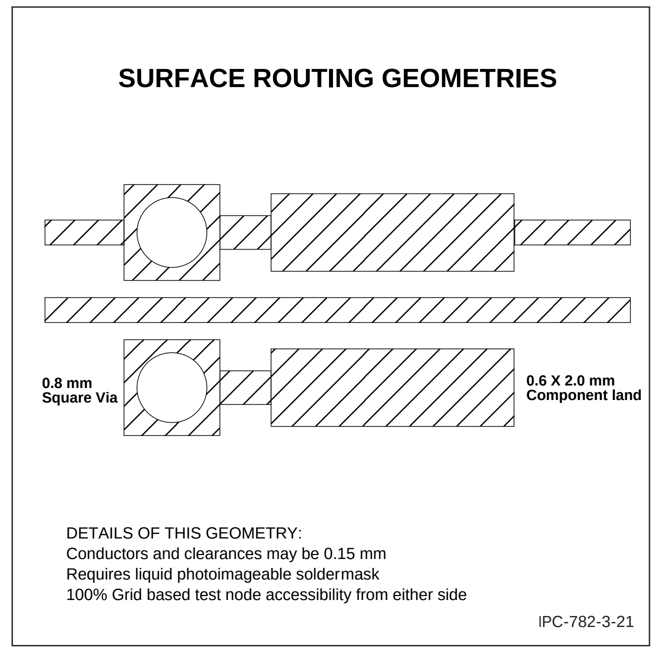


Figure 3-21 Surface routing geometries

zero clearance devices. Via holes may be located underneath zero clearance surface mount packages in full surface mount assemblies that will not be wave soldered. See Figure 3–26.

3.6.3.4 Vias as Test Points Via holes are used to connect surface mounted component lands to conductor layers. They may also be used as test targets for bed-of-nails type probes and/or rework ports. Via holes may be tented if they are not required for node testing or rework. When a via is used as a test point it is required that the location of a test land be defined. See Section 5.0.

3.6.4 Standard Fabrication Allowances Manufacturing tolerances or Standard Fabrication Allowances (SFA) exist in all PB fabrication shops. Virtually every registration or alignment operation that is performed has some potential for misregistration. There are approximately 42 basic steps in fabricating a multilayer PB, several of which involve operations that require precision in location. They are as follows: artwork generation, artwork tooling hole locations, core material tooling hole size, inner layer image printing operation, laminating fixture tooling pin locations, material shrinkage during lamination, drill tooling pin location, drill x/y table tolerances, drill spindle tolerances, drill wander, outer layer imaging, to name a few. The SFA considers all of the tolerances of all the steps mentioned above. If all of the equipment in a fabrication shop is old and worn the SFA could be as high as 0.3 mm, whereas, a manufacturer with new, precise equipment may have an SFA of 0.2 mm. An industry average SFA of 0.4 mm may be used. The tolerance varies according to the printed board maximum diagonal dimension and must be included in the land size calculations. The fabricator should be consulted prior to beginning a design to determine his SFA. With this number, the designer can proceed accordingly, preventing tolerances from stacking up and creating yield and/or production problems. (See IPC-2221.)

3.6.4.1 Manufacturing Characteristics Figure 3–27 shows the various characteristics of conductor geometry. End product drawings and specifications should specify only minimums for conductor width and spacing. Tolerance with plating of ±0.03 mm [±0.001 in] can be achieved under special conditions. Artwork allowances that should be incorporated into a design are shown in Table 3–8.

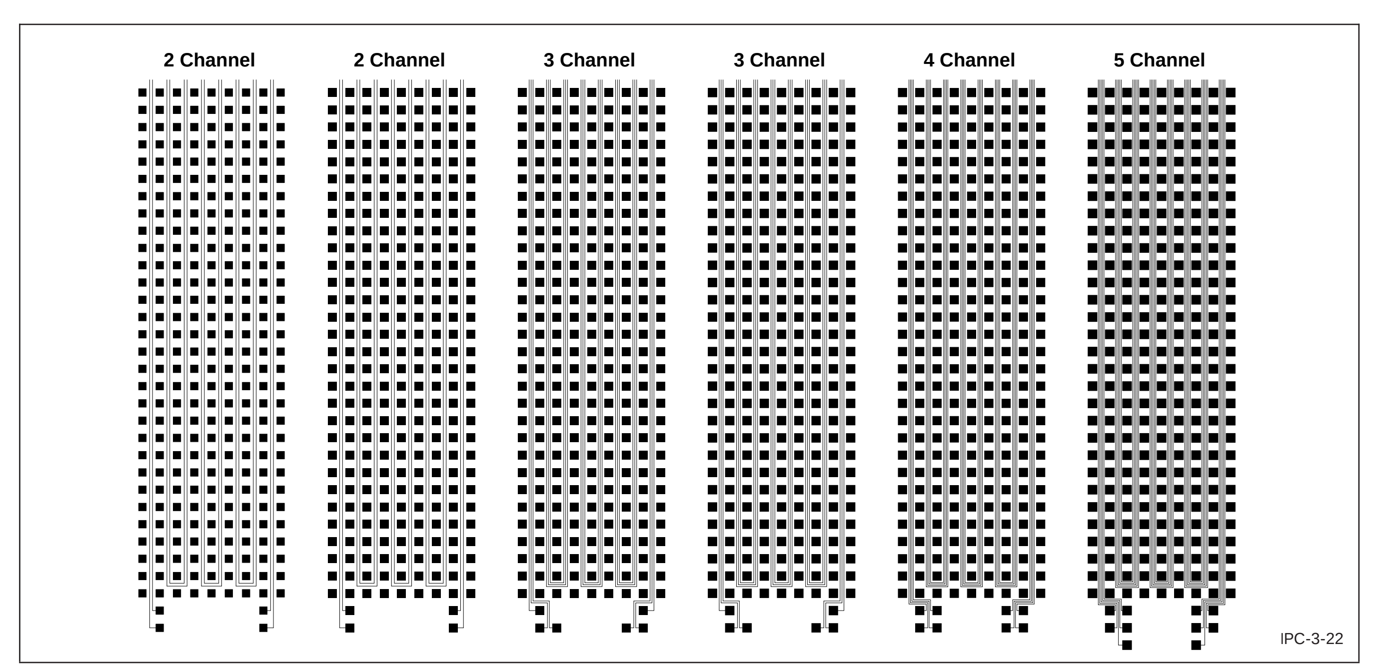


Figure 3–22 Conductor routing capability test pattern

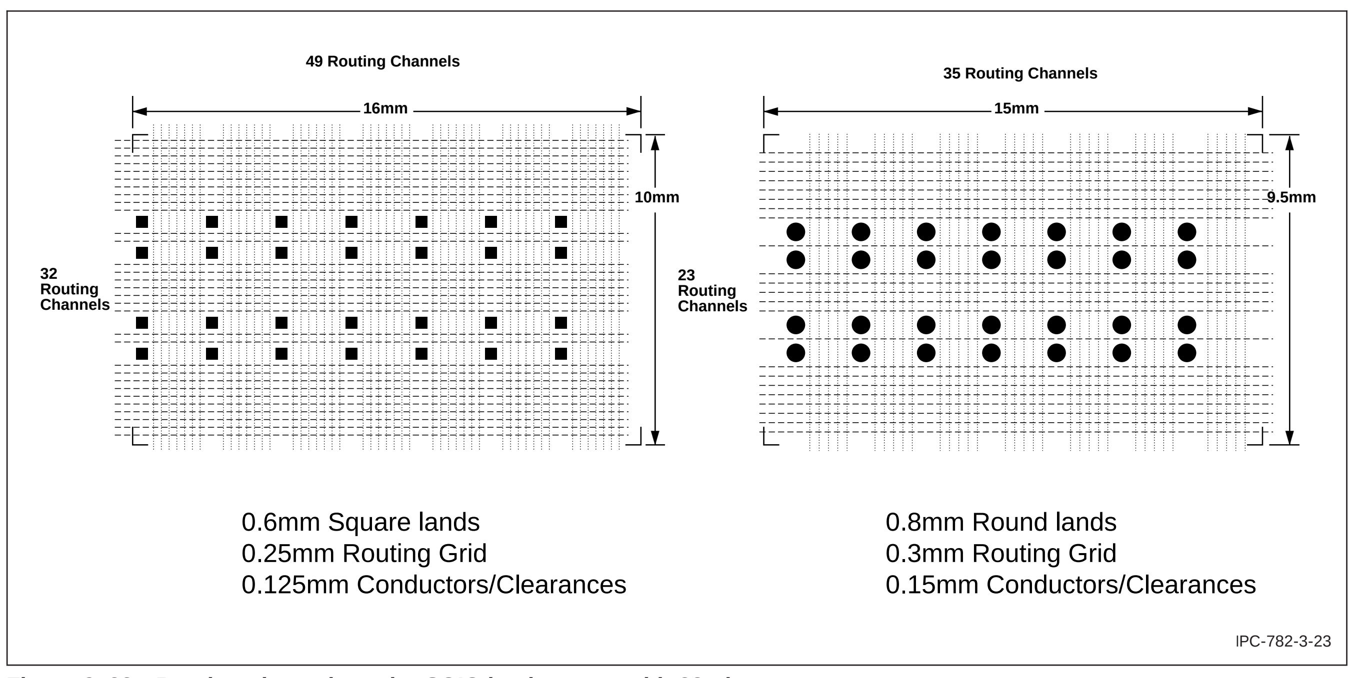


Figure 3–23 Routing channels under SOIC land pattern with 28 pins

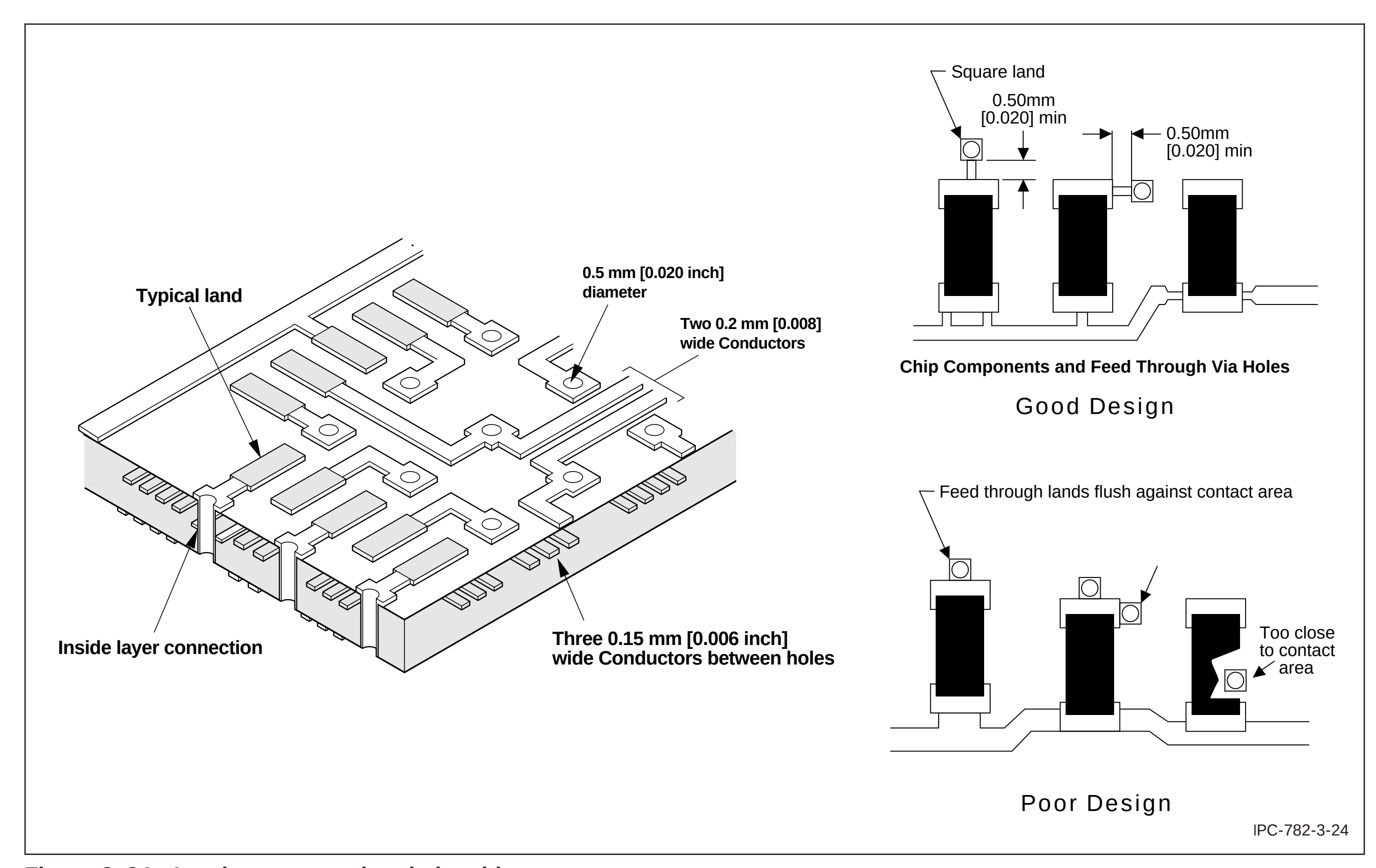


Figure 3–24 Land pattern to via relationships

Spacing requirements are usually the inverse of the tolerances shown for conductors in Table 3–9. For additional information see IPC-D-310, Artwork Generation and Measurement Techniques.

3.6.4.2 Conductor Width and Spacing Tolerances The presentation in Table 3–9 represents process tolerances that can be expected with normal processing. (Specific process

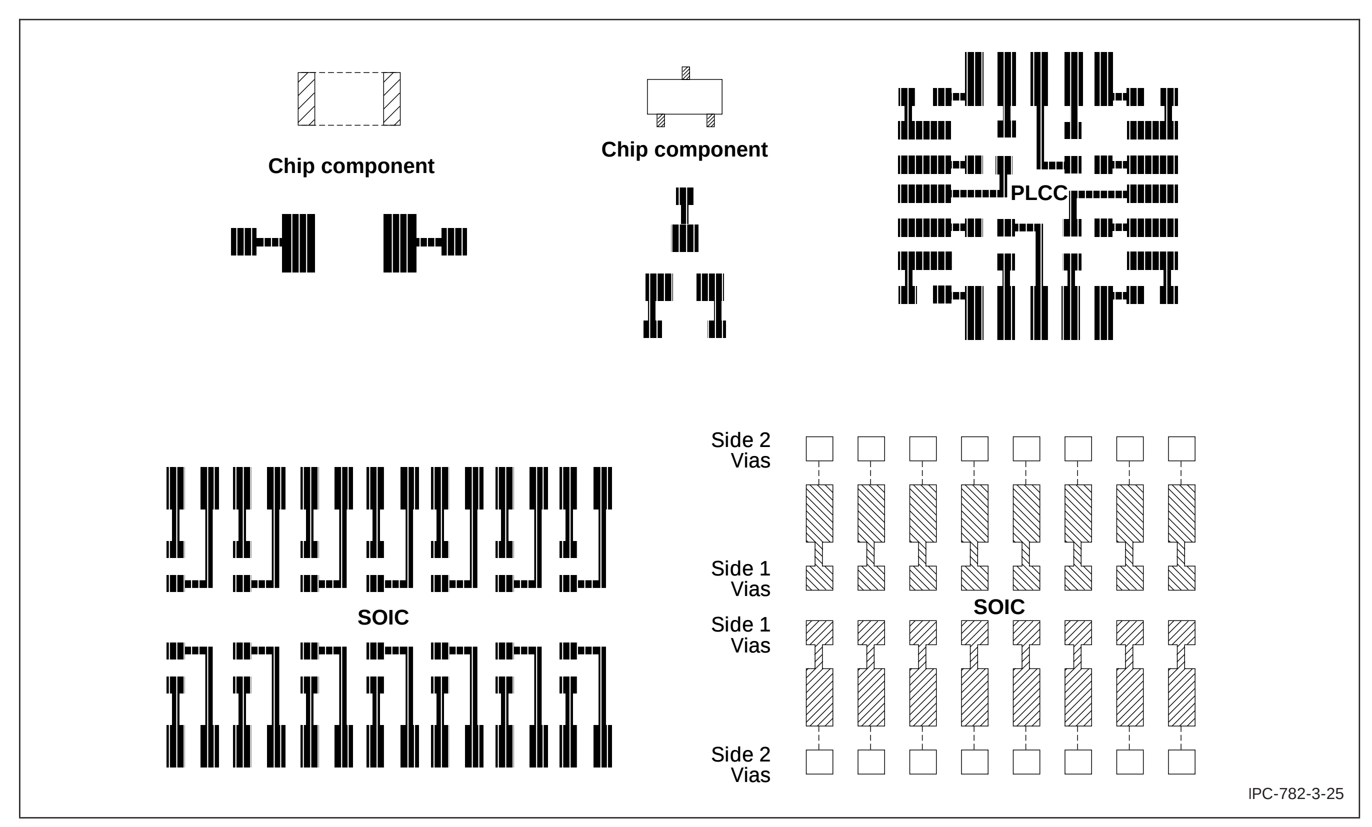


Figure 3–25 Examples of via positioning concepts

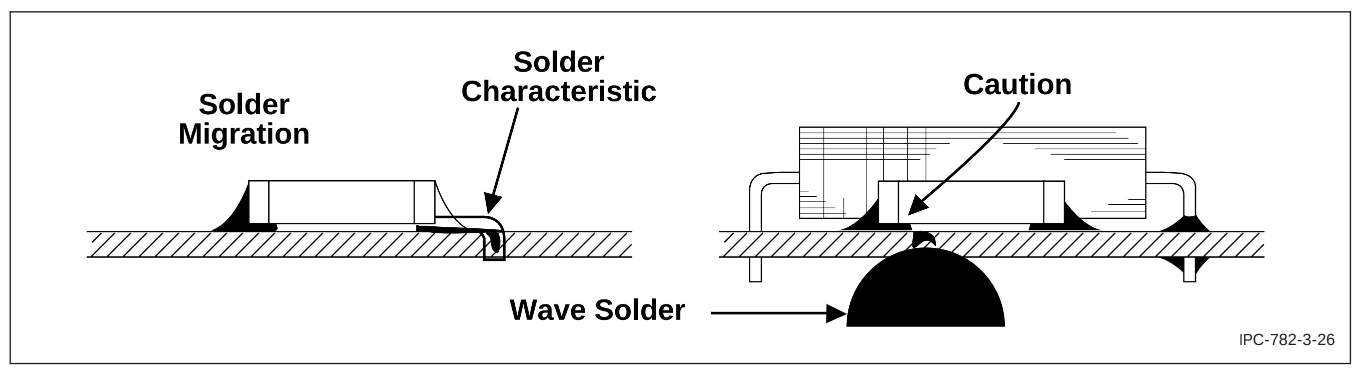


Figure 3–26 Vias under components

tolerances should be discussed with the board manufacturer.) The tolerances are based on copper thickness up to and including one ounce copper. For each ounce of additional copper, an additional 0.03 mm [0.001 in] variation per conductor edge can be expected.

3.6.4.3 Conductive Pattern Feature Location Tolerance The presentation in Table 3–10 is for the tolerance to be applied to the nominal dimension chosen for the location of the lands, connector contacts and conductors in relation tothe datums. This tolerance includes tolerances for master pattern accuracy, material movement, layer registration and fixturing.

3.6.4.4 Annular Ring Control The annular ring is defined as the amount of land that is remaining after a hole is drilled through it. With high density SMT designs, maintaining minimum annular requirements has emerged as one of the most difficult parts of multilayer PB fabrication in terms of producibility. Perfect registration will maximize the annular ring all around the drilled hole. Using a 0.8 mm [0.030 in] land with a 0.5 mm [0.020 in] drill will result in a 0.15 mm [0.006 in] annular ring under perfect registration conditions. If misregistration of 0.15 mm [0.006 in] occurs in any direction, the result will be a 0.3 mm [0.010 in] annular ring on one side of the pad, and no annular ring on the other side. If misregistration is greater than 0.15 mm [0.006 in], i.e., 0.2 mm [0.008 in], then the drill will actually break out of the land. If the breakout is in the direction where the conductor connects to the land, the drill will effectively disconnect the conductor from the land. The net

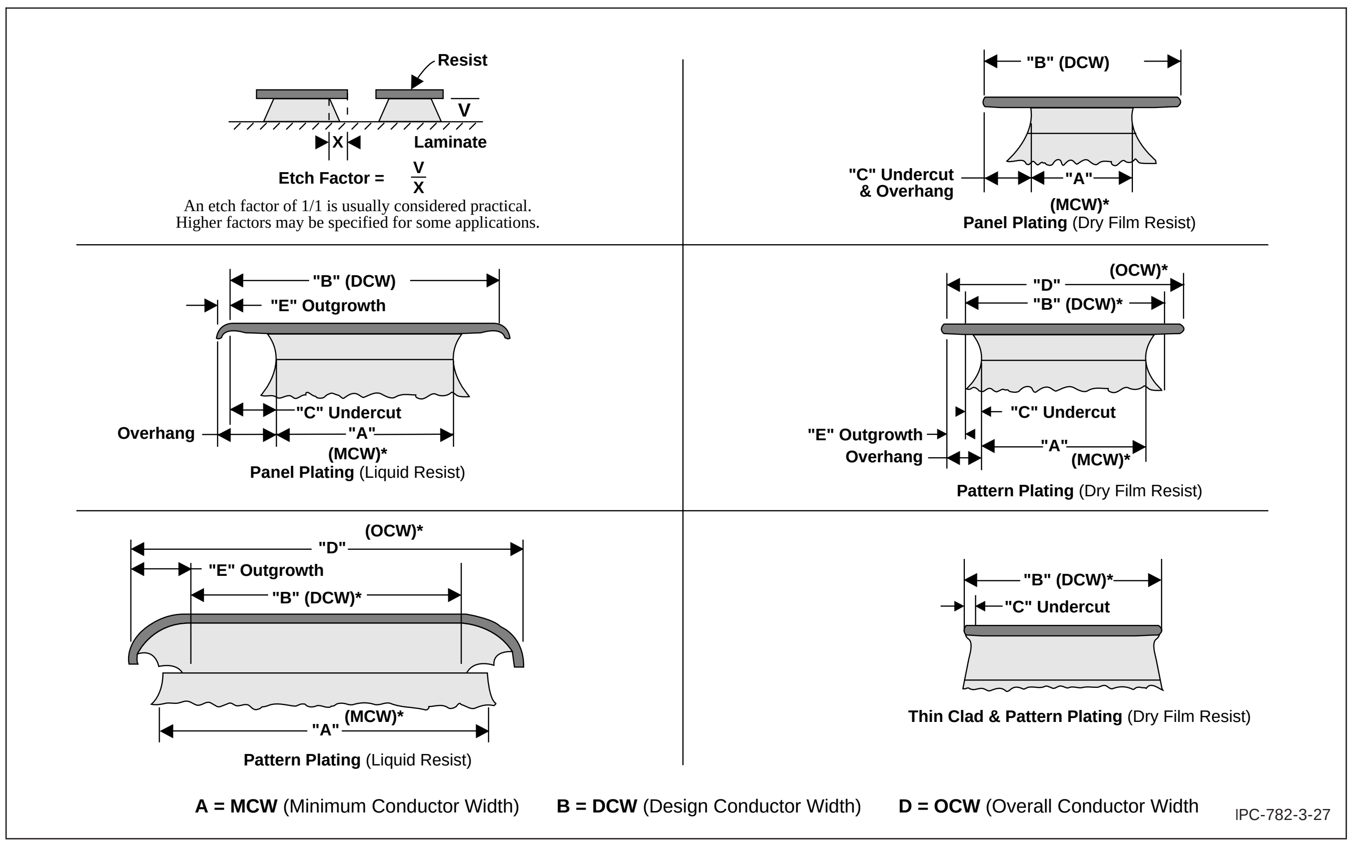


Figure 3–27 Conductor characteristics

Table 3–8 Typical Values to Be Added or Subtracted to Nominal Production to Achieve Desired Nominal Conductor Width

	1/2 Oz. Copper						1 Oz. Copper						2 Oz.Copper					
	Panel			Pattern			Panel			Pattern			Panel			Pattern		
Description	Screen	Liquid Photo	Dry Film Photo	Screen	Liquid Photo	Dry Film Photo	Screen	Liquid Photo	Dry Film Photo	Screen	Liquid Photo	Dry Film Photo	Screen	Liquid Photo	Dry Film Photo	Screen	Liquid Photo	Dry Film Photo
Subtractive Method Simple Etch	+25µm [+0.0010]	+25µm [+0.0010]	+25µm [+0.0010]	—	—	—	+38µ [+0.0015]	+38µm [+0.0015]	+38µm [+0.0015]	—	—	—	+63µm [+0.0025]	+63µm [+0.0025]	+63µm [+0.0025]	—	—	—
Bare Copper [PTH]	+38µ [+0.0015]	+38µm [+0.0015]	+50µm [+0.0020]	-25µ [-0.0010]	-25µm [-0.0010]	-25µm [-0.0010]	+50µm [+0.0020]	+50µm [+0.0020]	+63µm [+00025]	0	0	+50µm [+0.0020]	+76µm [+0.0030]	+76µm [+0.0030]	+89µm [+0.0035]	+38µm [+0.0015]	+38µm [+0.0015]	+89µm [+0.0035]
Tin-Lead [PTH]	+38µm [+0.0015]	+38µm [+0.0015]	+50µm [+0.0020]	-25µm [-0.0010]	-25µm [-0.0010]	+25µm [+0.0010]	+50µm [+0.0020]	+50µm [+0.0020]	+63µm [+0.0025]	0	0	+50µm [+0.0020]	+76µm [+0.0030]	+76µm [+0.0030]	+89µm [+0.0035]	+38µm [+0.0015]	+38µm [+0.0015]	+89µm [+0.0035]
Gold Nickel [PTH]	+38µm [+0.0015]	+38µm [+0.0015]	+50µm]+0.0020]	-25µm [-0.0010]	-25µm [-0.0010]	+25µm [+0.0010]	+50µm [+0.0020]	+50µm [+0.0020]	+63µm [+0.0025]	0	0	+50µm [+0.0020]	+76µm [+0.0030]	+76µm [+0.0030]	+89µm [+0.0035]	+38µm [+0.0015]	+38µm [+0.0015]	+89µm [+0.0015]
	For Deposited Copper Thickness Equivalents																	
Additive Method Electroless Copper No-Etch	—	—	—	-50µ [-0.0020]	-25µm [-0.0010]	-0µm [0.0000]	—	—	—	-76µm [-0.0030]	-50µ [-0.0020]	-0µ [-0.0000]	—	—	—	-101µ [-0.0040]	-76µm [-0.0030]	-0µm [-0.0000]
Semi Additive Method Copper-No Overplate	—	—	—	-50µm [-0.0020]	-25µm [-0.0010]	-0µm [-0.0000]	—	—	—	-76µm [-0.0030]	-50µm [-0.0020]	-0µm [-0.0000]	—	—	—	-101µm [-0.0040]	-76µm [-0.0030]	-0µm [-0.0000]
Tin Lead Overplate	—	—	—	-76µm [-0.0030]	-50µm [-0.0020]	-25µm [-0.0010]	—	—	—	-101µ [-0.0040]	-76µm [-0.0030]	-25µm [-0.0010]	—	—	—	-127µm [-0.0050]	-101µm [-0.0040]	-25µm [-0.0010]

Table 3–9 Conductor Width Tolerances

Feature	Level A	Level B	Level C
Without plating	+0.05 –0.10 [+0.002] [–0.004]	+0.03 –0.05 [+0.001] [–0.002]	+0.02 –0.04 [+0.0008] [–0.0016]
With plating	+0.10 –0.10 [+0.004] [–0.004]	+0.08 –0.08 [+0.003] [–0.003]	+0.05 –0.05 [+0.002] [–0.002]

Table 3–10 Conductive Pattern Location Tolerances

Greatest Board/ X, Y Dimension	Level A	Level B	Level C
Up to 300 mm [12.0]	0.30 mm [0.012]	0.20 mm [0.008]	0.10 mm [0.004]
Up to 450 mm [18.0]	0.40 mm [0.016]	0.30 mm [0.012]	0.20 mm [0.008]
Up to 600 mm [24.0]	0.40 mm [0.016]	0.30 mm [0.012]	0.20 mm [0.008]

result is a scrapped PB. Since signal conductors intersect the lands from all directions, any breakout has the potential to randomly disconnect conductors all over the PB.

Maintaining consistent annular ring control is difficult at best, another method had to be developed to insure connectivity between lands and conductors. This method is called filleting, corner entry or keyholing. Explained simply, each method is intended to provide excess original copper material at the junction where the conductor enters the land. The land which is filleted resembles a teardrop; it is square for the corner entry, and looks like a figure eight for keyholing. All features point in the direction of the conductor to permit additional misregistration allowances (see Figure 3–28).

3.6.4.5 Fabrication Panel Format Components can be mounted on individual boards or on boards that are still organized in panel form. Boards or panels that will be moved by automatic handling equipment or pass through automated operations, (parts placement, soldering, cleaning, etc.) must have the sides kept free of parts or active circuitry. Special tooling and fixturing holes are generally located within the edge clearance areas. The clearance areas are needed to avoid interference with board handling fixtures, guidance rails and alignment tools.

Typically a clear area of 3.0 to 5.0 mm [0.118 to 0.200 in] must be allowed along the sides for the clearance. The required clearance width is dependent upon the design of the board handling and fixturing equipment. These dimensions should be obtained from the equipment manufacturer before board or panel design. (See Figure 3–29.)

For accurate fixturing, a minimum of two (and preferably four) nonplated holes are located in the corners of the board to provide accurate mechanical registration on board transfer equipment. Board handling holes (typically 3.2 mm [0.125] diameter) may also be located in the clearance areas. These holes are used by automated board handling equipment to move boards (or panels) from station to station in automated assembly lines. Specific sizes should be obtained from the equipment manufacturer. In addition, optical fiducial marks may be located near the fixturing holes if optical alignment is used, to improve registration (see Figure 3–14).

3.6.4.6 Board Size and Panel Construction In order to fully utilize the automation technology associated with surface mount components, a designer should consider how a printed board or P&I structure will be fabricated, assembled and tested. Each of these processes, because of the particular equipment used, requires fixturing which will

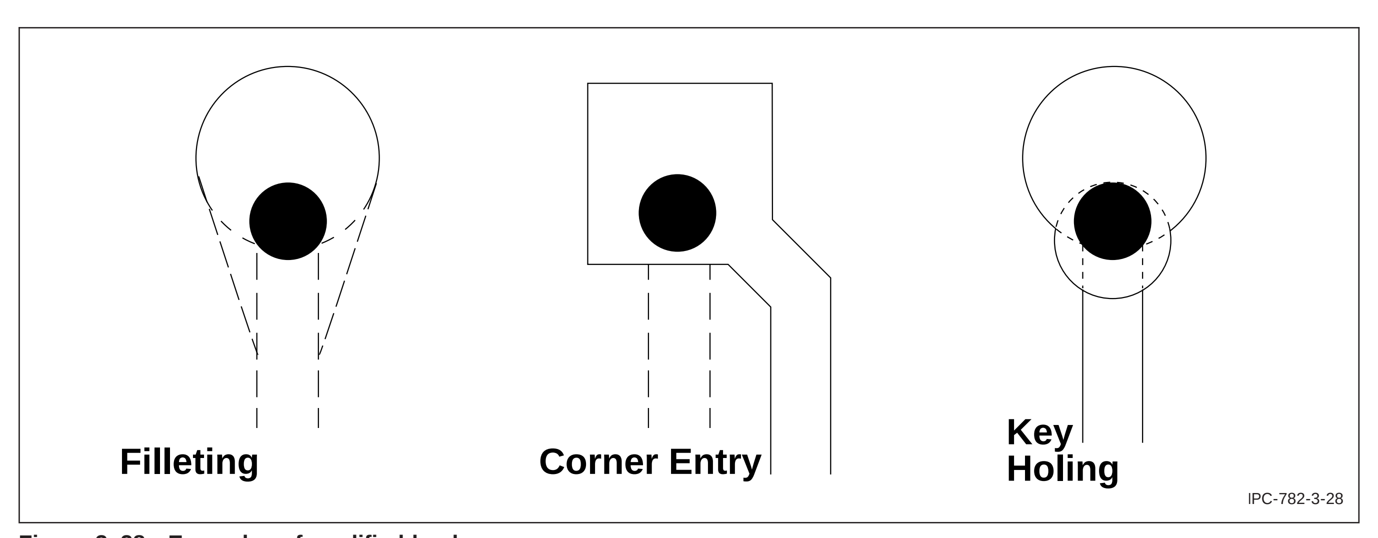


Figure 3–28 Examples of modified landscapes

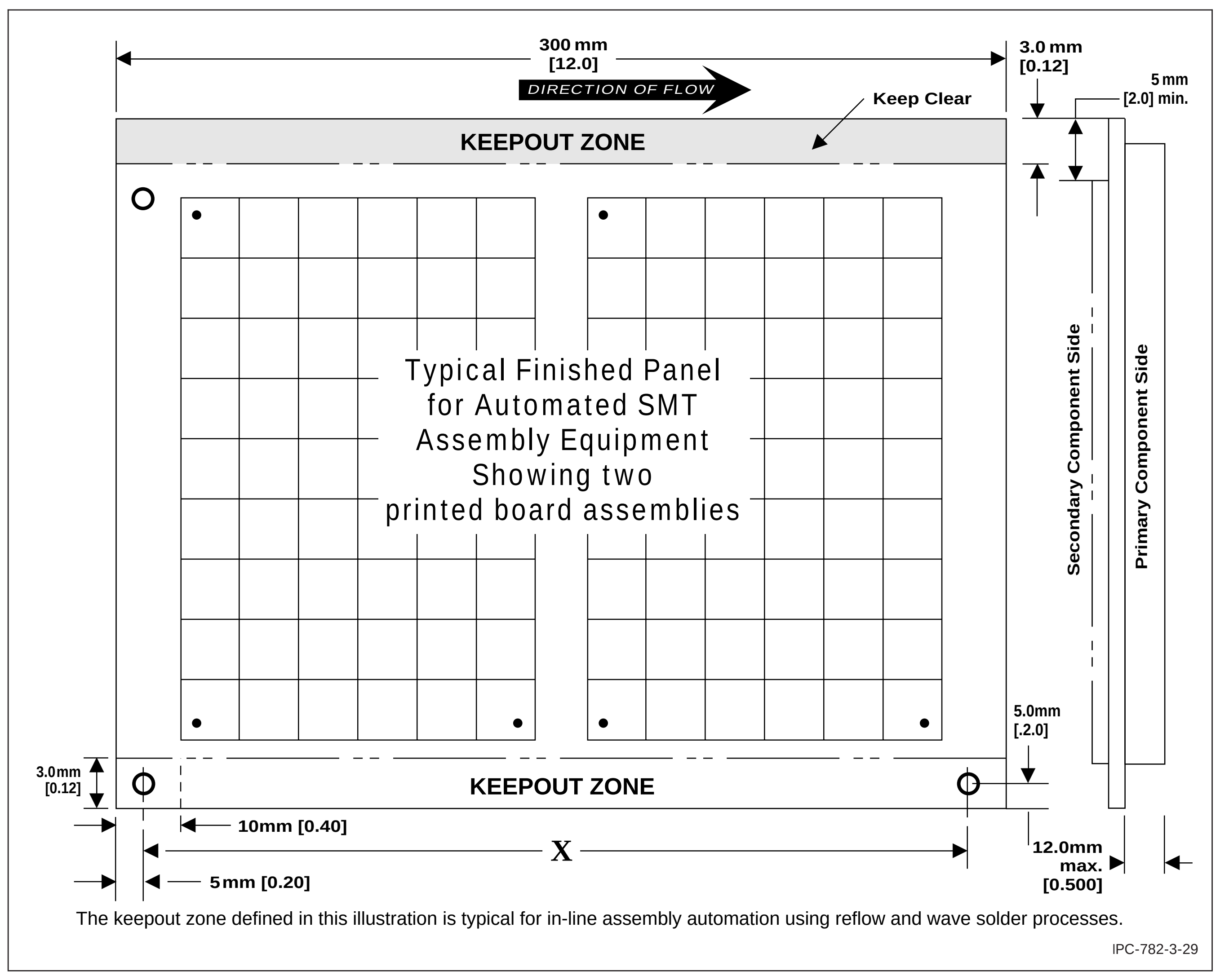


Figure 3–29 Typical copper glass laminate panel

affect or dictate certain facets of the board layout. Tooling holes, panel size, component orientation and clearance areas (both component and conductor) on the primary and secondary sides of the board are all equipment and process dependent.

To produce a cost effective layout through optimum base material utilization a designer should consult with the board fabricator to determine optimum panel size. The board should be designed to utilize the manufacturer's suggested usable area. Smaller boards can be ganged or nested on this same panel size to simplify fixturing and reduce excessive handling during assembly. Most manufacturers will suggest various methods of retaining assemblies in panels. A method should be chosen taking the assembly and test processes into consideration.

Figure 3–29 shows the typical use of a copper clad glass laminate panel. See IPC-D-322 for panel to board relationship.

Small boards can effectively be arranged on a single working panel, if the designer works closely with manufacturing. These are commonly called nested panels or pallets.

Panel construction may include several boards arranged in a matrix or simply one board requiring additional material retained for efficient assembly processing. The large board or several smaller boards are retained in the panels and separated after all assembly processes are completed. Excising or separating the individual boards from the panel must be planned as well. Several methods are used to retain circuits in a panel, including V-groove scoring and routed slot with break-away tabs.

V-groove scoring is generally provided on both surfaces of the board, and only in a straight line. A small cross section of board material is retained at the break line. An allowance for the scoring angle must be made as well. Conductors that are located too close to the score groove will be

exposed or damaged, and rough edges must be sanded lightly to remove burrs and rough fabric particles. See Figure 3–30.

The routed slot and tab pattern is widely used for panel construction and break-away tab extensions. Routing is more precise than scoring, and edge surfaces are smooth, but the break-away ‘‘tab’’ points will require consideration. Tabs can be cut and ground flush with the board edge or pre-drilled in a pattern. The drilled pattern furnishes a low stress break point on the ‘‘tab’’. If the hole pattern is recessed within the board edge, secondary sanding or grinding can be bypassed. See Figures 3–31 and 3–32.

3.6.4.7 Artwork Compensation and Scaling Artwork compensation and scaling are two adjustments that are made by the printed board fabricator to the original printed board artwork film or CAD data prior to beginning the fabrication process.

Modifications are made to the artwork feature sizes to compensate for the etch factor that occurs when etching away unwanted copper from the inner and outer layers of a printed board. The outer layers require more compensation than inner layers due to the overplating of copper and other metals that form the copper protection during the etching process. This is one of the reasons conductor width control on outer layers of printed boards can be substantially more difficult than inner layer conductor width control.

Scaling is an adjustment made to the artwork by the fabricator offset printed board material shrinkage, which is in the range of 8–13 µm [0.00035–0.0005 in] per 25 mm, that occurs during the lamination process. When the annular ring requirements fall below a nominal 0.25 mm [0.010 in], artwork scaling will typically be invoked by the printed board fabricator.

3.7 Outer Layer Finishes

3.7.1 Soldermask vs. Lands Only In referring to the outer layers of the multilayer PB, there is a dramatic difference between the concepts of soldermask and having no conductors on the outer layers. Conventional SMT design rules allow routing conductors on the outer layers, running the conductors between Surface Mount lands, then applying soldermask to cover the conductors and leave the lands exposed. For high density SMT applications, the conductors and clearances on the outer layers are generally in the 0.15–0.2 mm [0.006–0.008 in] range.

Aside from the soldermask registration, maintaining precision conductor width control on the outer layers is significantly more difficult than on the inner layers. Outer layer conductor integrity can be a cause of poor fabrication yields. The soldermask rule is very simple: the conductors between lands must be covered with soldermask, while the lands must not have any soldermask on them. When using smaller geometries, adding the Standard Fabrication Allowance of 0.2 mm [0.008 in] can make soldermask registration very difficult.

Given the two distinct yield difficulties of conductor width control and soldermask application, board manufacturers with experience in high density SMT printed conductor

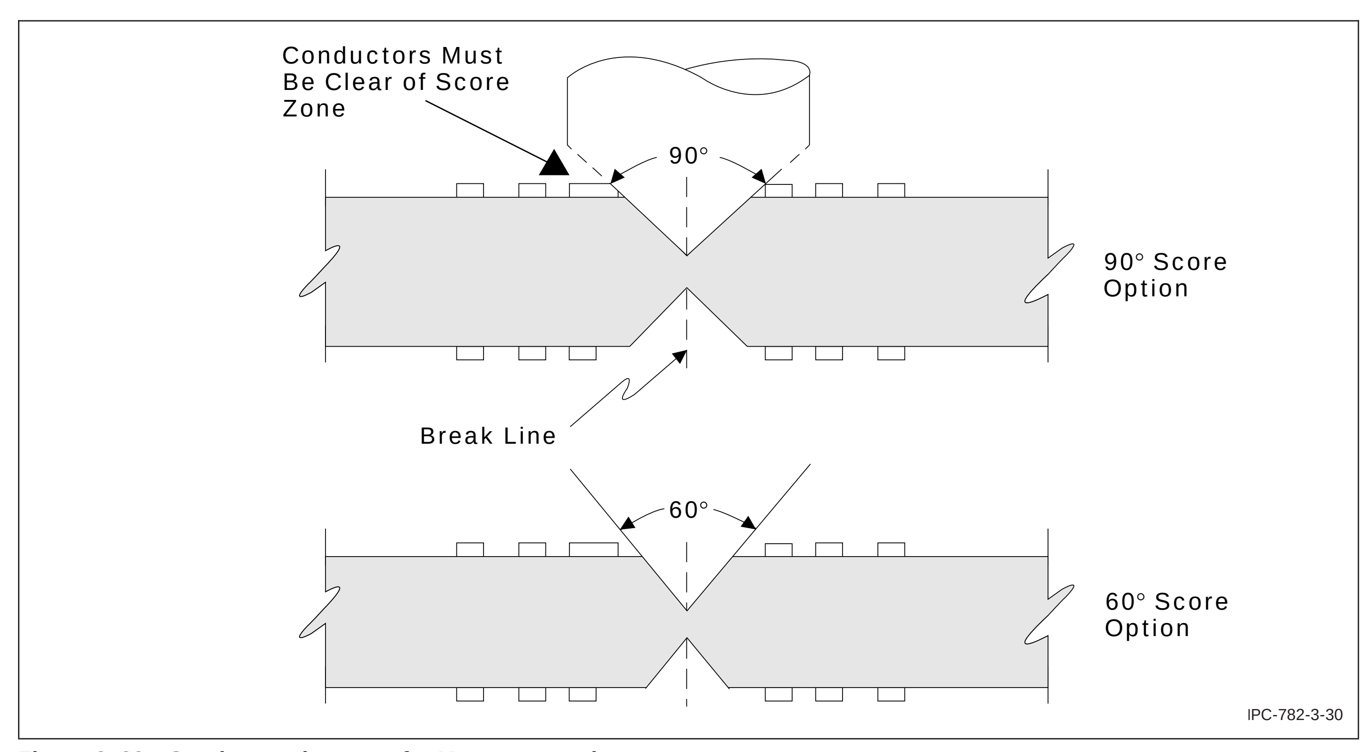


Figure 3–30 Conductor clearance for V-groove scoring

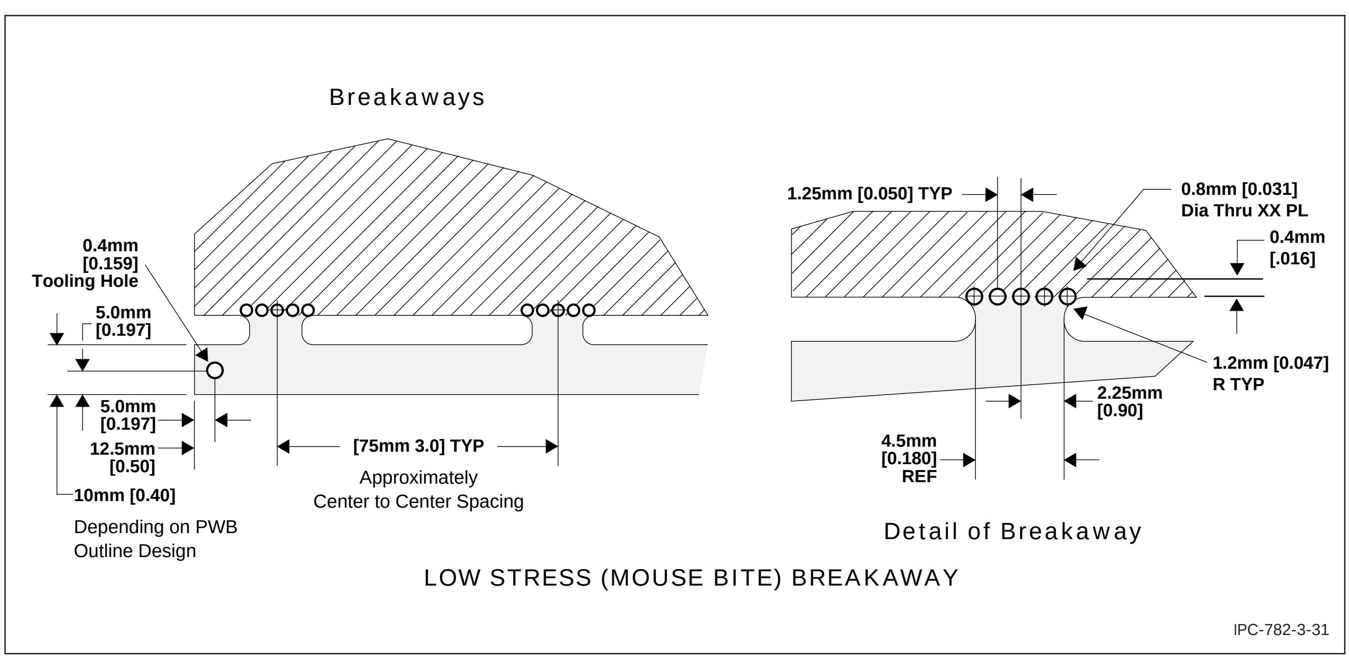


Figure 3–31 Breakaway (routed pattern)

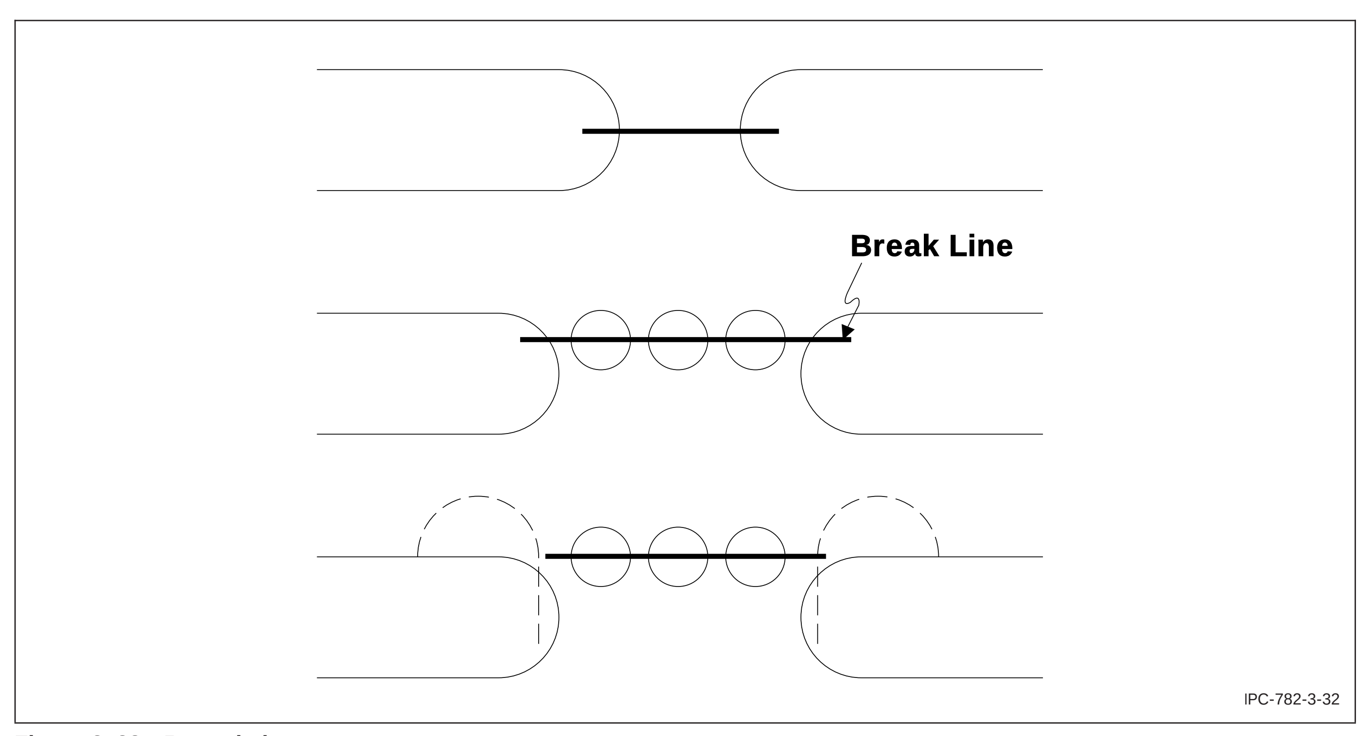


Figure 3–32 Routed slots

boards may favor the lands only (pad cap) concept. The pad cap concept has two yield improvement benefits: 1) no fine conductor geometries on the outer layers because they are buried in the inner layers where conductor width control is significantly easier, and 2) the need for soldermask is reduced or eliminated because there are no small spaces to protect from the soldering process.

In general, an 8-layer printed board, with lands only on the outer layer, is similar in cost to a 6-layer printed board with solder mask, assuming both have SMT geometries. The primary reason for this is that some PB fabricators are realizing about a 12% yield improvement by not having the fine line conductors on the outer layers.

The benefits of pad caps continue into the assembly process by increasing yields through the reduction of solder shorts or bridging. The pad cap concept provides 100% testability, thus testing benefits are both economical and practical.

3.7.2 Soldermask Issues Rework of Surface Mount Assemblies due to soldermask related defects is cited as a major cause of problems by assembly people. Following are two classes of assembly problems caused by improperly applied soldermask: 1) soldermask on the component mounting lands; 2) insufficient soldermask coverage of unrelated circuit features in close proximity to the component mounting land.

Regarding soldermask on the lands and assuming that the solderability requirements of the component leads and board mounting lands have been met, the solder paste composition, viscosity, and aging are within limits, and the thermal profile of the reflow oven is correct, the only other variable which could be detrimental to good solder joint integrity is soldermask material on the lands. If there is any soldermask (even if invisible to the naked eye) on the lands during reflow, solder joint integrity can be lost through improper surface wetting.

The second class of assembly defects is created when there is insufficient soldermask coverage of circuitry in close proximity to the component mounting land leading to solder shorts or bridging. The majority of SMT designs incorporate very small geometries of 0.15–0.2 mm [0.006–0.008 in] conductors and spacing on the outer layers of the printed board. Designing a soldermask to cover a 0.15 mm [0.006 in] conductor and only half of the 0.15 mm [0.006 in] space between the conductor and the land is easy enough to accomplish during design. However, photo imaged soldermask will overcome most of the above issues (see Section 3.7.4).

Close examination of solder bridging on Printed Board Assemblies will reveal that most of the bridging actually occurs between the component leads above the surface of the PB, and not between the lands on the board. Even if a soldermask has sufficient resolution and registration to provide a solder dam between lands, it still may not prevent bridging between the leads. Soldermask should not, and can not, be expected to compensate for deficiencies in the soldering process if the assembly uses Fine Pitch components.

3.7.3 Solder Mask Clearances A soldermask may be used to isolate the land pattern from other conductive features on the board such as vias, lands or conductors. Where no conductors run between lands, a simple gang mask can be used as shown in Figure 3–33. Tolerance requirements for this design can generally be met by a screen printed soldermask. A 0.38 mm [0.015 in] spacing could be acceptable. Any class of solder mask per IPC-SM-840 could be applied. The most commonly chosen solder mask would be a Class 3 mask because of its higher temperature characteristics. Due to the close proximity of the solder mask to the land pattern, care must be taken in choosing a mask that has low flow and low solvent-bleed characteristics to avoid land pattern contamination.

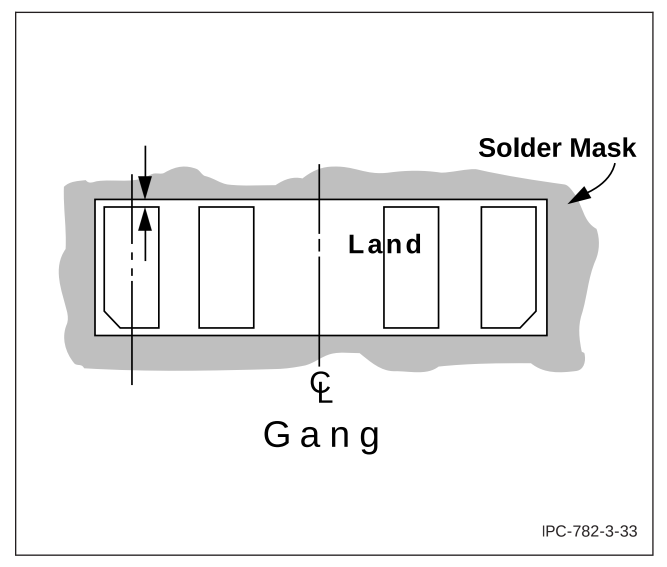


Figure 3–33 Gang solder mask window

For land pattern designs with routed conductors between lands (Figure 3–34) the tolerance requirement would require a photo-imageable soldermask. This is necessary because of the tight tolerance needed to cover the conductors without encroaching on the land area. A 0.08 to 0.125 mm [0.003 to 0.005 in] clearance is required with this type of design.

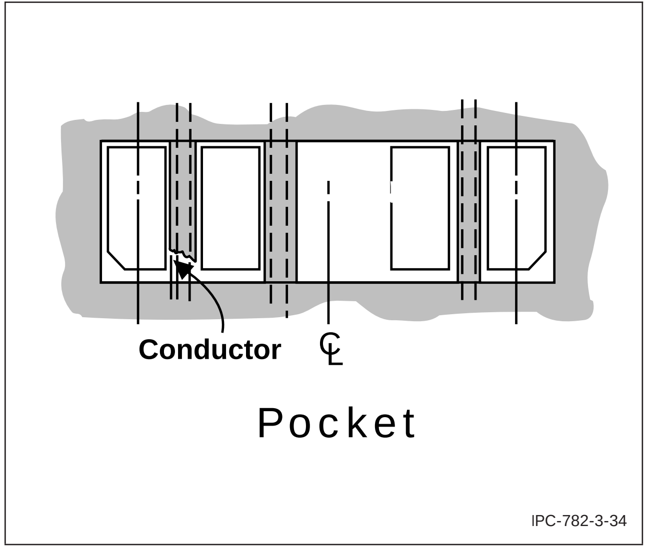


Figure 3–34 Pocket solder mask windows

3.7.4 Soldermask Types Solder mask coatings are available in two forms, liquid and dry film. The polymer mask material is applied using several process methods and are furnished in varying thicknesses. As an example, liquid materials will have a finished thickness of 0.02 to 0.025 mm while the dry film products are supplied for 0.08–0.10

mm thickness and a low profile 0.04 mm finished thickness. Although pattern screen printing is available, photo-imaged soldermask is recommended for surface mount applications.

The photo process provides a precise pattern image and when properly developed eliminates mask residue from land pattern surfaces. The mask thickness may not be a factor on most surface mount assemblies but when fine pitch (0.63 mm or less) devices are mounted on the printed boards, the lower profile soldermask will provide better solder printing characteristics.

4.0 QUALITY AND RELIABILITY VALIDATION

4.1 Validation Techniques The variety of component tolerances, and the possibility that tolerances may vary on interconnection products, users are encouraged to establish validation of the land pattern and component geometry. In addition, components should be checked for their maximum operating temperature limits. Figure 4–1 shows a general graph of the upper and lower limits of various components.

Validations of parts and circuits may be accomplished through the use of standard test patterns. These patterns may be used not only to evaluate a particular part to a land pattern, but may also be used to evaluate a particular interconnection product that must go through the various processes being used in assembling surface mounted parts.

4.1.1 Test Patterns—Process Evaluations The following test patterns have been developed as standards that may be used for the evaluation of standard board materials, with a variety of standard parts. IPC-A-49 artwork is available for these tests. The land patterns represent land pattern designs from the original IPC-SM-782.

The test specimen contains conductors and plated through holes and parts connected in a single daisy chain. One end of the daisy chain is connected to a common ground while the other end of the chain is connected to land patterns, then to a plated through hole in which a wire may be soldered for test purposes.

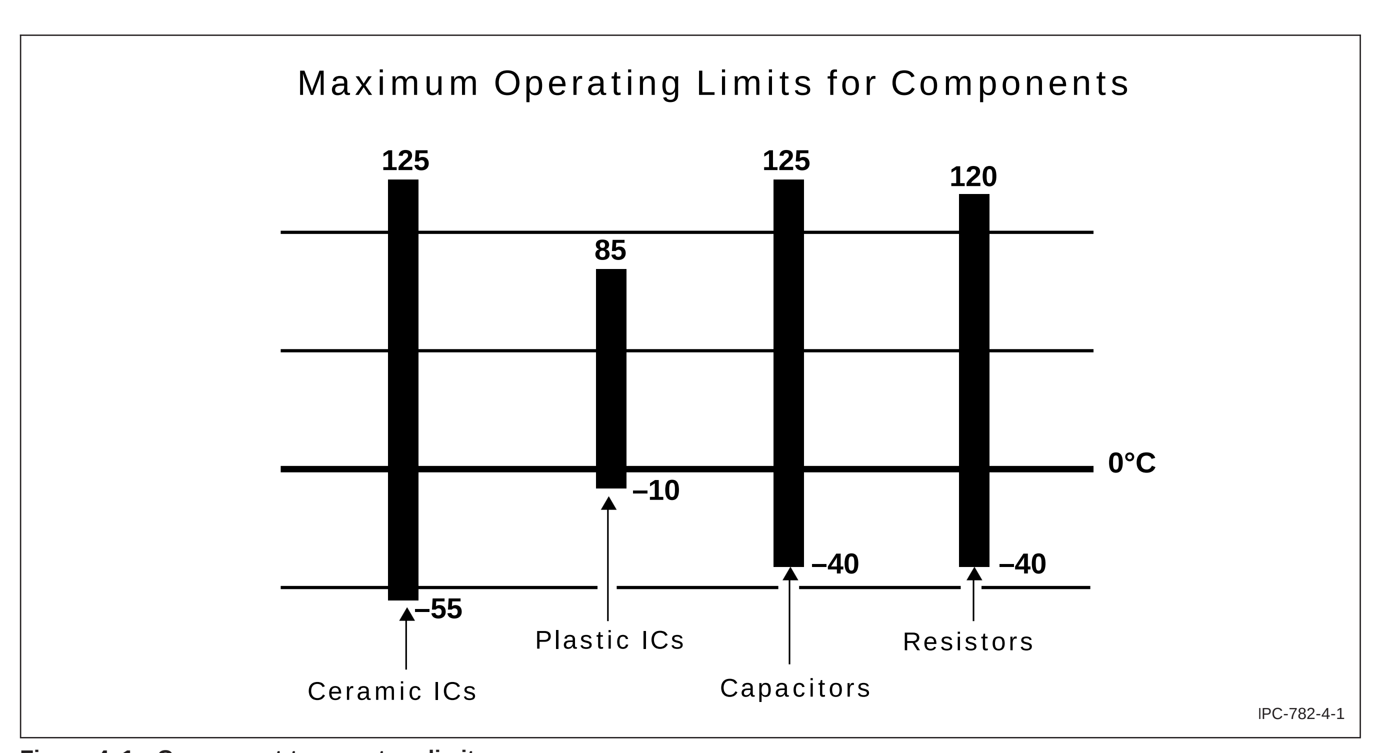


Figure 4–1 Component temperature limits

Circuits that are shown in Figures 4–2 and 4–3 contain the various components listed:

Test Vehicle

Primary (Top) Side	Secondary (Bottom) Side
__ SITE #1 (2) 44 I/O PLCC-J	__ SITE #1 Empty
__ SITE #2 (2) 16 I/O DIP-I	__ SITE #2 Empty
__ SITE #3 (8) RC1206 (8) SOT-23	__ SITE #3 (8) RC1206 (8) SOT-23
__ SITE #4 (1) 68 I/O CLCC-J	__ SITE #4 Empty
__ SITE #5 (68) I/O PLCC-J	__ SITE #5 Empty
__ SITE #6 (8) MELF 1/4W (8) CC1825	__ SITE #6 (8) MELF 1/4W (8) CC1825
__ SITE #8 (2) 24 I/O SOIC-L	__ SITE #8 Empty

Another test specimen is used for the testing of printed board structures that are intended to provide P&I structures used primarily for the mounting of leadless chip carriers. This test board is described in surface mount land pattern round robin artwork (IPC-A-48). The board is a 12-layer multilayer board which contains 38 positions for mounting leadless chip carriers used by an Air Force Mantech Program to evaluate printed board and substrate materials. The test boards produced from this artwork may contain metal cores, or other planes that control the coefficient of thermal expansion of the P&I structure.

The following are some examples of the type of materials that may be used as the constraining core.

- Nonorganic materials (alumina)
- Porcelainized clad Invar materials
- Printed boards bonded to low-expansion support (metal or nonmetal)
- Compliant layer constructions
- Metal core boards

4.2 Test Patterns—In-Process Validator Test patterns to validate in-process conditions are encourage to be incorporated into the panel of a printed board assembly. These designed-in land patterns provide special features for automatic optical inspection and visual inspection.

The land patterns shown in section 8–13 are designed to provide a clear view of the soldering characteristic such that land geometry is visible, and solder joint evaluation can be achieved. The same in-process validator are used to check the registration of solder paste prior to reflow soldering.

Figures 4–4 through 4–11 are illustrations from J-STD-001 that provide the key variables for meeting soldering requirements that are necessary for various surface mount parts. Land pattern samples provided around the periphery of a panel, should be designed to provide clear visibility of the solder joints shown in these figures.

4.3 Stress Testing Stress testing usually consists of temperature cycling of the printed board assembly that has been surface mounted through various extremes. The temperature cycling of the assembly or a coupon may be a standard MIL- STD-202 test method which cycles the board from –65°C to 125°C.

Alternate temperature cycles are also available. A temperature cycle test of 400 consecutive cycles to 1000 cycles has been identified for some assemblies. In these examples, the ramp time from high to low temperature is 30 minutes, and the time at the extreme is also 30 minutes. Figure 4–12 shows an example of the excursion rate of the various conditions of temperature cycling.

During the cycling processes, daisy chained plated-through holes and daisy chained solder joints, are measured during the initial phase as to their resistance, and then monitored for increased resistance during the thermal cycling. Increased resistance of 30 microohms in most instances constitutes a failure of the either the plated-through hole, or the solder joint.

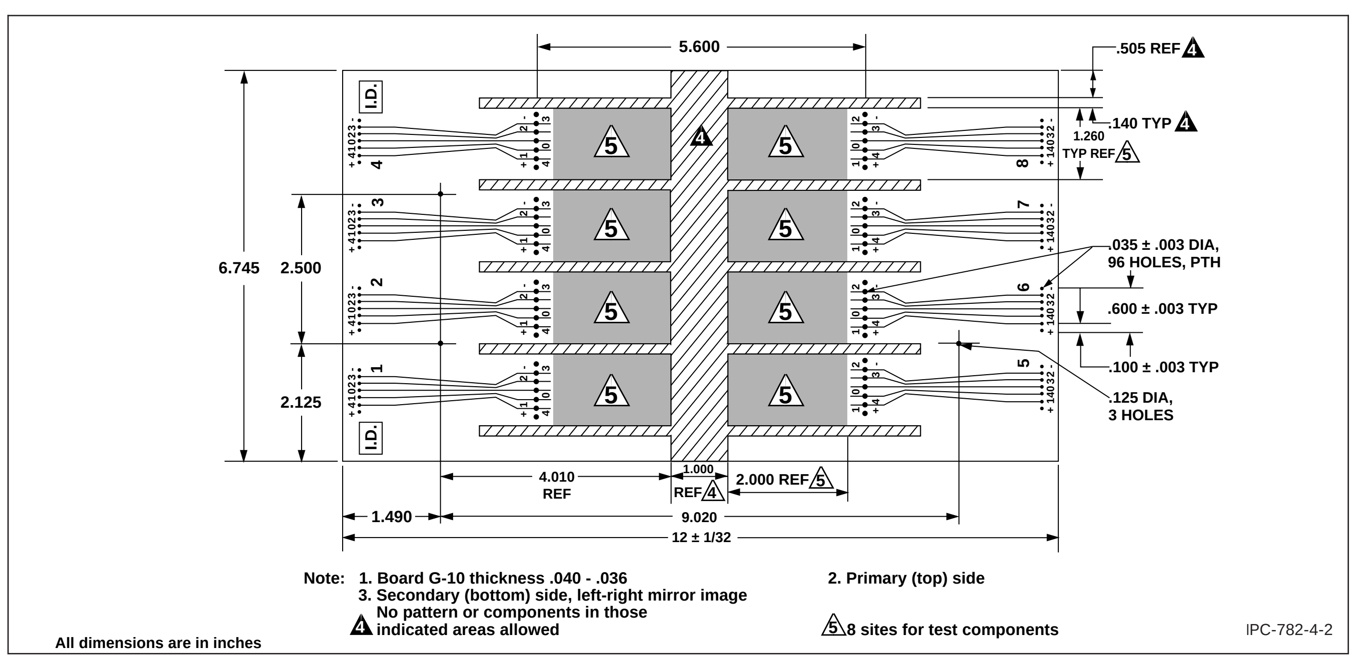


Figure 4–2 General description of process validation contact pattern and interconnect

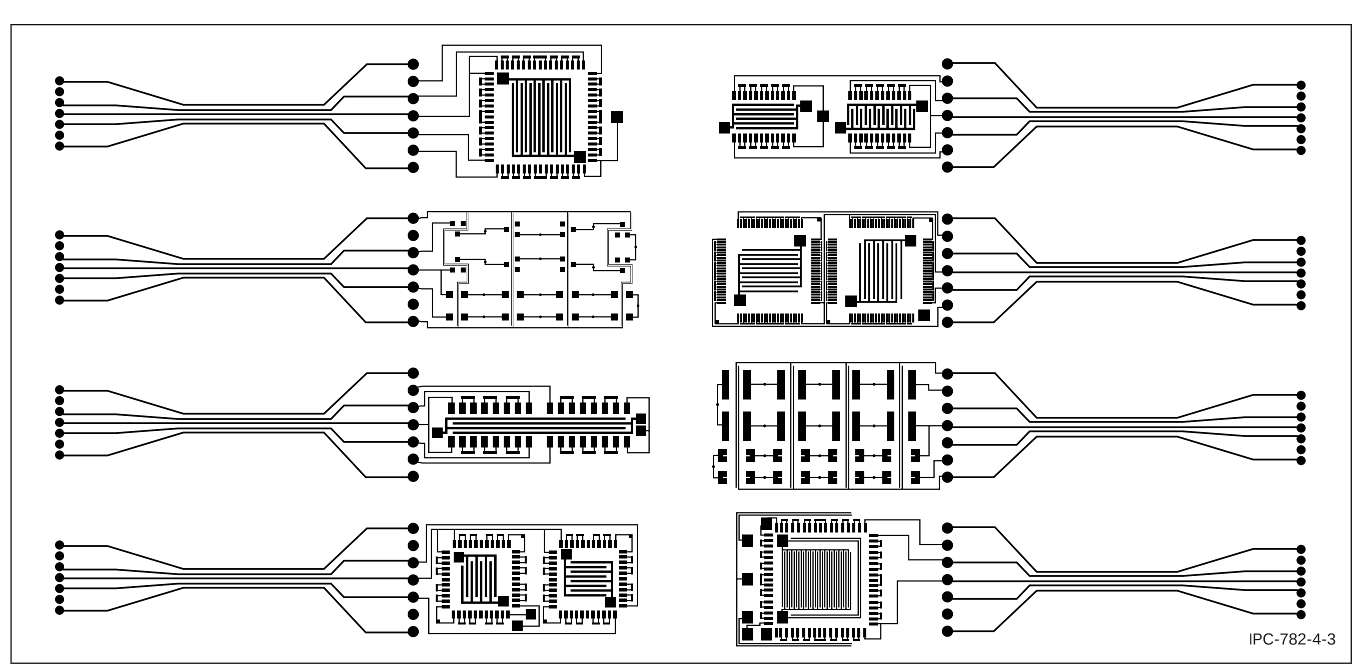


Figure 4–3 Photo image of IPC-A-49 test board for primary side

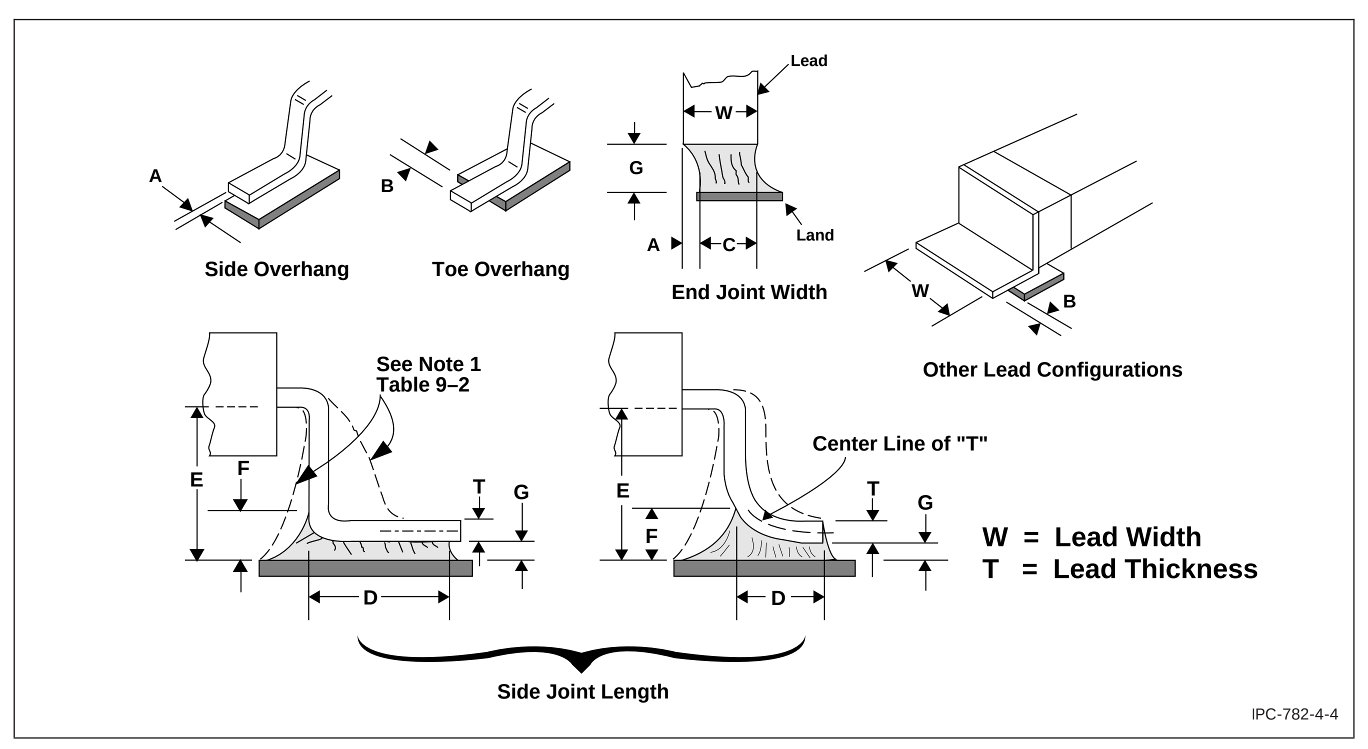


Figure 4–4 Flat ribbon, "L," and gullwing lead joint description

Note: See ANSI/J-STD-001 for specific details on minimum acceptability requirements.

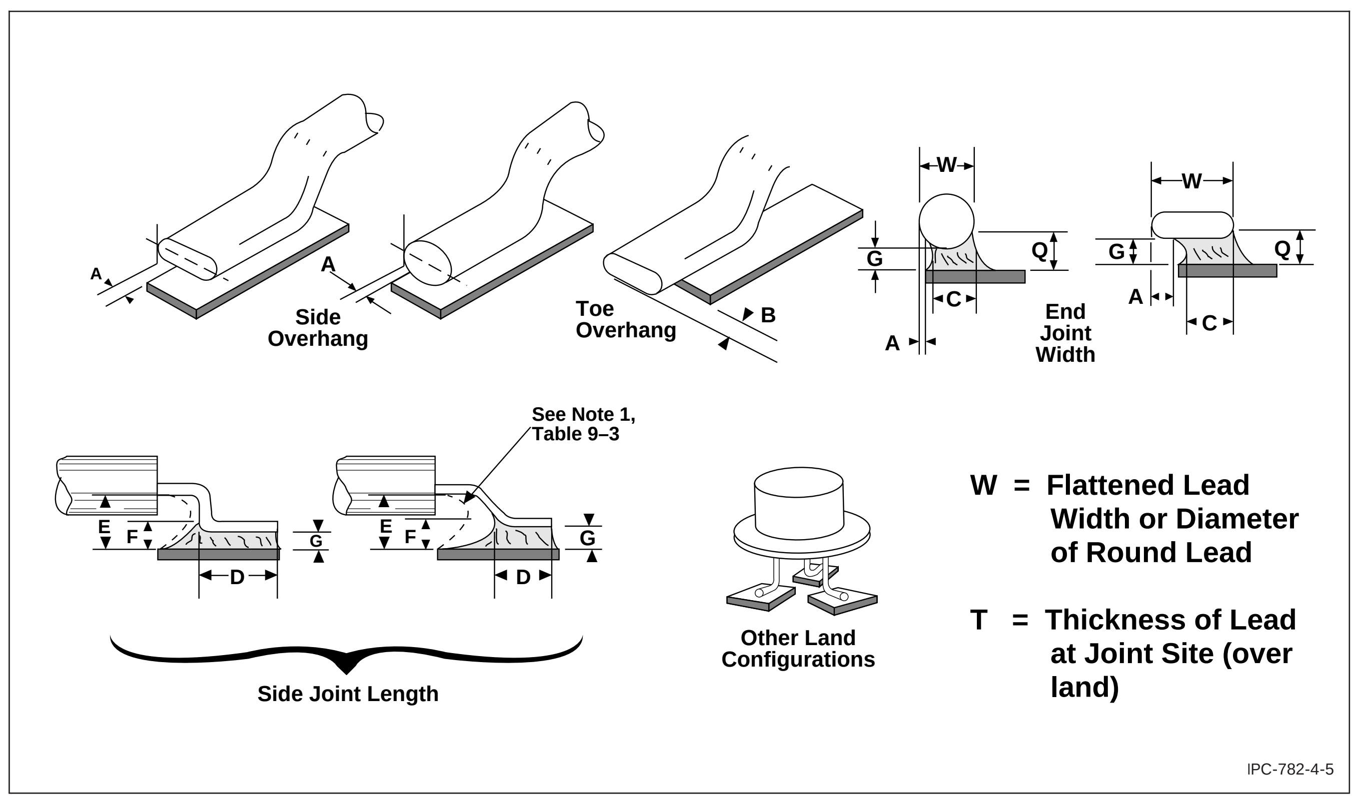


Figure 4–5 Round or flattened (coined) lead joint description

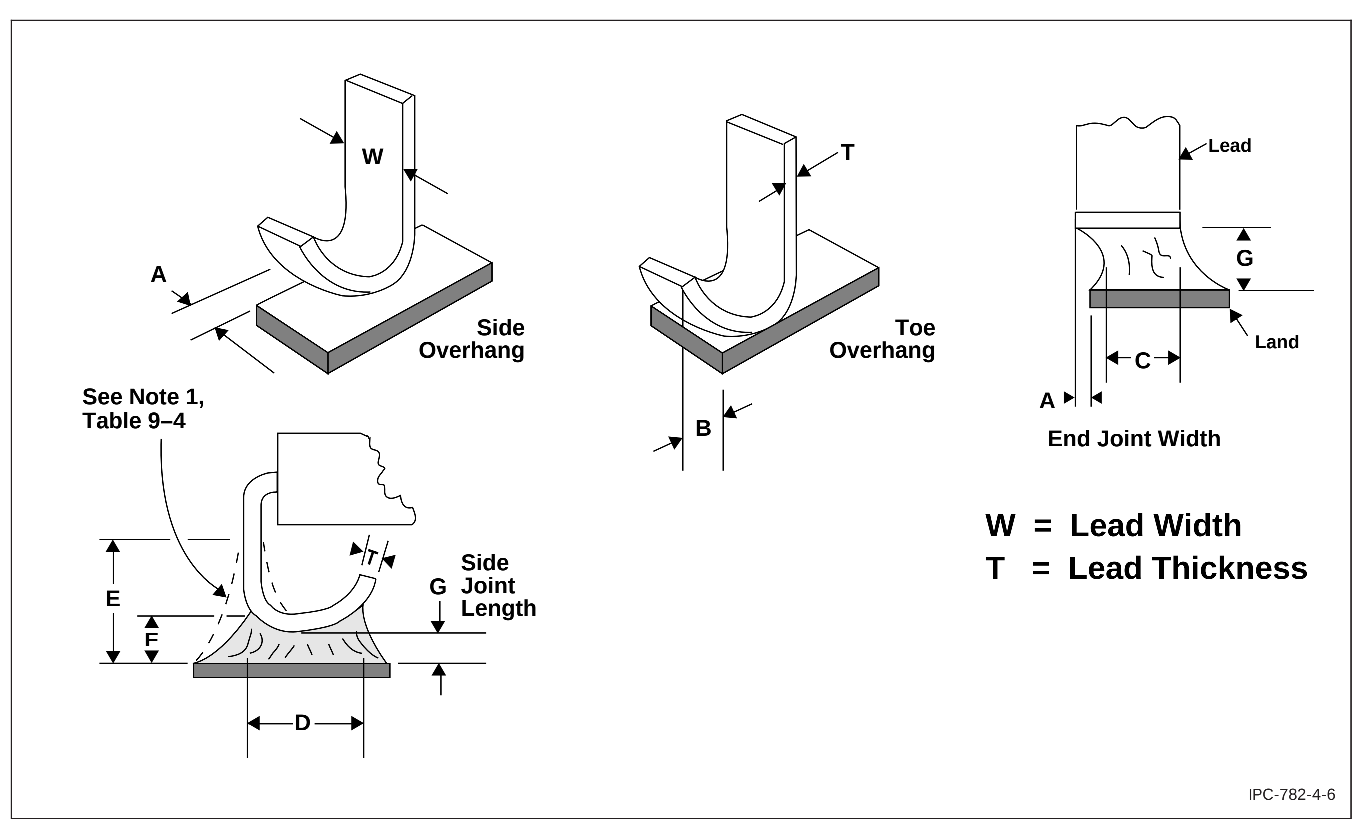


Figure 4–6 "J" lead joint description

Note: See ANSI/J-STD-001 for specific details on minimum acceptability requirements.

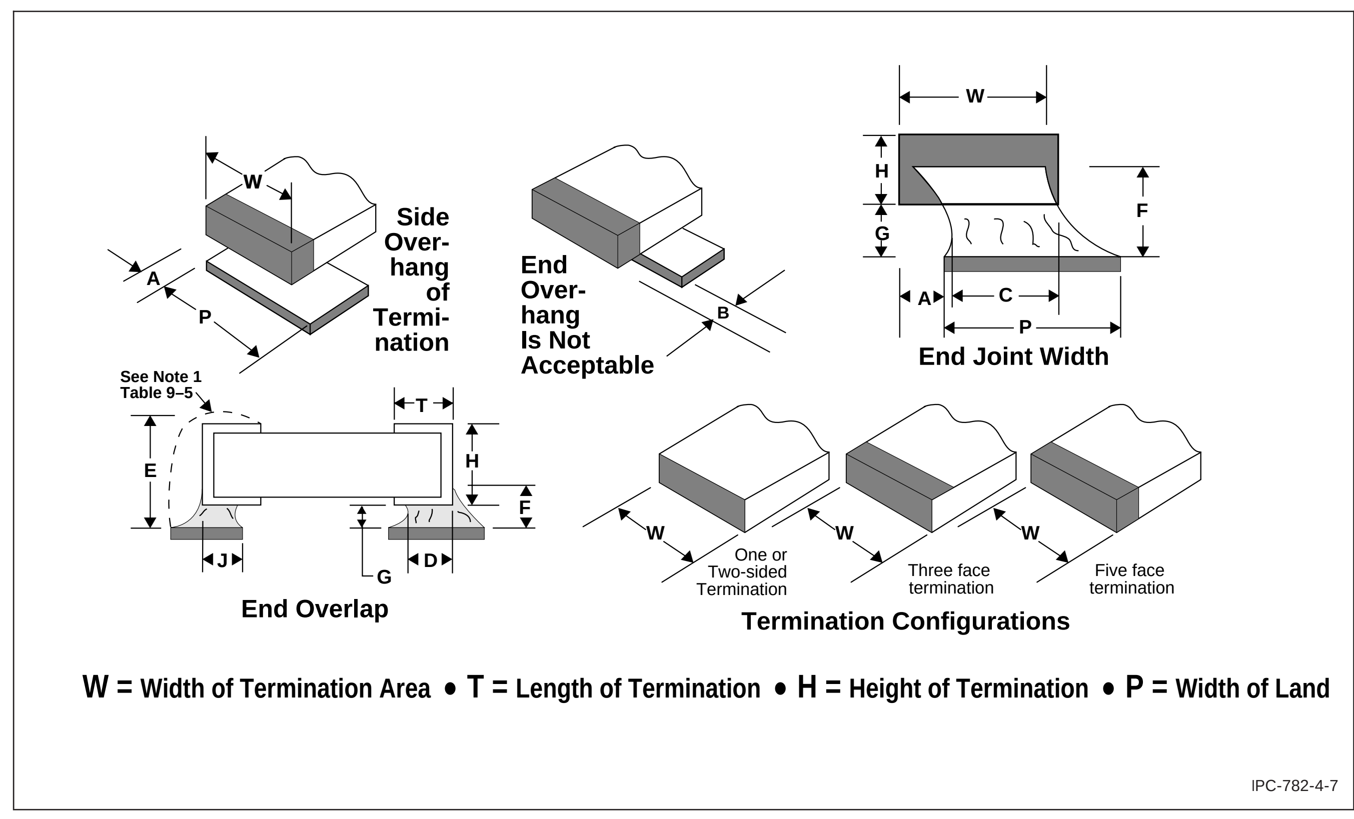


Figure 4–7 Rectangular or square end components

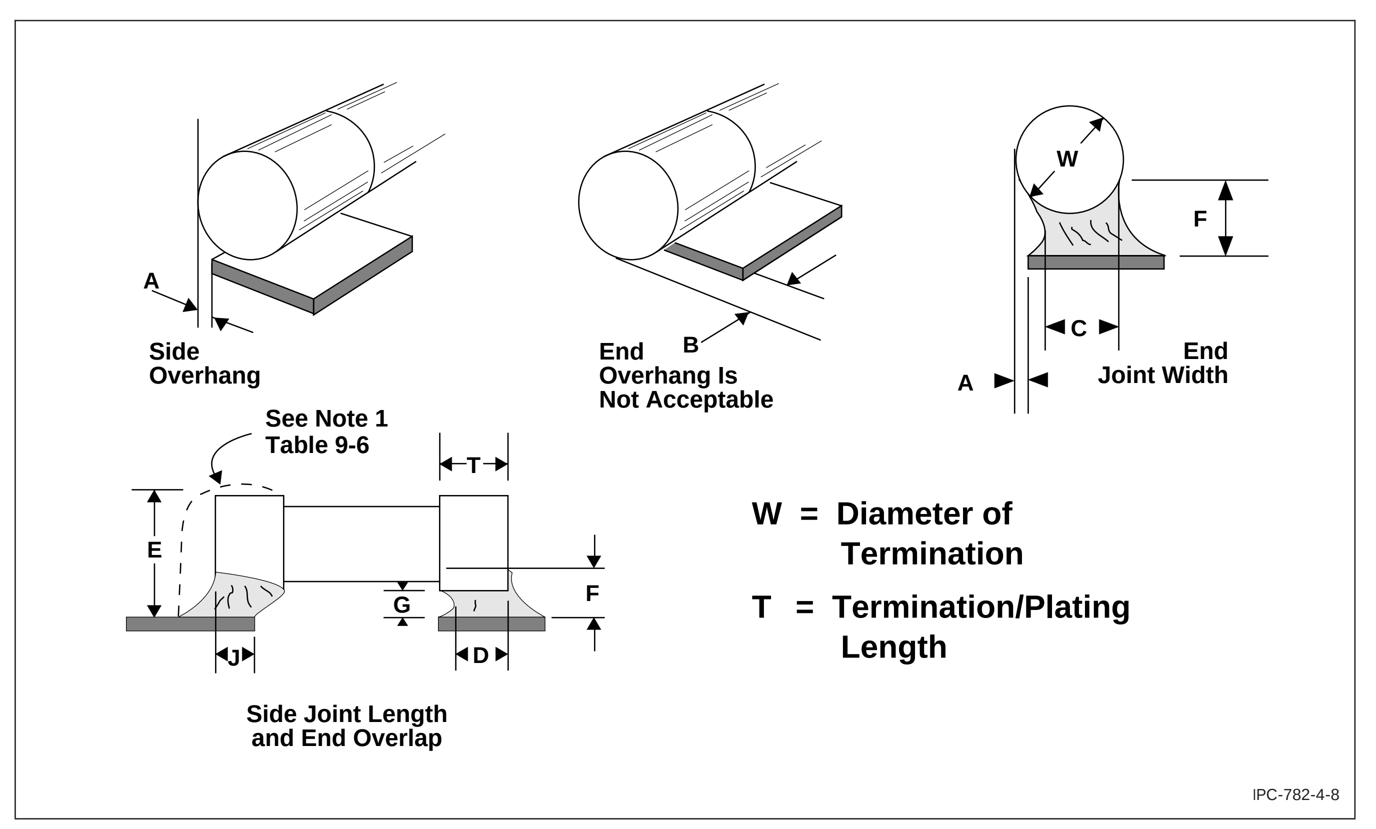


Figure 4–8 Cylindrical end cap terminations—joint illustration

Note: See ANSI/J-STD-001 for specific details on minimum acceptability requirements.

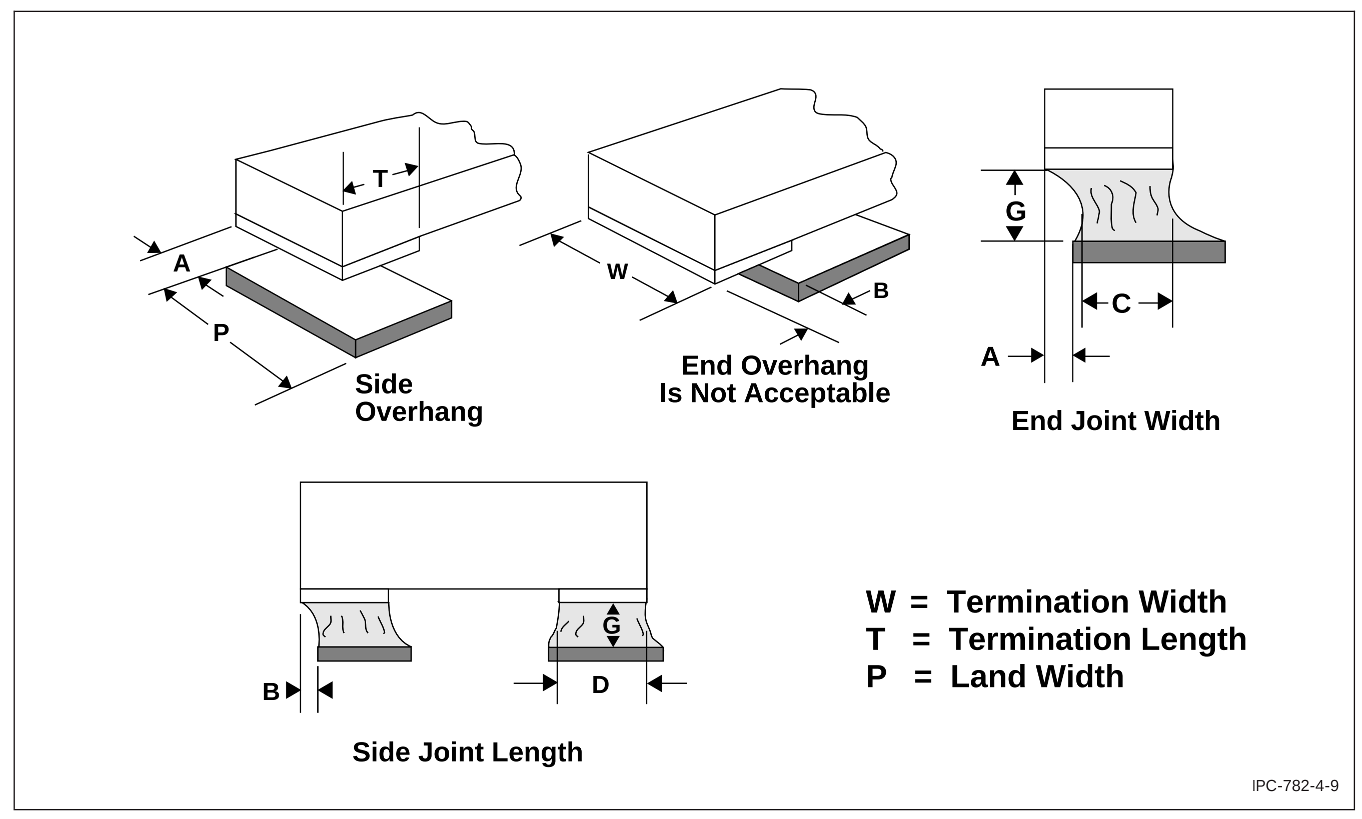


Figure 4–9 Bottom only terminations

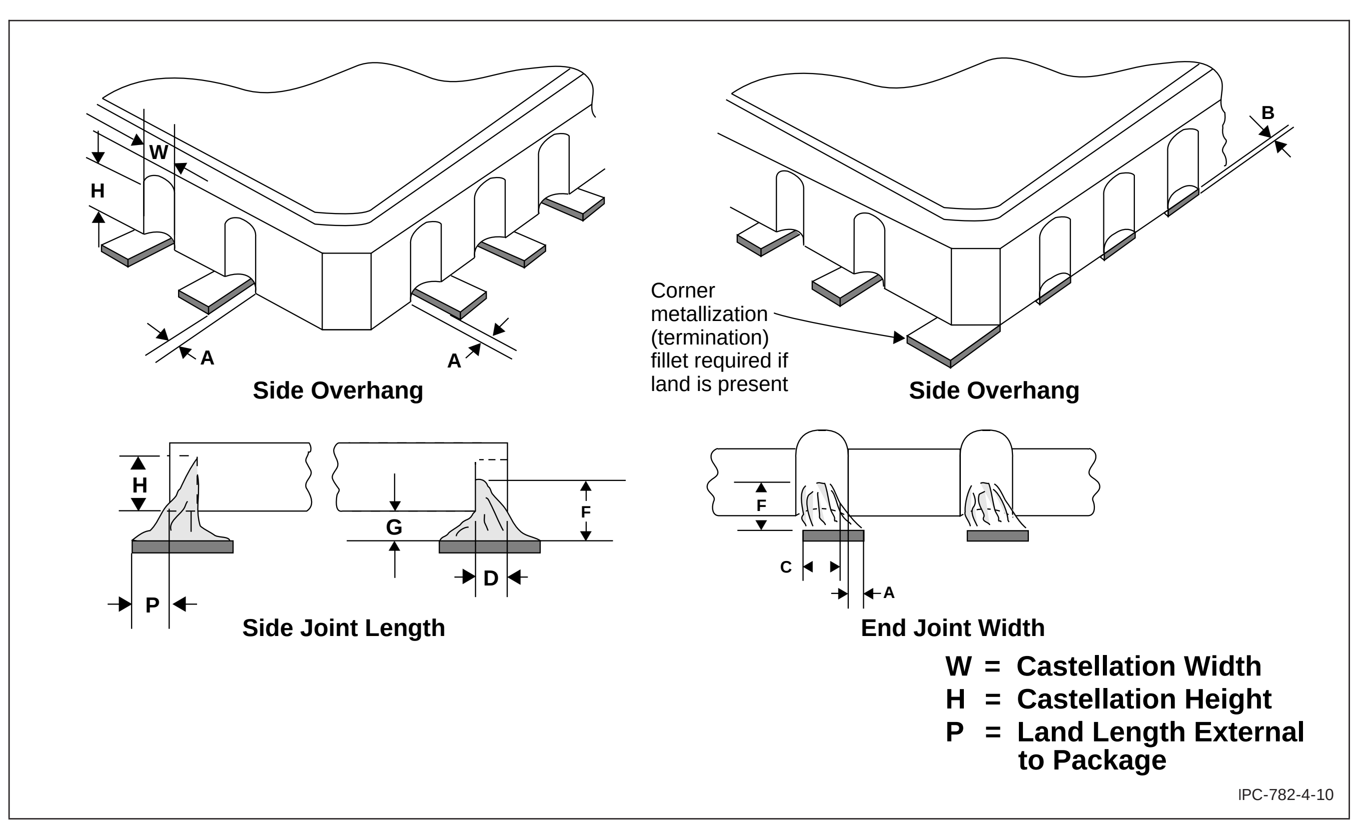


Figure 4–10 Leadless chip carriers with castellated terminations—joint description

Note: See ANSI/J-STD-001 for specific details on minimum acceptability requirements.

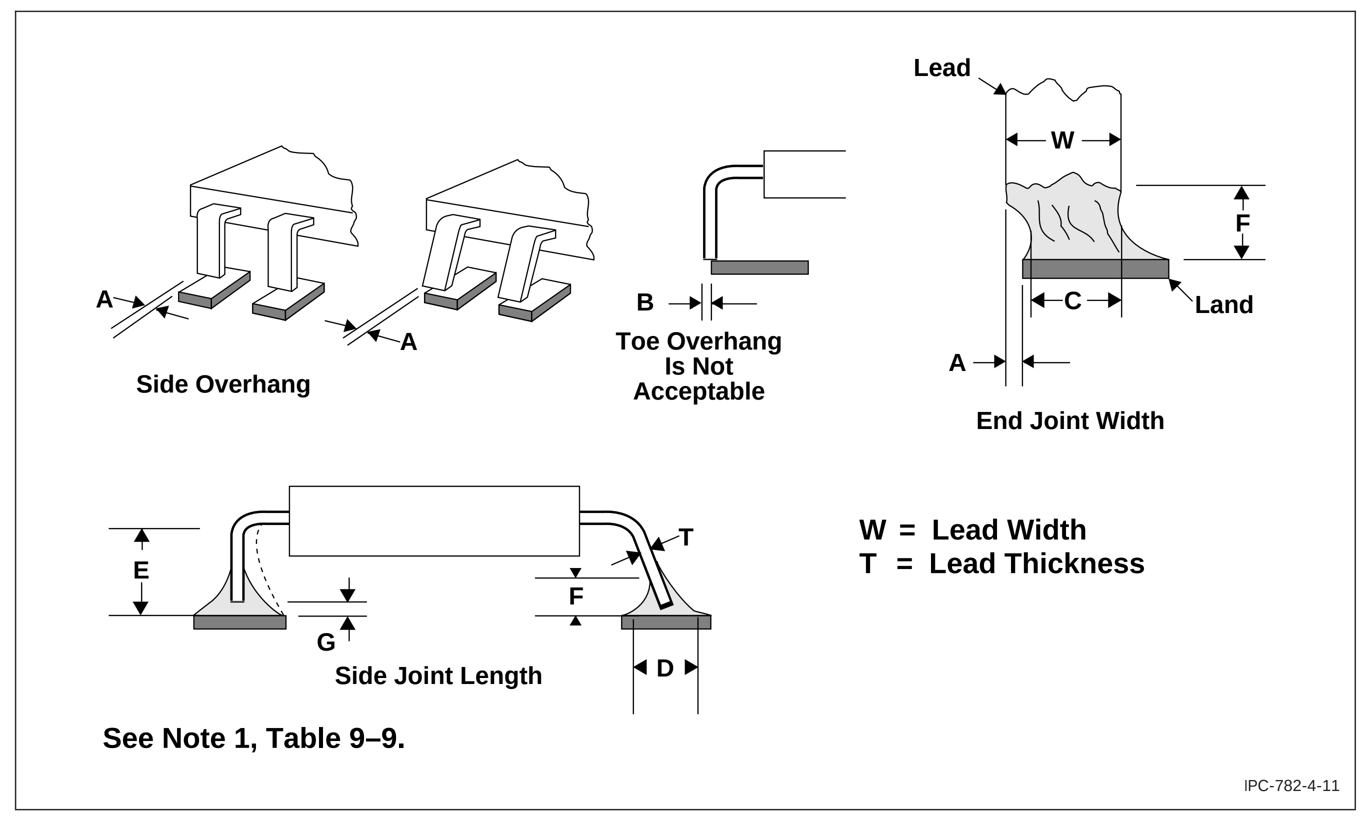


Figure 4–11 Butt joint description

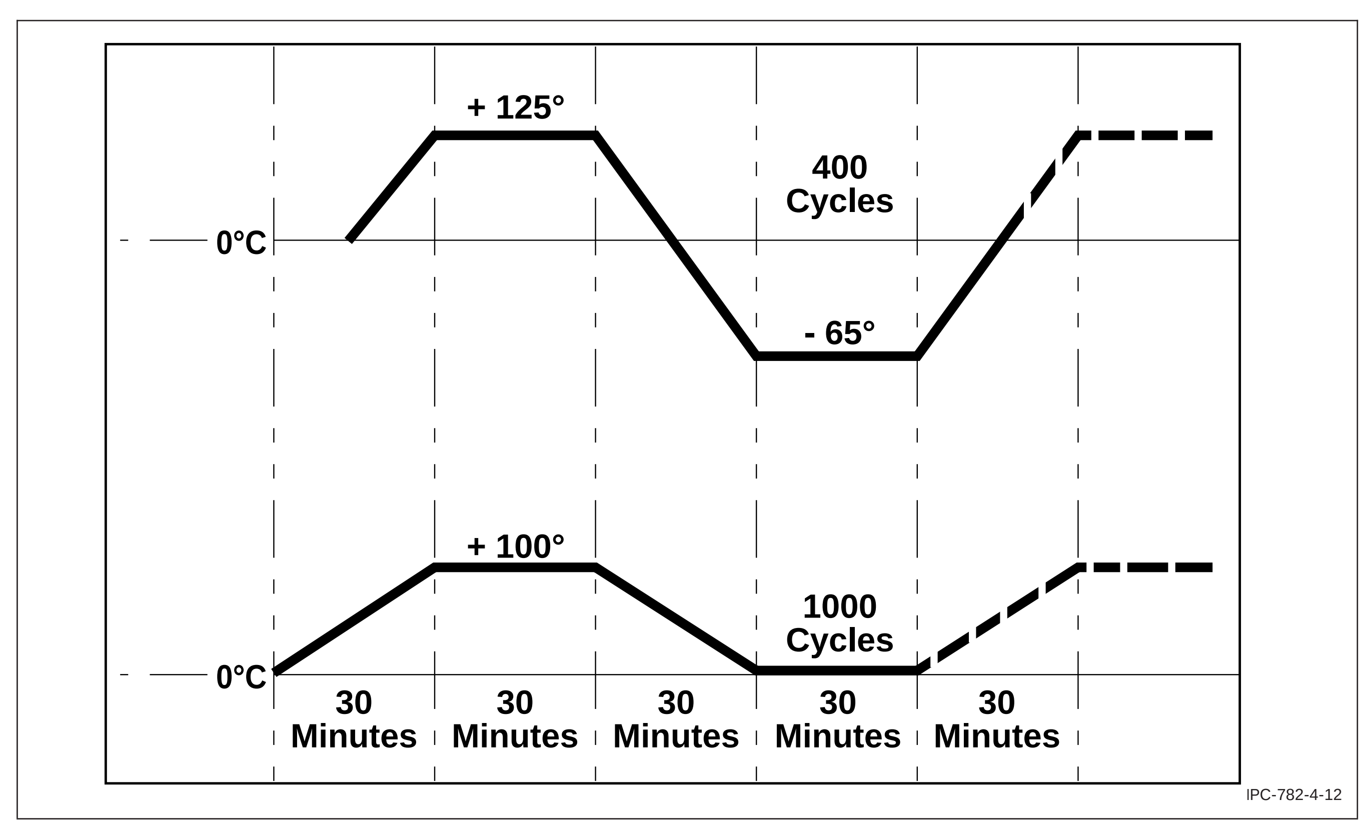


Figure 4–12 Thermal cycle excursion rate

5.0 TESTABILITY

5.1 Testing Considerations

5.1.1 Bare Board Test In testing printed board using through hole technology, the defect rate and the test methods chosen are the principle determiners of overall test cost. Real estate considerations (specifically the percentage of nodes that are available for bed-of-nails probing) are not a concern, since 100% nodal access practically comes ''for free''. In testing surface mount boards, however, real estate considerations (in addition to defect rates) impact test costs, since nodal access determines which test methods are possible and effective.

5.1.2 Loaded Board Test Given the same test costs, defect rate can be traded off against real estate. For example, if the defect rate is relatively high, most boards will require diagnosis, and the economics of Automatic Test Equipment (ATE) will demand that full nodal access be provided for in the board layout. If the defect rate is low, more time can be spent diagnosing each defect manually, rather than with ATE, and thus reduce the real estate impact to less than 100% nodal access. Extremely low defect levels would theoretically allow 0% nodal access (no bed of nails test at all), applying only a simple pass/no-pass test through the edge connector, and throw away failing assemblies rather than diagnose them.

The major considerations in determining nodal access are:

- Defect rate
- Diagnostic capability
- Real estate impact
  - —Board area
  - —Layer count
- Cost impact

Determining the percentage of nodal access to design into a board layout requires trading off all the issues discussed previously: defect rate, test development cost, test operation costs including manual troubleshooting costs, and of course, impacts on real estate. Short of having no defects at all, full nodal access remains the most desirable option.

As with Through Hole Technology boards, once the board is designed (nodal access fixed) and its tests are designed (test methods fixed), the defect rate becomes the primary key to reducing test costs. Therefore, defect reporting, analysis, and correction/prevention are imperative. This may involve closer supplier relationships to reduce component and board level problems, and in-house action to reduce process-induced problems.

5.2 Nodal Access In the early stages of product development cycles, test philosophies and strategies are often undefined. This is especially true when a company is moving from one level of packaging technology to the next higher level of packaging technology, for example, from through-hole technology to surface mount technology. During these transition periods, the concurrent engineering approach is essential for designing nodal access for testability into the product. Concurrent engineering is the principle vehicle by which test priorities can and should be moved up to the beginning of the design cycle and addressed with a higher priority. In the early stages of a design, a test philosophy should be clearly defined, then a strategy for executing the tests can be implemented. An ideal philosophy to adopt is one that identifies all of the different test types and the level of test that each type requires.

There are 2 basic categories of PB tests: The bare board test, and the loaded board test. The bare board test is performed at the end of the fabrication cycle and checks for shorts, opens, and net list connectivity. The loaded board tests occur at the end of the assembly cycle and are considerably more complex. They include: Manufacturing Defects Analyzer (MDA), in-circuit, functional and combinational tests.

The test philosophy should be written to encompass whatever combination of tests are necessary for the product. Then, a simple strategy for implementing the required tests can be defined prior to beginning the design process. Planning testability at the beginning of a product development cycle instead of the end can result in significantly lower test costs per node and provide higher nodal accessibility throughout the entire process from initial design to final test.

5.2.1 Five Types of Testing There are five basic types of tests which can be performed on SMT boards. These are:

- Bare Board Test
  Check the unpopulated board for shorts and opens
- Manufacturing Defects Analysis
  Checks the populated board for soldering shorts
- In-Circuit Test
  Operational verification of each individual component
- Functional Test
  Operational verification of functional block of circuits
- Combinational Test
  Limited integration of in-circuit and functional test

The first test type is a bare board test which is performed by the board fabricator. The remaining four test types are loaded on assembled board tests which are performed after assembly. The bare board test should be mandatory, while the loaded board may be tested using any combination of the four loaded board tests.

5.2.2 Test Philosophy The best test philosophy to adopt is one that will make provision for executing every test type available. Even if the product testing procedure is well defined at the beginning of the development cycle, it may

change after the design is complete. A generic test philosophy which has been applied to hundreds of dense SMT designs successfully.

• Strategic placement of all component vias
• Provide access to every node of every net
• Access every node from both sides of the board
• Grid based component and via placement
• Correct test pad geometries and clearances
• Do not probe directly to SMT component lands

Even in the most dense designs, the philosophy of providing 100% access to every node of every net from either side of the board can be accomplished. However, this decision must be made at the beginning of a design.

5.2.3 Test Strategy After the product test philosophy has been established, a test strategy or procedure can be defined. For an overview of several elements of a procedure consider the following:

• Vision inspection of inner layers using AOI
• Vision inspection of O/L land/via connections
• Probe only vias on either side for bare board test
• Do not damage SMT lands with probe tips
• Probe secondary side vias for loaded test board
• Screen paste on vias for airtight board

The actual product test strategy must be organized by all of the concurrent engineering team members who will be involved in the testing process. This will insure that the integration of the various test types and procedures will not have too much redundancy, or create gaps which may endanger test integrity.

5.2.4 Rework Strategy Rework of a multilayer SMT printed board can be difficult or impossible due to limited access to inner layer conductors. Typical rework procedures consist of manually cutting an inner layer conductor with special knives, programming a drill to move the board to a site on the board and then drilling a controlled depth hole to disconnect an inner layer conductor, or, lifting a lead on a surface mount component.

In the case of densely populated SMT boards, certain components may even have to be removed to gain access to a site where an inner layer conductor is to be cut. This violates an important rule with SMT components: Do not remove components from the board unless it is absolutely necessary. Doing so weakens the bond strength of the land to the board and may even cause the land to lift off the board. With some designs, where grid based 100% test via accessibility is built into the land pattern, the rework ports have been created. Each test via provides access to every conductor on every layer of the board without exception. In order to remove any terminal of any device from a net, the via may simply be drilled out by hand.

Using the vias as rework ports eliminates the need to remove any components, drill extra holes in the board, or cut into the board with a knife to disconnect nets.

Following disconnection, the device terminal may be reconnected to another terminal by simply soldering a wire to the terminal with a fine tip soldering iron. This is usually accomplished without disturbing any solder joints on the board, including the lead that is being soldered to the wire.

Aside from the wire, using this approach to rework an SMT printed board leaves no visible indications or obvious damage to highlight that the board has been modified.

5.3 Full Nodal Access Full nodal access has a different meaning for the bare board test than for the ATE test. To achieve full integrity at the bare board test level, 100% access to every node of every net is required. The number of test probes needed to test the board is equal to the total number of device terminations. However, in the case of most dense Surface Mount designs, this often requires the use of a double sided, or clamshell test fixture because all of the nodes are not accessible from one side of the board.

The ATE test only needs to have access to one node per net. Every net has at least two nodes. Some nets have many nodes, for example, on memory boards one net may be connected to many nodes. In order to achieve full integrity at the ATE test level, access to only one node of each net is all that is required. Therefore, the total number of test probes required to perform the ATE test is significantly less than the number required for the bare board test.

There are two alternatives to building in testability to the SMT printed board at the design phase. One is to build in 100% nodal access for the bare board test, with the secondary benefit being that 100% access for the loaded board test is automatically built in.

The other alternative is to build in 100% nodal accessibility for the loaded board test during the design phase. This approach will almost certainly guarantee that the bare board test will not have sufficient grid based test nodes available to complete the test without the use of a clamshell or two one-sided fixtures.

The use of design concepts with grid based 100% nodal access from either side of the board is the most economical approach from the total process perspective. If the grid based test land concept is used, the test fixtures for bare and loaded board tests will not become obsolete through later board connectivity revisions. This is yet another savings downstream in the product development process. Also, if the printed board uses buried vias, the grid based test land concept with 100% nodal access will even provide access to those buried nets from the ends of the nets. This is another benefit realized during the bare board test.

The overall impact on SMT printed board real estate must be considered when designing for test. There are three categories of design for test rules being employed on SMT designs:

1) complete the design, and add the test nodes randomly at the end;
2) develop land patterns with test vias on a 2.5 mm [0.100 in] grid;
3) develop land patterns with test vias on a 1.25 mm [0.050 in] grid.

The random approach needs no discussion. The second approach of bringing the land pattern test vias to a 2.5 mm [0.100 in] grid works with sparsely populated boards, but this approach consumes almost as much real estate as using Through Hole components. With the high component density requirements of most SMT designs, the third approach of bringing the land pattern test vias to a 1.25 mm [0.050 in] grid is the only method which will allow 100% test node accessibility for all printed board assembly types.

SMT has been and will continue to force the test grid down to 1.25 from 2.5 mm [0.050 from 0.100 inch]. Fine pitch components may force the test grid down to an even smaller size. Figure 5–1 is a schematic of various lead pitch and test grid combinations. Using a 2.5 mm [0.100 inch] test grid on a 1.25 mm [0.050 inch] pitch component consumes excessive real estate and is impossible on dense SMT designs. A 1.25 mm [0.050 inch] test grid on a 1.25 mm [0.050 inch] pitch component yields the most economical solution in terms of real estate and test node accessibility. Furthermore, it can be seen that Fine Pitch component land patterns can also be developed with the test vias on a 1.25 mm [0.050 in] grid.

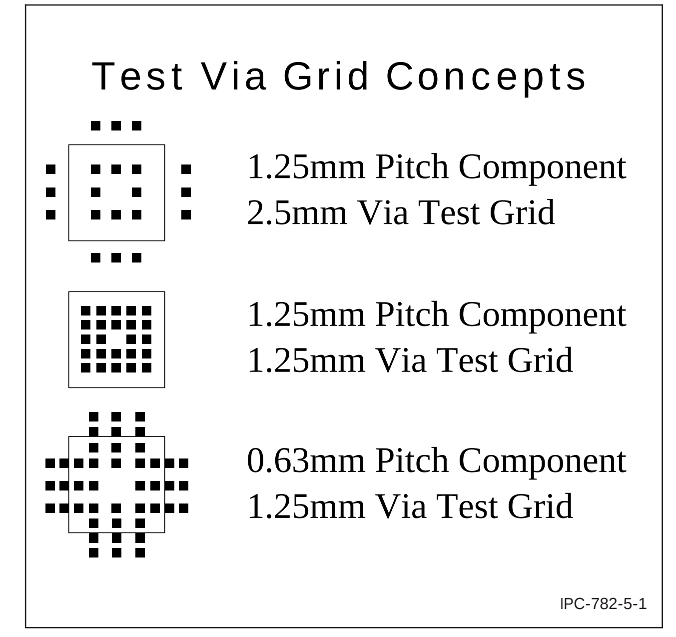


Figure 5–1 Test via grid concepts

For fine pitch components it is good design practice to bring approximately half of the test vias to the inside of the land pattern and the other half to the outside of the land pattern. This accomplishes two objectives: 1) the maximum loading of 100 test points per square inch limitation of all test equipment is not exceeded: and 2) wider distribution of test points reduces the high pressure point areas which cause fixture bowing during vacuum or mechanical actuation.

5.3.1 In-Circuit Test Accommodation Specific via lands and holes can be accessed for automatic in-circuit test (ICT). The via land location for each common network in a circuit is matched to a test probe contact in the test fixture. The test system can then drive each device on the assembly and quickly locate defective devices or identify assembly process problems.

To insure precise alignment of the probe contact pins with the printed board, exact probe position and specific networks must be furnished to the fixture developer. Identifying the test locations as components in the CAD data base will allow for easy transfer of drilling data. This data will reduce fixture development time and eliminate the drilling of excessive, non-functional holes in the fixture base.

5.4 Limited Nodal Access Limited nodal access (less than 100%) still allows the use of ATE bed-of-nails testing, but not as effectively as full nodal access does. As soon as nodal access goes below 100%, shorts, defects and in-circuit testing cannot be performed completely, and so some of these faults will survive to complicate later testing. At bed-of-nails functional test, there will be increased guided probing, because (1) not all shorts, manufacturing defects, and I/C failures were detected earlier, and (2) fewer internal nodes are ‘‘visible’’ through the fixture.

A greater burden is therefore placed on functional or system test to detect and diagnose shorts, defects, and bad devices. This burden varies inversely with the nodal access percentage. The extra effort at functional test may consist of additional recurring manpower cost to diagnose failing boards, or it may mean developing a more detailed functional test (non-recurring cost) than would have been planned otherwise.

5.5 No Nodal Access No nodal access (0%) prohibits bed-of-nails testing and defers all assembly defects and component testing until the functional or system test bed. This can only be cost justified if the much higher cost-per-defect repair is performed so infrequently that the total cost is less than the cost of developing and operating an ATE bed-of-nails test. In other words, the first pass yields must be extremely high to justify this approach.

A very strong quality control program as well as mature manufacturing process controls are required to maintain

this critical parameter. Also, the functional or system test must be capable of at least detecting any fault (even if detection means that the test simply won't run). A possibility in this case is to discard faulty product rather than diagnose it (of course this must be included in the cost analysis).

Another option is that the faulty unit can be debugged by a test technician, but this may also be an expensive proposition, as faults in unscreened boards (no shorts or defects testing) can be very time consuming to diagnose, even for an experienced technician.

5.6 Clam Shell Fixtures Impact Probing the printed board from both sides requires a ''clam shell'' type of fixture. These are expensive, take a long time to fabricate, require larger test lands on the primary side to protect against registration problems due to tolerance stackups. These typically would be 1.25 mm [0.050 in]. This uses up excessive real estate. Also, ''clam shell'' fixtures tend to lose their registration and are difficult to maintain.

5.7 Printed Board Test Characteristics

5.7.1 General Land Pattern Considerations Circuit design for testability refers to the practice of insuring observability and controllability of all nodes by not hard wiring presets or clears, and providing means to break any feedback loops.

Design for testability is as much a part of the schematic design process as it is a part of the board layout process.

Due to the extensive use of ATE to test SMT printed boards, the printed board designer needs to follow the previous rules to provide test node points on the printed board. As SMT Design for Test advances with technology, it is mandatory that continuous improvements to the test process be developed and implemented through Concurrent Engineering.

Ideally, the printed board would have 100% of the nodes accounted for on the secondary side. See Figure 5–2. In-Circuit Testers must have access to at least one node per net. All test lands would be on 2.5 mm [0.100 in] or 1.25 mm [0.050 in] minimum spacings. This allows for the least costly, most reliable, and fastest manufacture of the test fixture.

Lands or vias should be 0.9 to 1.0 mm [0.035 to 0.040 inch] for probing. This via size will ensure less than three misses per 1000 probes. As land sizes decrease, misses increase dramatically as shown in Figure 5–2. The use of square via lands will provide a larger target zone for the test probe to contact. Figure 5–2 demonstrates the additional area that the square land offers. Using the square land, the size may be reduced to 0.8 mm [0.032 in] to increase the spacing between lands if necessary.

The drawbacks to the 1.25 mm grid based test lands are: 1.25 mm [0.050 in] spring probes are more expensive than the cost of 2.5 mm [0.100 in] spring probes. They do not hold up as well in high volume production and the fixture takes longer to manufacture. Also, any vias used as test points should be solder filled for better contact and increased probe life.

5.7.2 Design for Test Parameters The following other considerations are important to the general land pattern design that should be incorporated into the printed board.

- Unplated tooling holes should be available on diagonal corners of the printed board.
- Test lands should be 2.5 mm [0.100 in] minimum from the edge of the printed board to facilitate gasketing on vacuum fixtures.
- When using vias for test points, caution should be taken to insure that signal quality is not degraded at the expense of testing capability.
- Test lands should be 0.63 mm [0.025 in] minimum from mounting land areas.
- It is useful to mark the test vias and lands on an assembly drawing in event of the need to modify the circuit topology. Changes made without moving test lands, avoid fixture modification, saving cost and time.
- When possible, provide numerous test lands for power and ground.
- When possible, provide test lands for all unused gates. Free running gates sometimes cause instability during in-circuit testing. This will provide a means of grounding these spurious signals.
- It is sometimes desirable to provide drive and sense nodes test lands to perform 6-wire bridge measurements during in-circuit test. Direction for this should come from test engineering.
- Caution should be taken when mounting components on the secondary side to avoid covering a via that is a designated test land. Also, if a via is too close to any component, damage may result to the component or fixture during probing. See Figure 5–3.

6.0 PACKAGING AND INTERCONNECTING STRUCTURE TYPES

The selection of a packaging and interconnecting structure for surface mounting applications is important for optimum thermal, mechanical and electrical systems reliability. Each candidate structure has a set of properties with particular advantages and disadvantages when compared to others (see Table 6–1).

It is probable that no one packaging and interconnecting structure or printed board will satisfy all of the needs of the application. Therefore, a compromise of properties should be sought that offers the best ''tailoring'' for component attachment and circuit reliability.

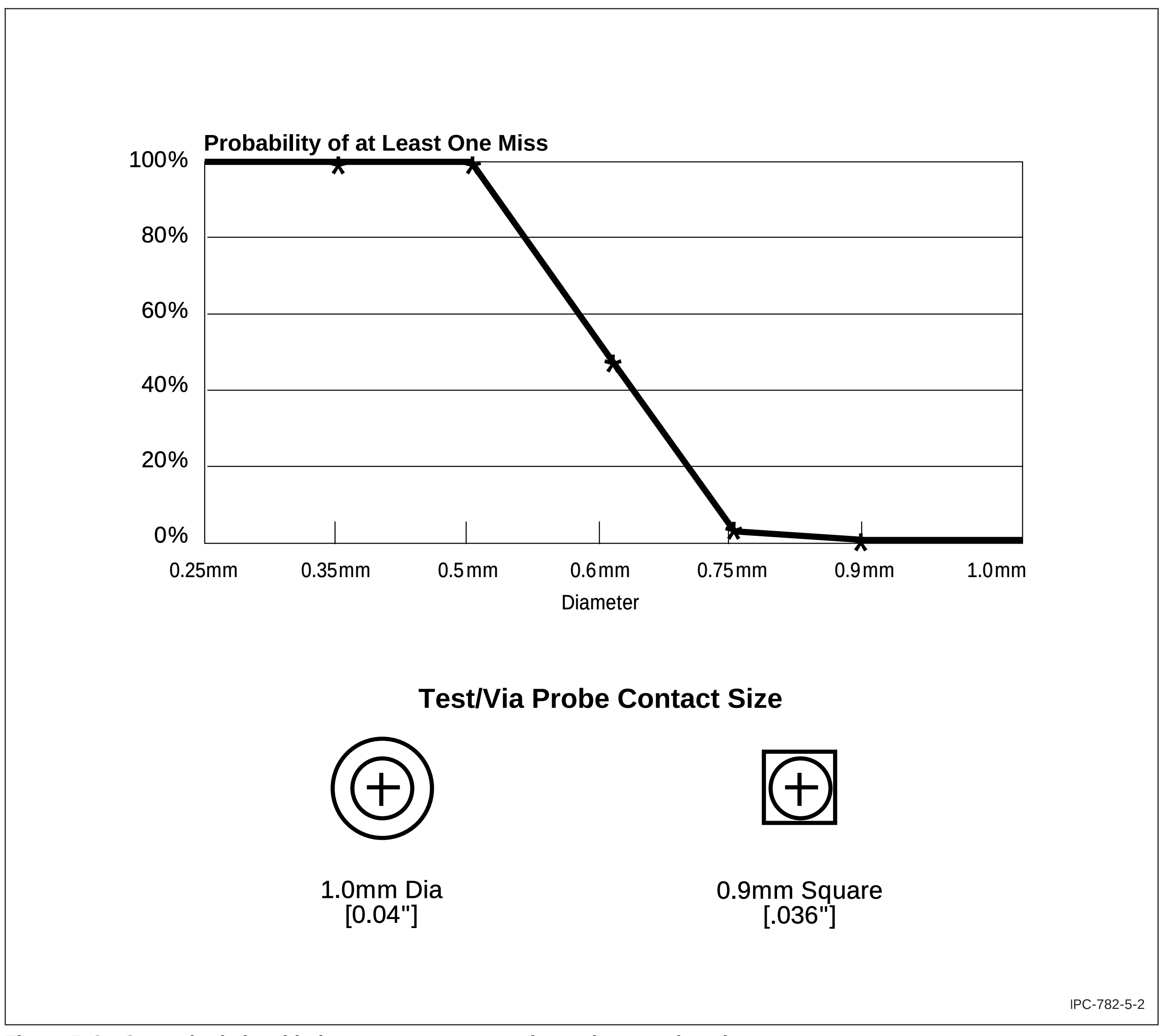


Figure 5–2 General relationship between test contact size and test probe misses

6.1 General Considerations P&I Structures vary from basic printed wiring boards to very sophisticated supporting-core structures. However, some selection criteria are common to all structures. To aid in the selection process, Table 6–2 lists design parameters and material properties which affect system performance, regardless of P&IS type. Also, Table 6–3 lists the properties of the materials most-common for these applications.

6.1.1 Categories In general, a P&I structure will fit into one of four basic categories of construction: organic base material, non-organic base material, supporting plane, and constraining core.

6.1.2 Thermal Expansion Mismatch A primary concern of surface mounted leadless parts is the thermal expansion mismatch between the leadless part and the P&I structure. This mismatch will fracture solder joint interconnections if the assembly is subjected to thermal shock, thermal cycling, power cycling and high operating temperatures. The number of fatigue cycles before solder joint failure depends on the thermal expansion mismatch between the part and the P&I structure, the temperature range over which the assembly must operate, the solder joint thickness, the size of the part and the power cycling. For example, power cycling may cause an undesirable thermal expansion mismatch if a significant temperature difference exists between a chip carrier and the P&I structure.

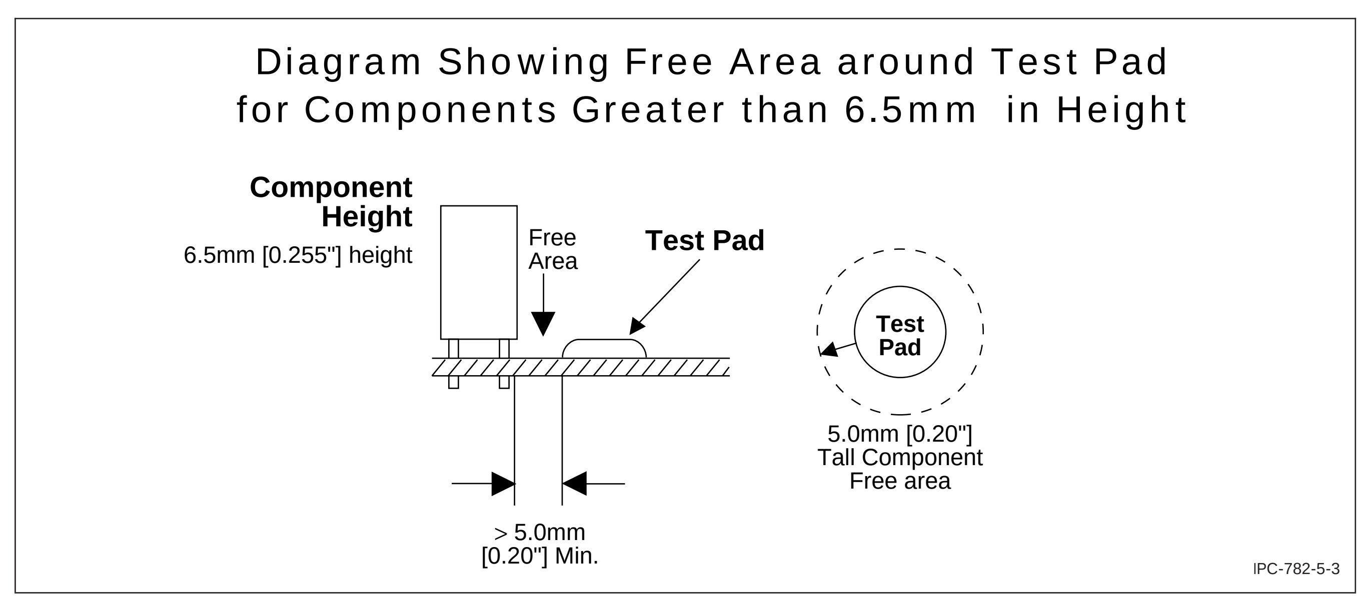


Figure 5–3 Test probe feature distance from component

The acceptable number of cycles can be increased by reducing the thermal expansion mismatch, reducing the temperature gradient, increasing the solder joint height, using the smallest physical size part where possible, and by optimizing the thermal path between the part and P&I structure. The overall systems operating requirements for each class of hardware determines the acceptable number of cycles.

6.2 Organic-Base Material P&IS Organic-base materials work best with leaded chip carriers. With leadless chip carriers, however, the thermal expansion mismatch between package and substrate can cause problems. Also, flatness, rigidity, and thermal conductivity requirements may limit their use. Finally, you must pay attention to package size, I/O count, thermal cycling stability, maximum operating temperature and solder joint compliance.

6.3 Non-Organic Base Materials Non-organic base materials typically used with thick-or thin-film technology are also ideally suited for leaded and leadless chip carrier designs. They can incorporate thick- or thin-film resistors directly on the P&I structure and buried capacitor layers that increase density and improve reliability. However, repairability of the P&I structure is limited. Ceramic materials, usually alumina, appear ideal for P&I structure with leadless ceramic chip carriers because of their relatively-high thermal conductivity (see Table 6–3) and the coefficient of thermal expansion (CTE) match. Unfortunately, the P&I structure is limited to approximately 22,600 sq. mm. [35 square inches]. However, the evolving use of these materials with non-noble metals, such as copper, has attracted both military and commercial applications.

Ceramic P&I structures currently have three applications: ceramic hybrid circuits, ceramic multichip modules (MCM-L) and ceramic printed boards.

6.4 Supporting-Plane P&I Structures Supporting metallic or non-metallic planes can be used with conventional printed boards or with custom processing to enhance P&IS properties. Depending on the results desired, the supporting plane can be electrically-functional or not and can also serve as a structure stiffener, heatsink and/or CTE constraint.

High-density, sequentially-processed, multilayer P&I structures are available with organic dielectrics of specific thickness, ultrafine conductors, and solid plated vias for layer-to-layer interconnections with thermal lands for heat transfer, all connected to a low-CTE metal support heatsink. Thus, this technology combines laminating materials, chemical processing, photolithography, metallurgy, and unique thermal transfer innovations, such that it is also appropriate for mounting and interconnecting bare integrated circuit chips.

The major advantage of this system is that the vias can be as small as 0.20 mm [0.005 inches] square and conductor widths can range from 0.12 to 0.20 mm [0.003 to 0.005 inches] for high interconnection density. Thus, most applications can be satisfied with two signal layers with additional layers for power and ground.

Discrete-wire P&I structures have been developed specifically for use with surface mounted components, as shown in Figure 5–3. These structures are usually built with a low-expansion metal support plane that also offers good heat dissipation.

The interconnections are made by discrete 0.06 mm [0.0025 inch] diameter insulated copper wires precisely placed on a 0.03 mm [inch] grid by numerically-controlled

Table 6–1 Packaging and Interconnecting Structure Comparison

Type	Major Advantages	Major Disadvantages	Comments
Organic Base Substrate Epoxy Fiberglass	Substrate size, weight, reworkable, dielectric properties, conventional board processing	Thermal conductivity, X, Y and Z axis CTE	Because of its high X–Y plane CTE, it should be limited to environments and applications with small changes in temperature and/or small packages.
Polyimide Fiberglass	Same as Epoxy Fiberglass plus high temperature X–Y axis CTE, substrate size, weight, reworkable, dielectric properties, high Tg.	Thermal conductivity, Z-axis CTE, moisture absorption	Same as Epoxy Fiberglass
Epoxy Aramid Fiber	Same as Epoxy Fiberglass, X–Y axis CTE, substrate size, lightest weight, reworkable, dielectric properties	Thermal conductivity, Z-axis CTE, resin microcracking, Z axis CTE, water absorption	Volume fraction of fiber can be controlled to tailor X–Y CTE. Resin selection critical to reducing resin micro-cracks
Polyimide Aramid Fiber	Same as Epoxy Aramid Fiber, X–axis CTE, substrate size, weight, reworkable, dielectric properties	Thermal conductivity, Z–axis CTE, resin microcracking, water absorption	Same as Epoxy Aramid Fiber
Polyimide Quartz (Fused Silica)	Same as Polyimide Aramid Fiber, X–Y axis CTE, substrate size, weight, reworkable, dielectric properties	Thermal conductivity, Z axis CTE, drilling, availability, cost, low resin content required	Volume fraction of fiber can be controlled to tailor X–Y CTE. Drill wearout higher than with fiberglass.
Fiberglass/Aramid Composite Fiber	Same as Polyimide Aramid Fiber, no surface microcracks, Z axis CTE, substrate size, weight, reworkable, dielectric properties	Thermal conductivity, X and Y axis CTE, water absorption, process solution entrapment	Resin microcracks are confined to internal layers and cannot damage external circuitry.
Fiberglass/Teflon® Laminates	Dielectric constant, high temperature	Same as Epoxy Fiberglass, low temperature stability, thermal conductivity, X and Y axis CTE	Suitable for high speed logic applications. Same as Epoxy Fiberglass.
Flexible Dielectric	Light weight, minimal concern to CTE, configuration flexibility	Size, cost, Z-axis expansion	Rigid-flexible boards offer trade-off compromises.
Thermoplastic	3–D configurations, low high-volume cost	High injection-molding setup costs	Relatively new for these applications
Non-Organic Base Alumina (Ceramic)	CTE, thermal conductivity, conventional thick film or thin film processing, integrated resistors	Substrate size, rework limitations, weight, cost, brittle, dielectric constant	Most widely used for hybrid circuit technology
Supporting Plane Printed Board Bonded to Plane Support (Metal or Non-Metal)	Substrate size, reworkability, dielectric properties, conventional board processing, X–Y axis CTE, stiffness, shielding, cooling	Weight	The thickness/CTE of the metal core can be varied along with the board thickness, to tailor the overall CTE of the composite.
Sequential Processed Board with Supporting Plane Core	Same as board bonded to supporting plane	Weight	Same as board bonded to supporting plane.
Discrete Wire	High-speed interconnections. Good thermal and electrical features.	Licensed process. Requires special equipment.	Same as board bonded to low-expansion metal support plane.
Constraining Core Porcelainized Copper Clad Invar	Same as Alumina.	Reworkability, compatible thick film materials.	Thick film materials are still under development.
Printed Board Bonded with Constraining Metal Core	Same as board bonded to low expansion metal cores, stiffness, thermal conductivity, low weight.	Cost, microcracking.	The thickness of the graphite and board can be varied to tailor the overall CTE of the composite.
Compliant Layer Structures	Substrate size, dielectric properties, X–Y axis, CTE.	Z axis CTE, thermal conductivity.	Compliant layer absorbs difference in CTE between ceramic package and substrate.

Table 6–2 P & I Structure Selection Considerations

Design Parameters	Material Properties								
	Transition Temperature	Coefficient of Thermal Expansion	Thermal Conductivity	Tensile Modulus	Flexural Modulus	Dielectric Constant	Volume Resistivity	Surface Resistivity	Moisture Absorption
Temperature & Power Cycling	X	X	X	X					
Vibration				X	X				
Mechanical Shock				X	X				
Temperature & Humidity	X	X				X	X	X	X
Power Density	X		X						
Chip Carrier Size		X		X					
Circuit Density						X	X	X	
Circuit Speed						X	X	X	

Table 6–3 P & I Structure Material Properties

Material	Material Properties							
	Glass Transition Temperature	XY Coefficient of Thermal Expansion	Thermal Conductivity	XY Tensile Modulus	Dielectric Constant	Volume Resistivity	Surface Resistivity	Moisture Absorption
Unit of measure	(°C)	(PPM/°C) (note 4)	(W/M°C)	(PSI x 10^{-6})	(At 1 MHz)	(Ohms/cm)	(Ohms)	(Percent)
Epoxy Fiberglass	125	13–18	0.16	2.5	4.8	10^{12}	10^{13}	0.10
Polyimide Fiberglass	250	12–16	0.35	2.8	4.8	10^{14}	10^{13}	0.35
Epoxy Aramid Fiber	125	6–8	0.12	4.4	3.9	10^{16}	10^{16}	0.85
Polyimide Aramid Fiber	250	3–7	0.15	4.0	3.6	10^{12}	10^{12}	1.50
Polyimide Quartz	250	6–8	0.30		4.0	10^{9}	10^{8}	0.50
Fiberglass/Teflon	75	20	0.26	0.2	2.3	10^{10}	10^{11}	1.10
Thermoplastic Resin	190	25–30		3–4	10^{17}	10^{13}	NA	
Alumina–Beryllia	NA	5–7 21.0	44.0	8.0	10^{14}			
Aluminum (6061 T–6)	NA	23.6	200	10	NA	10^{6}		NA
Copper (CDA101)	NA	17.3	400	17	NA	10^{6}		
Copper-Clad Invar	NA	3–6	150XY/20Z	17–22	NA	10^{6}		NA

Notes:
1. These materials can be tailored to provide a wide variety of material properties based on resins, core materials, core thickness, and processing methods.
2. The X and Y expansion is controlled by the core material and only the Z axis is free to expand unrestrained. Where the Tg will be the same as the reinforced resin system used.
3. When used, a compliant layer will conform to the CTE of the base material and to the ceramic component, therefore reducing the strain between the component and P&I structure.
4. Figures are below glass transition temperature, are dependent on method of measurement and percentage of resin content.

NA = Not Applicable

machines. This geometry results in a low-profile interconnection pattern with excellent high-speed electrical characteristics and a density normally associated with thick-film technology.

6.5 Constraining Core P&I Structures As with supporting- plane P&IS, one or more supporting metallic or non-metallic planes can serve as a stiffener, heatsink, and/or CTE constraint in constraining core P&IS structures.

6.5.1 Porcelainized-Metal (Metal Core) Structures An integral core of low-expansion metal (e.g., copper-clad Invar), can reduce the CTE of porcelainized-metal P&I structures so that it closely matches the CTE of the ceramic chip carrier. Also, the P&I structure size is virtually unlimited. However, the low melting point of the porcelain requires low-firing-temperature conductor, dielectric and resistor inks.

A number of composite P&I structures use leadless components. An integral material with a lower CTE than that of the printed boards controls the CTE of these structures.

7.0 ASSEMBLY CONSIDERATIONS FOR SURFACE MOUNT TECHNOLOGY (SMT)

The smaller size of surface mount components and the option of mounting them on either or both sides of the packaging and interconnecting structure reduces board real estate significantly. The type of SMT assembly is basically determined by the type of surface mount components to be used; see paragraph 3.6.1.5 for a description of types and classes.

This section will briefly discuss the assembly process issues for SMT assemblies. For additional information, see IPC-SM-780 and IPC-CM-770. The reader is also directed to IPC-9191 for continued process improvement.

7.1 SMT Assembly Process Sequence The SMT assemblies are soldered by reflow (vapor phase, infra red, hot air, convection, laser, conduction belt) and/or wave soldering processes depending upon the mix of surface mount and through hole mount components.

The process sequence for Type 2c SMT is shown in Figure 7–1. The leaded components are automatically or hand inserted. The assembly is turned over and adhesive applied. Then the surface mount components are placed by a pick-and-place machine, the adhesive is cured, the assembly is turned over again and the wave soldering process is used to solder both leaded and surface mount components in a single operation. Finally the assembly is cleaned, inspected, repaired if necessary, and tested.

The process sequence for Type 1b SMT is shown in Figure 7–2. Solder paste is applied, components are placed, the assembly is reflow soldered and cleaned. For Type 2b SMT assemblies, the board is turned over and the process sequence just described is repeated.

The process sequence for Type 2c Complex SMT, shown in Figure 7–3, is simply a combination of SMT processes.

7.2 Substrate Preparation Adhesive, Solder Paste

7.2.1 Adhesive Application In wave soldering of SMT, selection and application of adhesive plays a critical role. With too much adhesive, the adhesive gets on lands resulting in poor solder fillets. Too little adhesive will fail to accomplish its objective of holding parts to the bottom of the board during wave soldering.

A good adhesive has desirable properties such as being single part, colored, long shelf life, ease of application, and an adequate bond strength with short cure time. In addition, after curing and soldering, the adhesive should remain moisture resistant, nonconductive, noncorrosive, and be reworkable. There are various companies that supply adhesives for SMT. Some of these adhesives require UV cure followed by IR; others can be cured in IR (infrared) or conventional ovens.

For adhesive cure, temperature plays a bigger role than the time. Only 10°C temperature variation from the recommended cure temperature may cause loss of chips in the wave (under cure) or difficult repair problems (overcure).

7.2.2 Conductive Epoxy Some applications for SMT attachment use conductive epoxy as the attachment material. Adequate conductive epoxy volume is essential at the location of the epoxy on the land.

Unlike solder paste which is redistributed when reflowed, conductive epoxies must be properly controlled to ensure adequate joint strength. Also, component placement must be controlled in order to prevent epoxy squeeze-out, and possible shorts to adjacent lands.

7.2.3 Solder Application, Paste, and Preform Solder paste plays an important role in reflow soldering. The paste acts as an adhesive before reflow. It contains flux, solvent, suspending agent, and alloy of the desired composition. In selecting a particular paste, rheological characteristics such as viscosity, dispensing, screening or stencil, flow, and spread are very important. Susceptibility of the paste to solder ball formation and wetting characteristics are also important.

Solder paste is applied on the lands before component placement either by screening, stenciling, or syringe. Screens are made from stainless steel or polyester wire mesh and stencils are etched stainless steel, brass sheets and other stable alloy

Stencils are preferred for high volume applications. They are more durable than screens, easier to align, and can be used to apply a thicker layer of solder paste.

Solder preforms are sometimes used for through-board-mounted devices. They come in required size and composition, with flux either inside the preforms, or as a coating or without flux. They may be cost effective to avoid wave solder processes if there are only a few leaded components on the board.

7.2.4 Solid Solder Deposition

7.3 Component Placement The accuracy requirements almost make it mandatory to use autoplacement machines for placing surface mount components on the board. Selection of the appropriate autoplacement machine is dictated by the type of parts to be placed and their volume. There are basically four types of autoplacement machines available.

- In-line placement
- Simultaneous placement
- Sequential placement
- Sequential/simultaneous placement

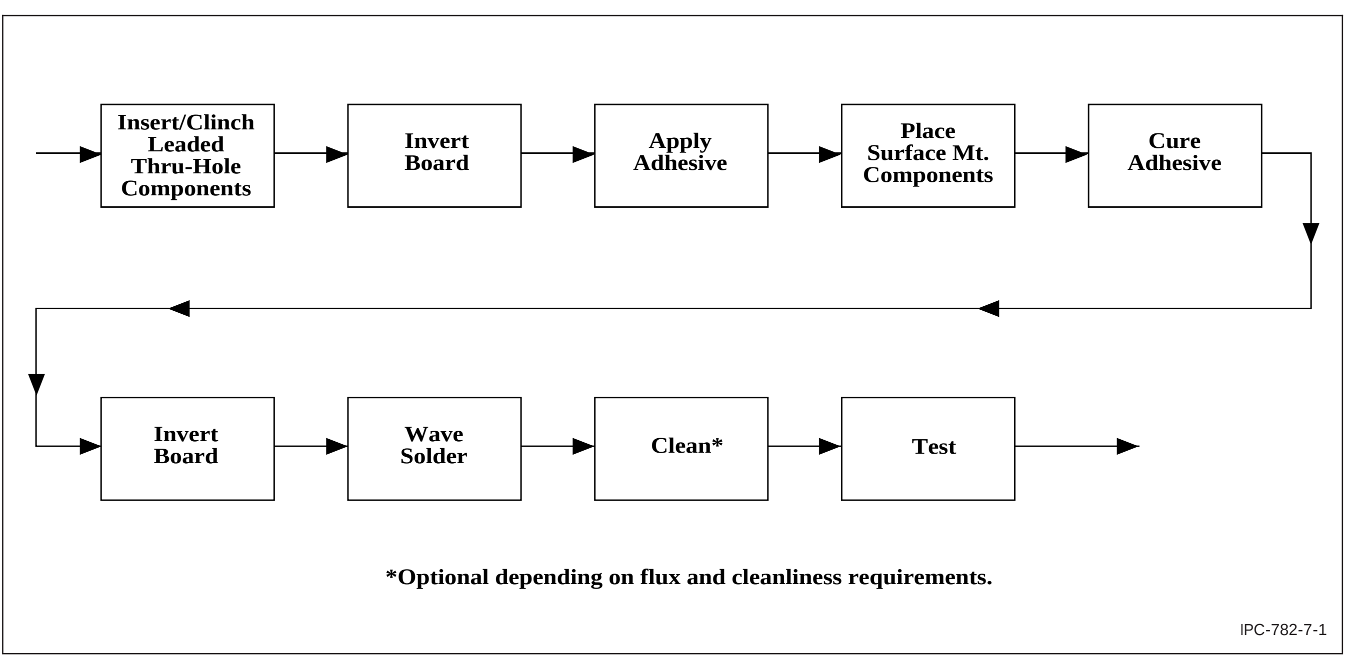


Figure 7–1 Typical process flow for underside attachment type 2c (simple) surface mount technology

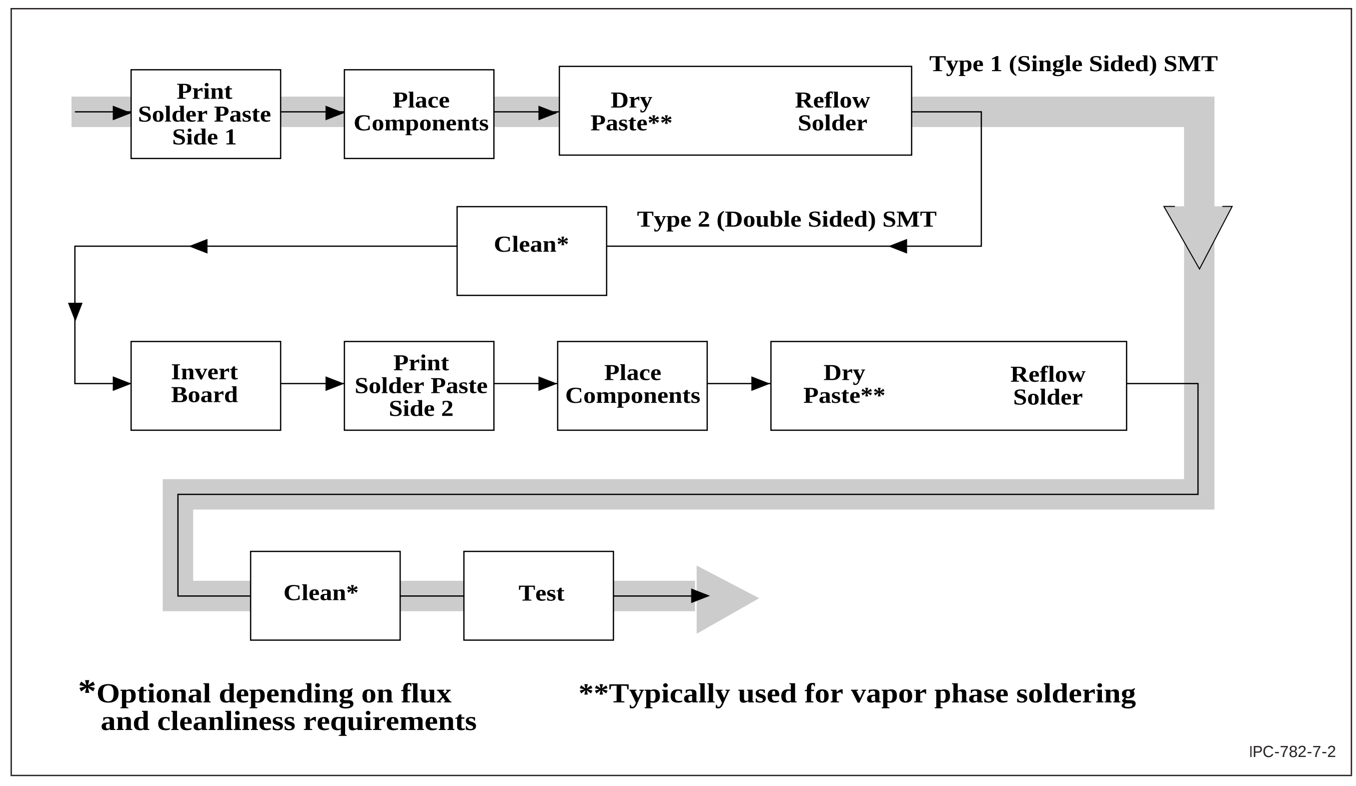


Figure 7–2 Typical process flow for full surface mount type 1b and 2b surface mount technology

In-line placement equipment (Figure 7–4) employs a series of fixed position placement stations. Each station places its respective component as the printed board moves down the line. Cycle times vary from 1.8 to 4.5 seconds per board.

Simultaneous placement equipment (Figure 7–5) places an entire array of components on the printed board at the same time. Typical cycle times vary from 7 to 10 seconds per board.

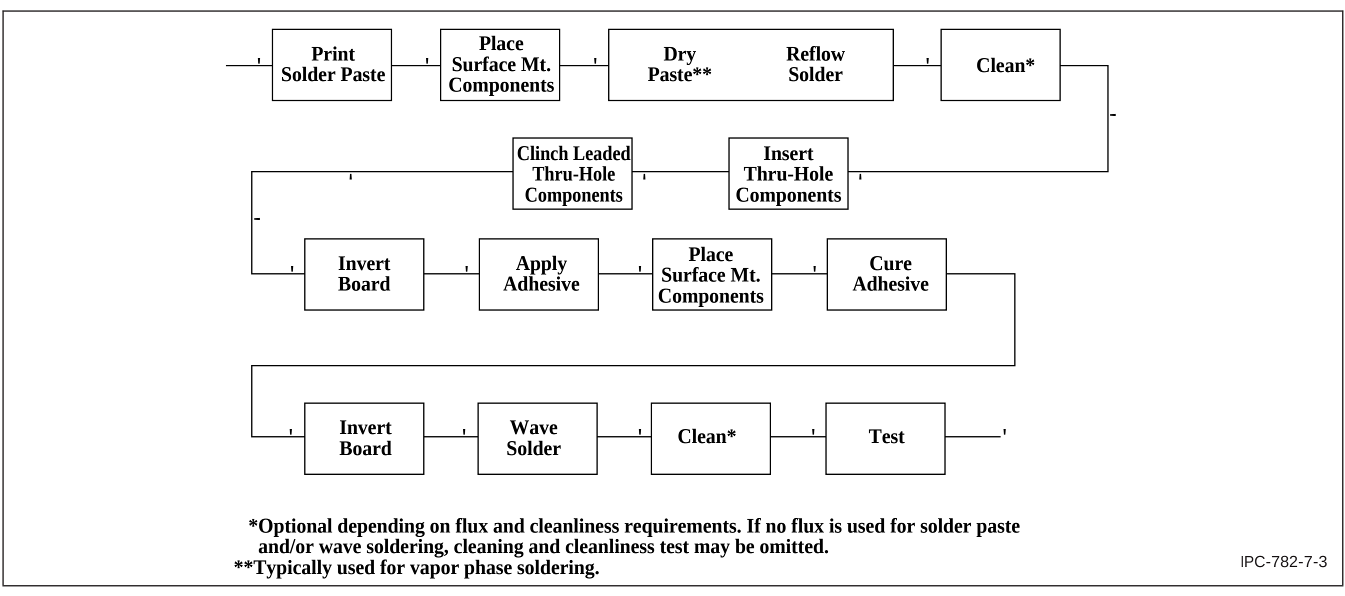


Figure 7–3 Typical process flow for mixed technology type 2c (complex) surface mount technology

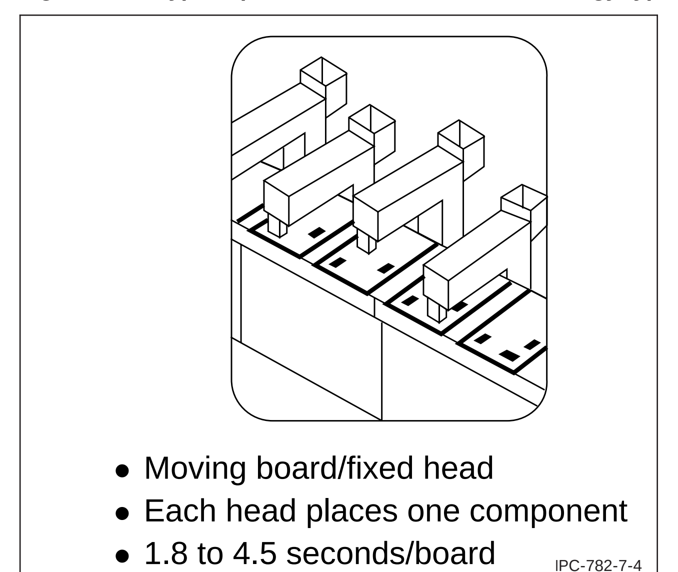


Figure 7–4 In-line placement equipment

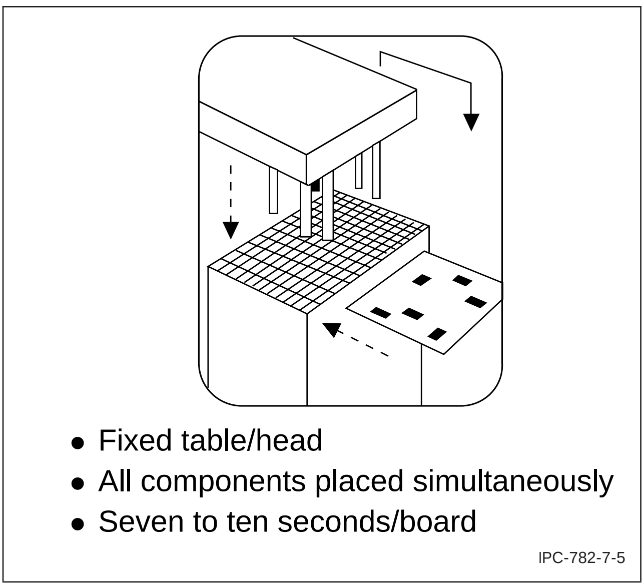


Figure 7–5 Simultaneous placement equipment

Sequential placement equipment (Figure 7–6) typically utilizes a software controlled X-Y moving table system. Components are individually placed on the printed board in succession. Typical cycle times vary from 0.3 to 1.8 seconds per component.

Sequential/simultaneous placement equipment (Figure 7–7) features a software controlled X-Y moving table system. Components are individually placed on the printed board from multiple heads in succession. Simultaneous firing of heads is possible. Typical cycle times vary around 0.2 seconds per component.

There are many autoplacement machines available in each of the four categories. One must establish guidelines for selection of a machine. For example, what kind of parts are to be handled? Will they come in bulk, magazine, or on a tape? Can the machine accommodate future changes in tape sizes?

Selection and evaluation of tapes from various vendors for compatibility with the selected machine is very important. The off-line programming, teach mode, and edit capability along with computer aided design/computer aided manufacture (CAD/CAM) compatibility may be very desirable, especially if a company has already developed a CAD/CAM data base. Special features such as adhesive application, component testing, board handling, and reserve capability for further expansion in a machine may be of special interest for many applications. Reliability, accuracy of placement, and easy maintenance are important to all users.

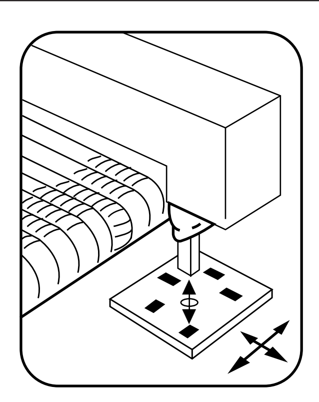


Figure 7–6 Sequential placement equipment

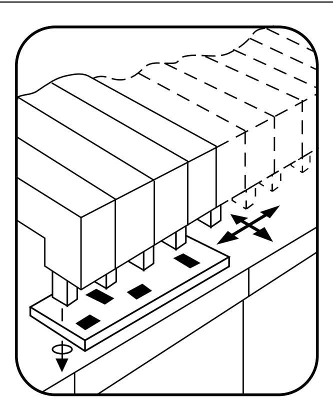


Figure 7–7 Sequential/Simultaneous placement equipment

7.4 Soldering Like the selection of autoplacement machines, the soldering process selection depends upon the type of components to be soldered and whether or not they will be used in combination with leaded parts. For example, if all components are surface mount types, reflow method (vapor phase, hot air convection or infrared) may be desirable. However, for through-hole and surface mount combinations, in mixed technology, a combination of wave soldering and reflow soldering may be used. No process is best for all soldering tasks. In addition, the number of soldering processes discussed in the following text are by no means complete.

7.4.1 Wave Soldering Wave soldering is an economical method of soldering mass terminations. There are four main process variables that must be controlled in the wave soldering process: preheat, fluxing, speed, and solder wave.

In preheat, allowance in the conveyer system must be made for the thermal expansion of the board during preheating and soldering to prevent board warpage.

In fluxing, flux density, activity and flux foam/wave height must be closely monitored. A system must be in place to determine when the flux activity has deteriorated and when the old flux must be replaced and the new flux added.

Speed is the time sequence and duration of all of the steps in soldering. By controlling the speed, more uniform and better joints result. In controlling the conveyer speed, preheating a packaging and interconnecting assembly in two or three stages minimizes the thermal shock damage to the assembly and improves its service life. Uniform preheating is achieved by developing a solder schedule that specifies preheat settings and conveyer speed for each type of board.

The solder wave is an important variable. Wave geometry is especially important for preventing icicles and bridges and for the proper soldering of surface mounted components. Wave geometries include uni- and bidirectional; single and double; rough, smooth and dead zone; oil intermix, dry, and bubbled, and with or without a hot air knife. Special solder waves just for surface mounted components are also available.

The concern generally expressed in wave soldering of surface mount devices is damage to the components when they go through the soldering wave at 260°C [500°F]. The maximum shift in tolerance of resistors and capacitors is generally found to be 0.2%. This is a negligible amount considering the part tolerance of commonly used components is +5 to 20%. The components generally spend about three seconds in the wave but they are designed to withstand soldering temperatures of 260°C [500°F] for up to 10 seconds.

In wave soldering, outgassing and solder skips are two other main concerns. The outgassing or gas evolution occurs on the trailing terminations of chip resistors and capacitors. It is believed to be caused by insufficient drying of flux and can be corrected by raising the packaging and interconnecting assembly preheat temperature or time. The other concern, solder skips, is caused by the shadow effect of the part body on the trailing terminations. Orienting the part in such a way that both terminations are soldered simultaneously solves most shadow effect problems. Some manufacturers use an extra land to serve as a ‘‘solder thief’’ for active components.

The most common method for solving both outgassing and shadow effect is by switching to the dual wave system where the first wave is turbulent and the second wave is

laminar. The turbulent wave serves to provide an adequate amount of solder across the surface of the packaging and interconnecting structure in order to help eliminate outgassing and solder skips. The laminar wave is used to help eliminate icicles and bridging.

7.4.2 Vapor Phase Soldering Vapor phase soldering, also known as condensation soldering, uses the latent heat of vaporization of an inert liquid for soldering. The latent heat is released as the vapor condenses on the part to be soldered. The soldering temperature is constant and is controlled by the type of fluid. Thus, unlike wave, IR, convection and laser soldering, vapor phase soldering does not require control of the heat input to the solder joints or to the board. It heats independent of the part geometry, heats uniformly, and does not exceed the fluid boiling temperature. This process is also suitable for soldering odd-shaped parts, flexible circuits, and pins and connectors, as well as for reflow of tin-lead electroplate and surface mount packages. Since heating is by condensation, the rate of temperature rise depends on the mass of the part. Therefore, the leads on the package in contact with the packaging and interconnecting structure heat up faster than the component body. This may lead to wicking of the solder up the lead.

All these features make vapor phase soldering an easily automated process. It does not necessarily require the fluxing, preheating and soldering adjustments so critical in other process, although prebaking and preheating is recommended to remove moisture and reduce thermal shock in the boards. Vapor phase soldering is amenable to automation but does have process related problems such as a higher incidence of solder balls, part movement, which can be advantageous for alignment, and damage to temperature-sensitive parts.

Both inline and batch type systems are available. The inline system is suitable for mass production. For low volume production or for research and development, a batch process is generally used. For both processes, the major disadvantage is price of the liquid due to vapor loss. The batch process minimizes vapor loss by using a less expensive secondary fluid as a blanket over the primary fluid. Vapor loss does not change, but a cheap vapor is substituted for expensive ones. The cooling coils are used to minimize vapor loss.

7.4.3 IR Reflow In infrared (IR) reflow soldering, the radiant or convective energy is used to heat the assembly. There are basically two types of IR reflow process—focused (radiant) and nonfocused (convective). The latter is proving more desirable for SMT. The focused IR radiates heat directly on the parts and may unevenly heat assemblies. The heat input on the part may also be color dependent. In nonfocused or diffused IR, the heating medium can be air or an inert gas or simply the convection energy. A gradual heating of the assembly is necessary to drive off volatiles from the solder paste. After an appropriate time in preheat, the assembly is raised to the reflow temperature for soldering and then cooled.

7.4.4 Hot Air

7.4.5 Laser Reflow Soldering Laser soldering is a relative newcomer to the soldering technology. It complements other soldering processes rather than replacing them and, as with in-line reflow soldering, it lends itself well to automation. It is faster than hand soldering but not as fast as wave, vapor, IR soldering or hot air convection. Heat-sensitive components that may be damaged in reflow processes can be soldered by laser. Process problems include thermal damage to surrounding areas and solder balls.

7.5 Cleaning Cleaning of surface mount assemblies, in general, is harder than that of conventional assemblies because of smaller gaps between surface mount components and the packaging and interconnecting structure and because of the more complex solder paste residues left on the assembly and under components. The smaller gap may entrap flux which may cause potential reliability problems if the packaging and interconnecting assembly is not properly cleaned. Hence the cleaning process to be used is dependent upon the spacing between component leads, spacing between the components and substrate, the source of the flux residue and the soldering process.

Flux requiring solvent cleaning—synthetic or rosin based fluxes are generally known as synthetic activated (SA), synthetic mildly activated (SMA), rosin activated (RA) or rosin mildly activated (RMA). Stabilized halogenated hydrocarbon/alcohol azeotropes are the preferred solvents for removal of synthetic and rosin based flux residues.

Flux requiring a water clean process—Companies that use organic acid (OA) flux for reflow or wave soldering must filter residue from water before disposal. Residues from OA fluxes are generally removed with water.

Requirements for cleaning are dependent upon the type of equipment as classified in Section 1.3. Some individuals do not clean assemblies used for products; however, assembly performance is predicated on the type of flux being used to assist in the soldering operation.

ANSI/J-STD-001 provides characteristics of various fluxes correlated to cleaning procedures. Users are cautioned to thoroughly understand the corrosive or conductive properties of the flux and flux residue, before making a decision on whether to clean or not to clean based on the end product environment of the equipment.

7.6 Repair/Rework The repair/rework of surface mount assemblies requires special care. Because of the small land geometries, heat applied to the board should be minimized.

There are various tools available for removing components. Resistance heating tweezers are also used for removing surface mounted components. Various types of hot air/gas and IR systems are also used for removing surface mounted components. One of the main issues when using hot air/gas devices is preventing damage to adjacent components.

No matter which system tool is used, all the controlling desoldering/soldering variables, such as number of times a component can be removed and replaced, desoldering temperature and time, and damage to the packaging/interconnection assembly, need to be addressed.

Land Pattern Details

The information in the following sections is intended to represent requirements for families of surface-mountable components that have been standardized by standard developers throughout the world (e.g., EIA, JEDEC, and EIAJ). The principles used in the data embody the concepts of ''design for manufacturability,'' and specify criteria for analysis or modification in order to make the manufacturing process as robust as possible.

Each component family type has been organized into a four-page set that has its own number identification (a paragraph number of the mother document—IPC-SM-782) and its own revision status. As changes are necessary (the addition or deletion of information, or corrections to modify the text or numerical data), a four-page signature(s) will be reissued as a set for replacement in this handbook.

A summary of the contents with revision status is provided at the conclusion of this explanation.

Introduction

Page 1 of each data set (four-page signature) provides general information about the part, its usage or performance requirements, and techniques for handling the attachment of the component. Any useful information about the particular component type is detailed on this introductory page.

Component Dimensions

Page 2 of each data set describes the critical component dimensions necessary to make judgements for reliable mounting recommendations. The standards organizations provide many more dimensions to define the requirements for manufacturing the specific components in a family class; only those dimension that are necessary for land pattern development are repeated on page 2 of each data set.

Every attempt has been made to check and correlate the dimensions used against the published standard. Unfortunately, the standards do not always provide adequate information, or full disclosures of maximum and least material conditions of the component dimensions used in land pattern development. At times, the numbers shown in the data set have been enhanced (nominal dimensions converted to maximum/minimum dimensions), at times the numbers shown have been derived (terminal dimensions subtracted from an overall dimension with their inherent tolerances considered in an RMS condition), and at other times the dimensions have been tailored (total tolerances spread between maximum/minimum limits reduced to a reasonable amount) in order to facilitate a producible land pattern and assembly.

Users are encouraged to check with their component suppliers in order to ascertain that the suppliers certify to the numbers used on page 2 in order to use the registered land patterns on page 3. In the event of disparities, if they are component-supplier specific, users are encouraged to modify their use of the land patterns shown on page 3 in accordance with the principles outlined in Section 3.3 on the registered land patterns dimensioning system. If the disparities are industry specific, please inform the IPC using the form at the end of this section to initiate a data set change.

Land Pattern Dimensions

Page 3 of the data set provides the details for the land pattern. Since the design concepts are dedicated to establishing the most favorable solder joint conditions, all land pattern dimensions are shown at maximum material condition (MMC). This is the ''target value'' for the board manufacturer; moving away from MMC to the least material condition (LMC) reduces the opportunity for formation of the optimum solder fillet. The LMC dimensions should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

In addition to specifying maximum and minimum limits, the resultant land width is provided as a reference (dimension ''Y''). Designers are encouraged to incorporate the MMC conditions into their library symbols, and when sending electronic data to their board manufacturer they should identify that the data is at MMC. Specifying minimum conductor width as a manufacturing goal should be avoided, since the manufacturer is compensating and scaling data to accommodate process allowances in the phototool, and is concentrating on meeting minimum requirements. This is opposite to the desire to have robust land patterns which should be at maximum material conditions.

Page 3 also provides an area around the land pattern known as the ''grid courtyard.'' The description is in the 0.05 mm elements of the international grid. An area described as 4x6 is equal to 2.00 mm by 3.00 mm. When placing parts on a printed board, the highest density is when one courtyard touches another. Courtyards are intended to encompass the land pattern and a component body that is centered on the land pattern.

Tolerance Analysis

Page 4 shows the details of the tolerance analysis of the component and land pattern shown in the data set. The first two columns of the table show the board fabrication allowances in the analysis; the second column shows the allowances used to represent placement registration in terms of DTP (diameter of true position), with the point of origin being the center of the land pattern.

The next part of the analysis provides three pieces of information for the toe fillet, heel fillet, and side fillet. The first part of the set is the range of differences between maximum and minimum component dimensions. These are: the overall dimension (usually ''L'') identified as ''C''; the inside dimension l (usually ''S'') identified as ''C''; and the side or lead width s (usually ''W'') identified as ''C.'' The second and third columns w of each triplet set show the minimum and maximum statistically derived solder fillet opportunity. These two columns become the upper and lower specification limits for any statistical process control (SPC) analysis. If these conditions are not met, something has shifted in the process, or the parts being assembled in the process.

Revision Status

The following is the revision status of the component family data sets of IPC-SM-782A. A dash (''-'') signifies that the section is the original release; the letter ''A'' after the section number refers to the first revision to the four-page set; the letter ''B'' refers to the second revision, etc.

Section Number	*Revision Status*	*Section Title*
8.0	—	Discrete Components
8.1	A	Chip Resistors
8.2	A	Chip Capacitors
8.3	—	Inductors
8.4	A	Tantalum Capacitors
8.5	A	Metal Electrode Face (MELF) Components
8.6	—	Small Outline Transistor (SOT) 23
8.7	—	Small Outline Transistor (SOT) 89
8.8	A	Small Outline Diode (SOD) 123
8.9	—	Small Outline Transistor (SOT) 143
8.10	—	Small Outline Transistor (SOT) 223
8.11	A	Modified Through-Hole Component (TO) 252
9.0	—	Components with Gullwing Leads on Two Sides
9.1	A	Small Outline Integrated Circuits (SOIC)
9.2	A	Small Outline Integrated Circuits (SSOIC)
9.3	A	Small Outline Package Integrated Circuit (SOPIC)
9.4	A	Thin Small Outline Package
9.5	—	Ceramic Flat Pack (CFP)
10.0	—	Components with J Leads on Two Sides
10.1	A	Small Outline Integrated Circuits with J Leads (SOJ)—7.63 mm [0.300] Body Size
10.2	—	Small Outline Integrated Circuits with J Leads (SOJ)—8.88 mm [0.350] Body Size
10.3	—	Small Outline Integrated Circuits with J Leads (SOJ)—10.12 mm [0.400] Body Size
10.4	—	Small Outline Integrated Circuits with J Leads (SOJ)—11.38 mm [0.450] Body Size
11.0	—	Components with Gullwing Leads on Four Sides
11.1	A	Plastic Quad Flat Pack (PQFP)
11.2	A	Shrink Quad Flat Pack (SQFP), Square
11.3	A	Shrink Quad Flat Pack (SQFP), Rectangular
11.4	A	Ceramic Quad Flat Pack (CQFP)
12.0	—	Components with J Leads on Four Sides
12.1	A	Plastic Leaded Chip Carrier (PLCC), Square
12.2	A	Plastic Leaded Chip Carrier (PLCC), Rectangular
12.3	—	Leadless Ceramic Chip Carrier (LCC)
13.0	—	Modified Dual-In-Line Pin (DIP) Components
13.1	—	DIP
14.0	–	Components with Ball Grid Array Contacts
14.1	–	Plastic Ball Grid Array
14.2	–	1.27 mm Pitch Rectangular PBGA JEDEC MS-028



IPC-SM-782

Surface Mount Design and Land Pattern Standard

Date	Section
8/93	8.0
Revision	Subject
	Discrete Components

1.0 INTRODUCTION

This section covers land patterns for various discrete components. Each subsection contains information in accordance with the following format:

1.0 Scope
2.0 Applicable Documents
3.0 General Component Description (Figure 1)
4.0 Component Dimensions (Figure 2)
5.0 Land Pattern Dimensions (Figure 3)
6.0 Tolerance and Solder Joint Analysis (Figure 4)

The following is the table of contents for this section:

Table of Contents

2.0 APPLICABLE DOCUMENTS

The following documents, of the issue in effect on the revision date of this section, form a part of this specification to the extent specified herein.

2.1 Electronic Industries Association (EIA)[1]

EIA-PDP-100 Registered and Standard Mechanical Outlines for Electronic Parts

EIA-481-A Taping of Surface Mount Components for Automatic Placement

EIA-481-1 8 mm and 2 mm Taping of Surface Mount Components for Automatic Handling

EIA-481-2 16 mm and 24 mm Embossed Carrier Taping of Surface Mount Components for Automated Handling

EIA-481-3 32 mm, 44 mm, and 56 mm Embossed Carrier Taping of Surface Mount Components for Automated Handling

2.2 International Electrotechnical Commission (IEC)[2]

IEC 97 Grid System for Printed Circuits

3.0 GENERAL INFORMATION

3.1 Packaging Discrete components are generally purchased in 8 mm and 12 mm wide tape and reel. See Figure 1. EIA-481 is the applicable specification for tape and reel. Consult your manufacturers guide for the packaging availability of your component.

Parts susceptible to damage by electrostatic discharge shall be supplied in a manner that prevents such damage. Tape peel strength shall be 40 ±30 grams. Peel from the top for the top cover of the tape. Reel materials used in the construction of the reel shall be easily disposable metal, chip board, styrene plastic or equivalent. Reels shall not cause deterioration of the components or their solderability. Reels must be able to withstand high humidity conditions.

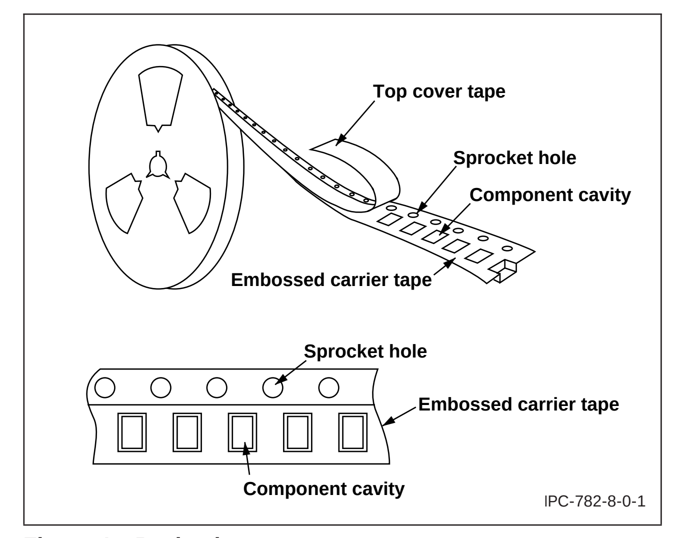


Figure 1 Packaging

3.2 Resistance to Cleaning Processes Parts must be capable of withstanding cleaning processes currently used by board assembly manufacturers. This may include as a minimum 4-minute exposures to solvent cleaning solutions at 40°C, plus a minimum of a 1-minute exposure to ultrasonic immersion at a frequency of 40 kHz and a power of 100 watts per square foot. Alkaline systems in use shall also not damage parts or remove markings.

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1. Application for copies should be addressed to EIA, 2001 Pennsylvania Ave N.W., Washington, DC, 20006-1813 or Global Engineering Documents, 1990 M St. N.W., Washington, DC 20036.
2. Application for copies should be addressed to IEC, 3 rue de Varembe, PO Box 131—1211 Geneva 20, Switzerland



IPC-SM-782

Surface Mount Design and Land Pattern Standard

Date	Section
5/96	8.1
Revision	Subject
A	Chip Resistors

1.0 SCOPE

Microminiature leadless devices are available to the circuit designer in rectangular form for discrete components such as chip resistors.

This subsection provides the component and land pattern dimensions for chip resistors, along with an analysis of tolerance and solder joint assumptions used to arrive at the land pattern dimensions. Basic construction of the chip resistor is also covered.

2.0 APPLICABLE DOCUMENTS

See Section 8.0 for documents applicable to the subsections.

3.0 COMPONENT DESCRIPTIONS

A variety of values exist for resistors. The following sections describe the most common types.

3.1 Basic Construction The resistive material is applied to a ceramic substrate and terminated symmetrically at both ends with a ‘‘wrap around’’ metal U-shaped band. The resistive material is face-up, thus trimming to close tolerances is possible. Since most equipment uses a vacuum-type pickup head, it is important that the surface of the resistor is made flat after trimming, otherwise vacuum pickup might be difficult. See Figure 1.

3.1.1 Termination Materials End terminations should be solder coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the termination by hot dipping or by plating from solution. Plated solder terminations should be subjected to a post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in.] thick.

The termination shall be symmetrical, and shall not have nodules lumps, protrusions, etc., that compromise the symmetry or dimensional tolerances of the part. The end termination shall cover the ends of the components, and shall extend out to the top and bottom of the component.

Solder finish applied over precious metal electrodes shall have a diffusion-barrier layer between the electrode metalization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick.

3.1.2 Marking Resistors equal to or larger than 2012 [0805] are labeled. Resistors smaller than 1608 [0603] are generally unlabeled.

3.1.3 Carrier Package Format Bulk rods, 8 mm tape/4 mm pitch is preferred for best handling. Tape and reel specifications provide additional requirements.

3.1.4 Resistance to Soldering Parts should be capable of withstanding five cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260°C.

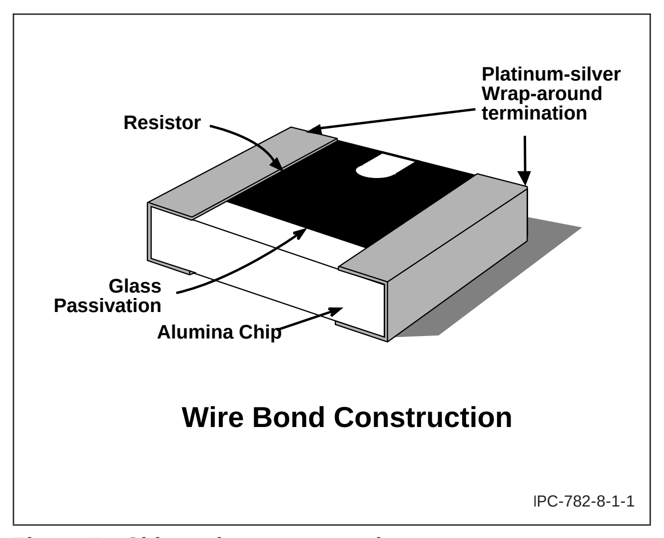
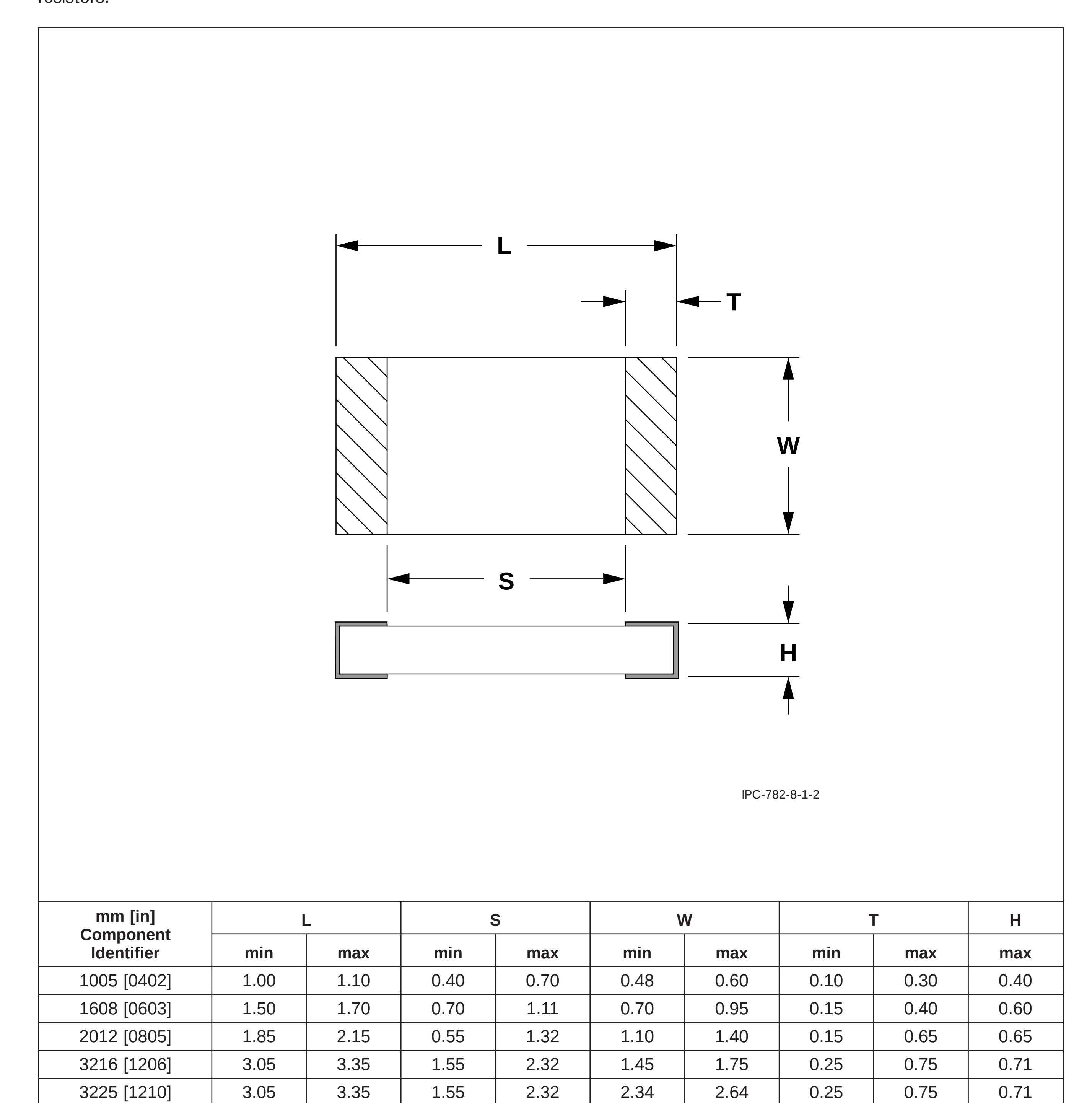


Figure 1 Chip resistor construction

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for chip resistors.



mm [in] Component Identifier	L		S		W		T		H
	min	max	min	max	min	max	min	max	max
1005 [0402]	1.00	1.10	0.40	0.70	0.48	0.60	0.10	0.30	0.40
1608 [0603]	1.50	1.70	0.70	1.11	0.70	0.95	0.15	0.40	0.60
2012 [0805]	1.85	2.15	0.55	1.32	1.10	1.40	0.15	0.65	0.65
3216 [1206]	3.05	3.35	1.55	2.32	1.45	1.75	0.25	0.75	0.71
3225 [1210]	3.05	3.35	1.55	2.32	2.34	2.64	0.25	0.75	0.71
5025 [2010]	4.85	5.15	3.15	3.92	2.35	2.65	0.35	0.85	0.71
6332 [2512]	6.15	6.45	4.45	5.22	3.05	3.35	0.35	0.85	0.71

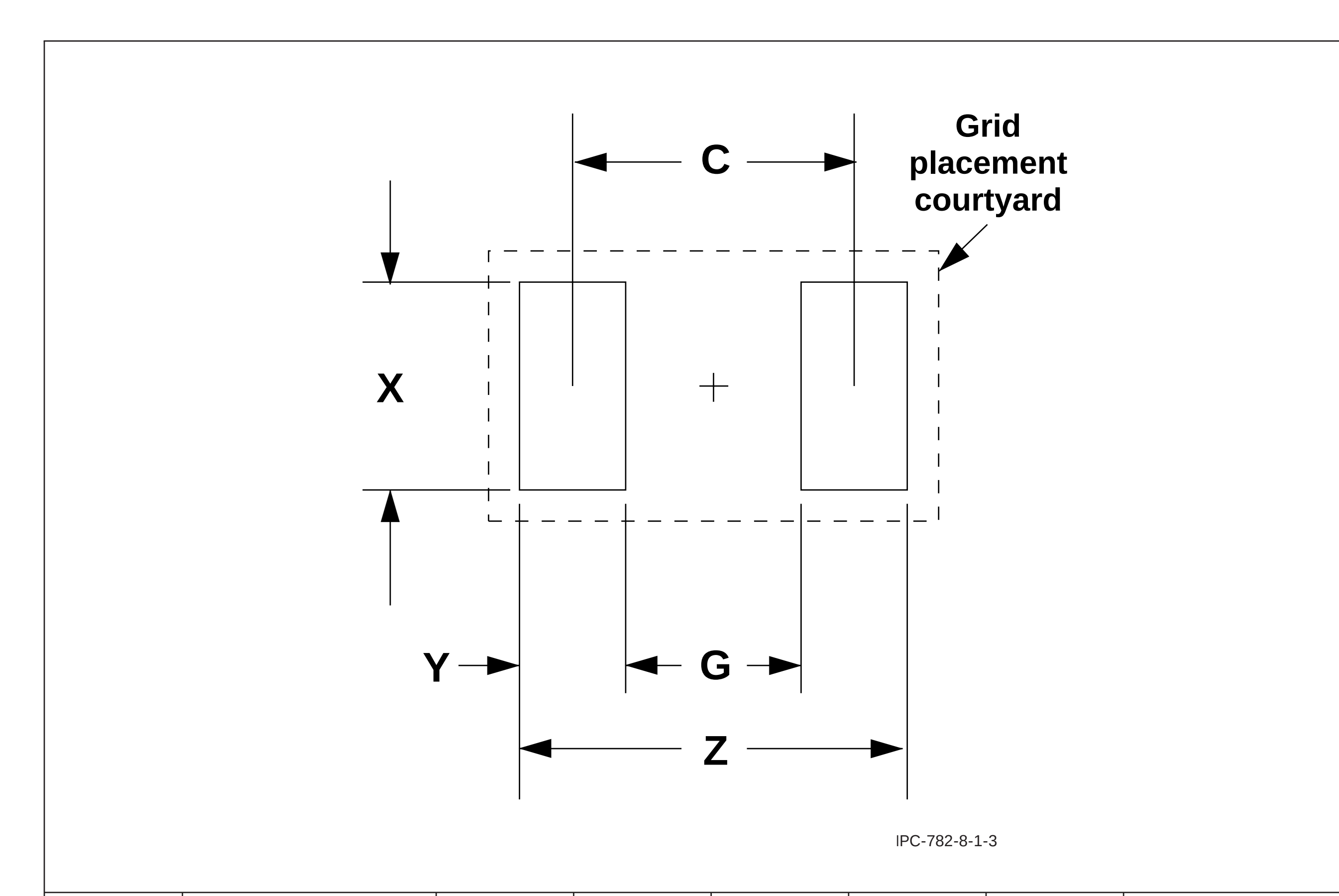
Figure 2 Chip resistor component dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for chip resistors. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



RLP No.	Component Identifier (mm) [in.]	Z (mm)	G (mm)	X (mm)	Y (mm) ref	C (mm) ref	Placement Grid (No. of Grid Elements)
100A	1005 [0402]	2.20	0.40	0.70	0.90	1.30	2x6
101A	1608 [0603]	2.80	0.60	1.00	1.10	1.70	4x6
102A	2012 [0805]*	3.20	0.60	1.50	1.30	1.90	4x8
103A	3216 [1206]*	4.40	1.20	1.80	1.60	2.80	4x10
104A	3225 [1210]*	4.40	1.20	2.70	1.60	2.80	6x10
105A	5025 [2010]*	6.20	2.60	2.70	1.80	4.40	6x14
106A	6332 [2512]*	7.40	3.80	3.20	1.80	5.60	8x16

**Note:* If a more robust pattern is desired for wave soldering devices larger than 1608 [0603], add 0.2 mm to the Y-dimension, and consider reducing the X-dimension by 30%. Add a ‘‘W’’ suffix to the number; e.g., 103W.

Figure 3 Chip resistor land pattern dimensions

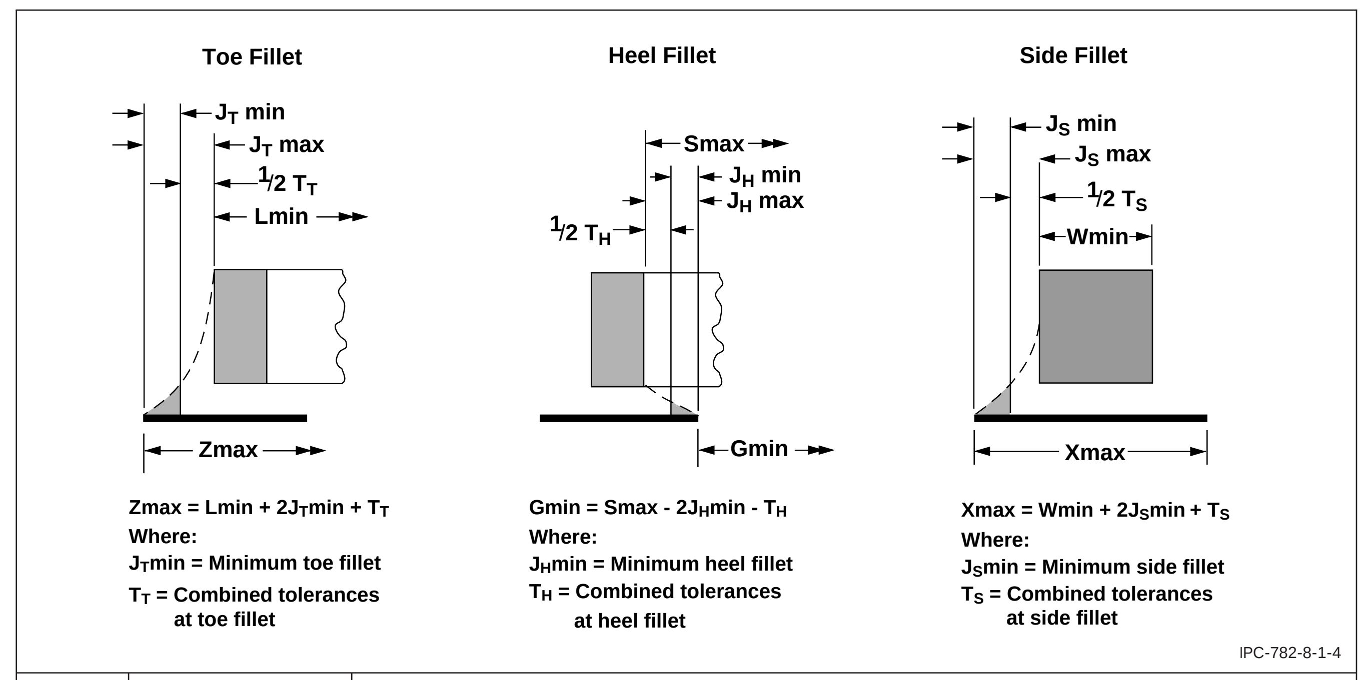
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed, and are given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions.)

The dimensions for the statistical minimum and maximum solder joint fillets at the toe, heel, or side (J_T, J_H, or J_S) have been determined based on the equations detailed in Section 3.3. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



RLP No.	Tolerance (mm) Assumptions		Solder Joint: Toe (mm)			Heel (mm)			Side (mm)		
	F	P	C_L	J_{Tmin}	J_{Tmax}	C_S	J_{Hmin}	J_{Hmax}	C_W	J_{Smin}	J_{Smax}
100A	0.10	0.10	0.10	0.51	0.60	0.30	–0.02	0.15	0.12	0.02	0.11
101A	0.10	0.10	0.20	0.53	0.65	0.41	0.04	0.25	0.25	0.01	0.15
102A	0.10	0.10	0.30	0.51	0.68	0.77	–0.03	0.36	0.30	0.03	0.20
103A	0.10	0.10	0.30	0.51	0.68	0.77	0.17	0.56	0.30	0.01	0.18
104A	0.10	0.10	0.30	0.51	0.68	0.77	0.17	0.56	0.30	0.01	0.18
105A	0.10	0.10	0.30	0.51	0.68	0.77	0.27	0.66	0.30	0.01	0.18
106A	0.10	0.10	0.30	0.46	0.63	0.77	0.32	0.71	0.30	–0.09	0.08

Figure 4 Tolerance and solder joint analysis

Surface Mount Design and Land Pattern Standard

1.0 SCOPE

Microminiature leadless devices are available to the circuit designer in rectangular form for discrete components such as chip capacitors.

This subsection provides the component and land pattern dimensions for chip capacitors, along with an analysis of tolerance and solder joint assumptions used to arrive at the land pattern dimensions. Basic construction of the chip capacitor is also covered.

2.0 APPLICABLE DOCUMENTS

See Section 8.0 for documents applicable to the subsections.

3.0 COMPONENT DESCRIPTIONS

A variety of values exist for capacitors. The following sections describe the most common types.

3.1 Basic Construction Multilayer ceramic capacitors use substrate materials such as alumina for hybrid circuits and porcelainized metal. The monolithic construction used in producing these chips results in a solid block of ceramic with an enclosed electrode system and metallized ends for circuit attachment. This solid block is rugged and capable of withstanding the harsh environment and treatment associated with manufacturing processes. See Figure 1.

Electrodes are given a common terminal by coating the chip ends with a precious metal-glass formulation suspended in an organic vehicle. Consecutive drying and firing eliminates the organic components and effects a bond between the ceramic dielectric and glass constituent in the termination.

3.1.1 Termination Materials End terminations should be solder coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the termination by hot dipping or by plating from solution. Plated solder terminations should be subjected to a post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

The termination shall be symmetrical, and shall not have nodules lumps, protrusions, etc., that compromise the symmetry or dimensional tolerances of the part. The end termination shall cover the ends of the components, and shall extend out to the top and bottom of the component.

Most common termination materials include palladium-silver alloy, silver, and gold. Solder finish applied over precious metal electrodes shall have a diffusion-barrier layer between the electrode metallization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick.

3.1.2 Marking Ceramic capacitors are typically unmarked.

3.1.3 Carrier Package Format Bulk rods, 8 mm tape/4 mm pitch is preferred for best handling. Tape and reel specifications provide additional requirements.

3.1.4 Resistance to Soldering Parts should be capable of withstanding five cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260°C.

Caution should be exercised when using the 4564 (1825) capacitor mounted on organic substrates due to CTE mismatch if the assembly sees wide temperature swings in the assembly process or end use.

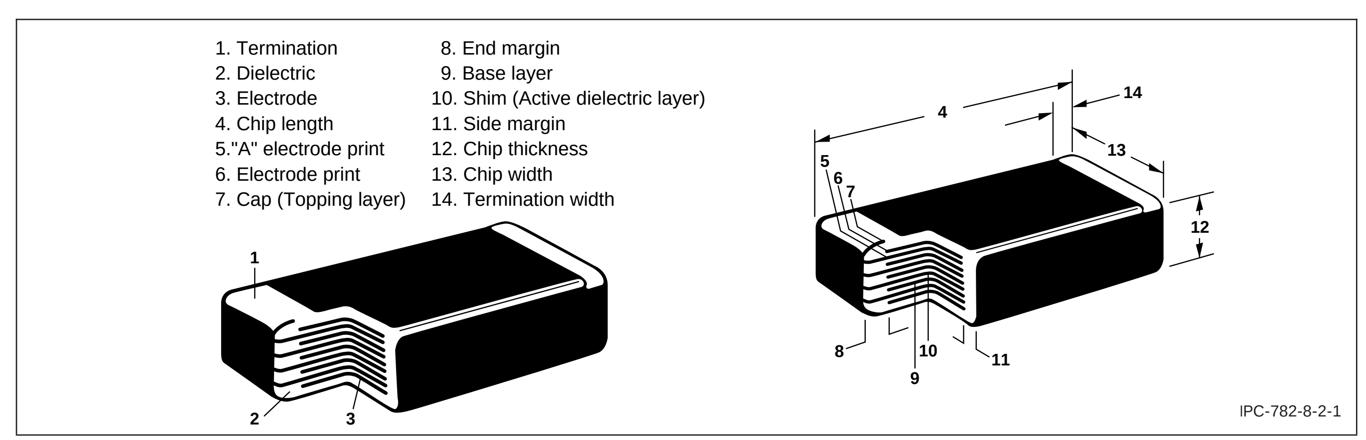
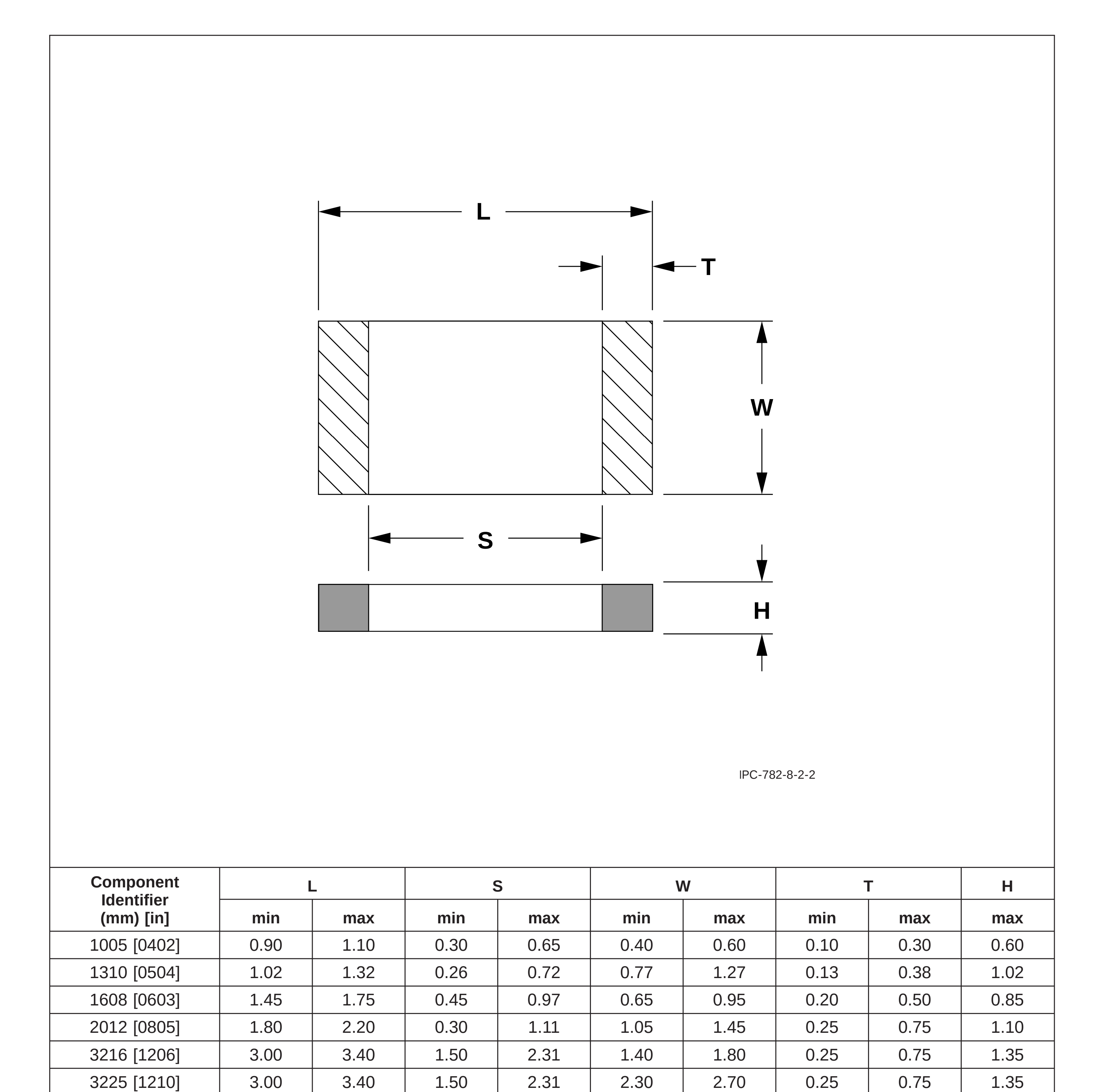


Figure 1 Chip capacitor construction

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for chip capacitors.



Component Identifier (mm) [in]	L		S		W		T		H
	min	max	min	max	min	max	min	max	max
1005 [0402]	0.90	1.10	0.30	0.65	0.40	0.60	0.10	0.30	0.60
1310 [0504]	1.02	1.32	0.26	0.72	0.77	1.27	0.13	0.38	1.02
1608 [0603]	1.45	1.75	0.45	0.97	0.65	0.95	0.20	0.50	0.85
2012 [0805]	1.80	2.20	0.30	1.11	1.05	1.45	0.25	0.75	1.10
3216 [1206]	3.00	3.40	1.50	2.31	1.40	1.80	0.25	0.75	1.35
3225 [1210]	3.00	3.40	1.50	2.31	2.30	2.70	0.25	0.75	1.35
4532 [1812]	4.20	4.80	2.30	3.46	3.00	3.40	0.25	0.95	1.35
4564 [1825]	4.20	4.80	2.30	3.46	6.00	6.80	0.25	0.95	1.10

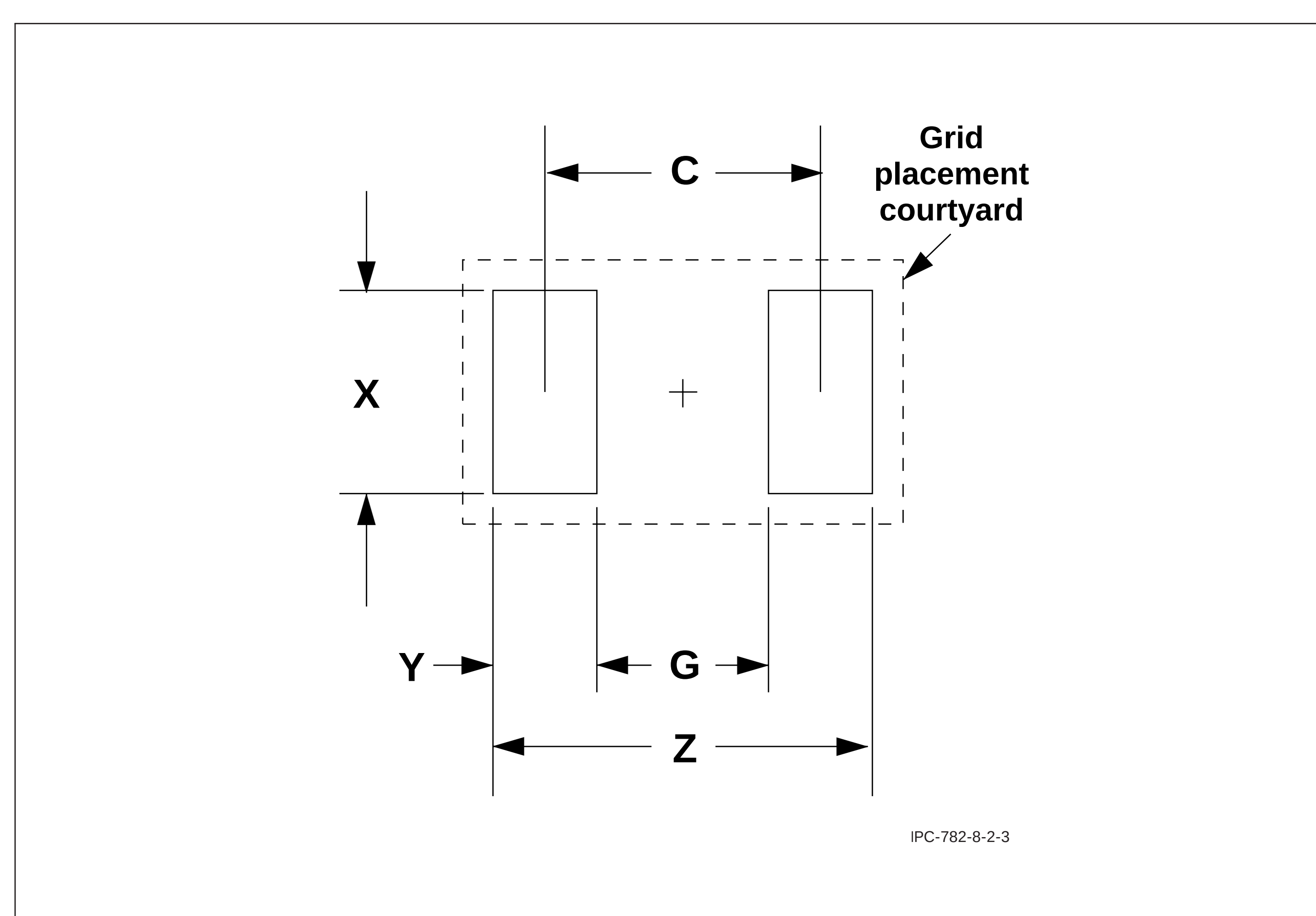
Figure 2 Chip capacitor component dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for chip capacitors. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



RLP No.	Component Identifier (mm) [in]	Z (mm)	G (mm)	X (mm)	Y ref	C ref	Placement Grid (No. of Grid elements)
130A	1005 [0402]	2.20	0.40	0.70	0.90	1.30	2x6
131A	1310 [0504]	2.40	0.40	1.30	1.00	1.40	4x6
132A	1608 [0603]	2.80	0.60	1.00	1.10	1.70	4x6
133A	2012 [0805]	3.20	0.60	1.50	1.30	1.90	4x8
134A	3216 [1206]	4.40	1.20	1.80	1.60	2.80	4x10
135A	3225 [1210]	4.40	1.20	2.70	1.60	2.80	6x10
136A	4532 [1812]	5.80	2.00	3.40	1.90	3.90	8x12
137A	4564 [1825]	5.80	2.00	6.80	1.90	3.90	14x12

Figure 3 Chip capacitor land pattern dimensions

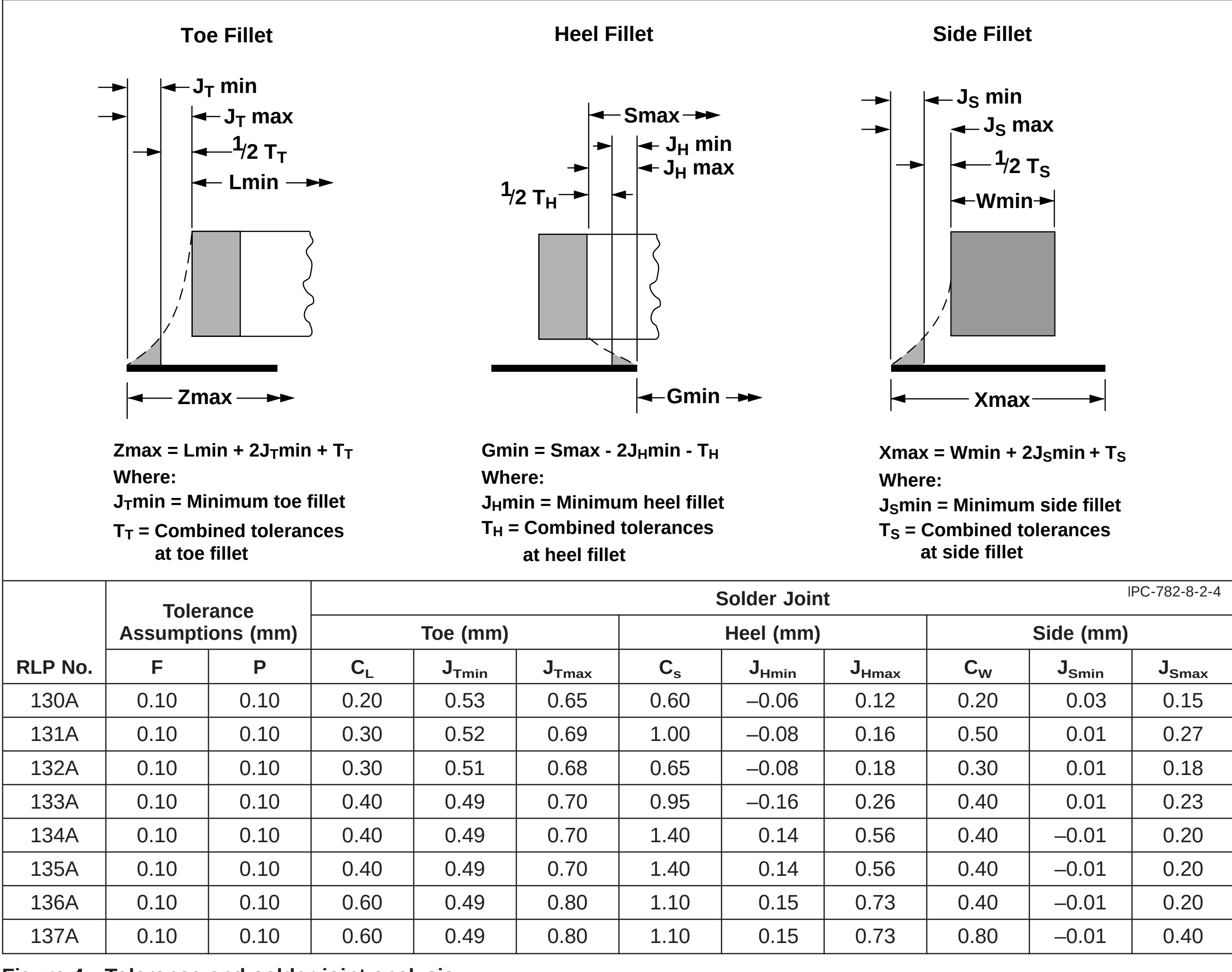
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



RLP No.	Tolerance Assumptions (mm)		Solder Joint: Toe (mm)			Heel (mm)			Side (mm)		
	F	P	C_L	J_{Tmin}	J_{Tmax}	C_s	J_{Hmin}	J_{Hmax}	C_W	J_{Smin}	J_{Smax}
130A	0.10	0.10	0.20	0.53	0.65	0.60	–0.06	0.12	0.20	0.03	0.15
131A	0.10	0.10	0.30	0.52	0.69	1.00	–0.08	0.16	0.50	0.01	0.27
132A	0.10	0.10	0.30	0.51	0.68	0.65	–0.08	0.18	0.30	0.01	0.18
133A	0.10	0.10	0.40	0.49	0.70	0.95	–0.16	0.26	0.40	0.01	0.23
134A	0.10	0.10	0.40	0.49	0.70	1.40	0.14	0.56	0.40	–0.01	0.20
135A	0.10	0.10	0.40	0.49	0.70	1.40	0.14	0.56	0.40	–0.01	0.20
136A	0.10	0.10	0.60	0.49	0.80	1.10	0.15	0.73	0.40	–0.01	0.20
137A	0.10	0.10	0.60	0.49	0.80	1.10	0.15	0.73	0.80	–0.01	0.40

Figure 4 Tolerance and solder joint analysis

Surface Mount Design and Land Pattern Standard

1.0 SCOPE

Microminiature leadless devices are available to the circuit designer in rectangular form for discrete components such as inductors.

This subsection provides the component and land pattern dimensions for inductors, along with an analysis of tolerance and solder joint assumptions used to arrive at the land pattern dimensions. Basic construction of the inductor is also covered.

2.0 APPLICABLE DOCUMENTS

See Section 8.0 for documents applicable to the subsections.

3.0 COMPONENT DESCRIPTIONS

A variety of values exist for inductors. The following sections describe the most common types.

3.1 Basic Construction At the time of publication, there was no industry standard document for leadless inductors. The dimensions were taken from manufacturer's catalogs, but only when at least two component vendors manufacture the same package. However, the same inductor value may not be available in the same package from the two manufacturers. See Figure 1.

3.1.1 Termination Materials End terminations should be solder coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the termination by hot dipping or by plating from solution. Plated solder terminations should be subjected to a post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

The termination shall be symmetrical, and shall not have nodules lumps, protrusions, etc., that compromise the symmetry or dimensional tolerances of the part. The end termination shall cover the ends of the components, and shall extend out to the top and bottom of the component.

Most common termination materials include palladium-silver alloy, silver, and gold. Solder finish applied over precious metal electrodes shall have a diffusion-barrier layer between the electrode metallization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick.

3.1.2 Marking Parts are available with or without marked inductance values.

3.1.3 Carrier Package Format Bulk rods, 8 mm tape/4 mm pitch is preferred for best handling. Tape and reel specifications provide additional requirements.

3.1.4 Resistance to Soldering Parts should be capable of withstanding five cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260°C.

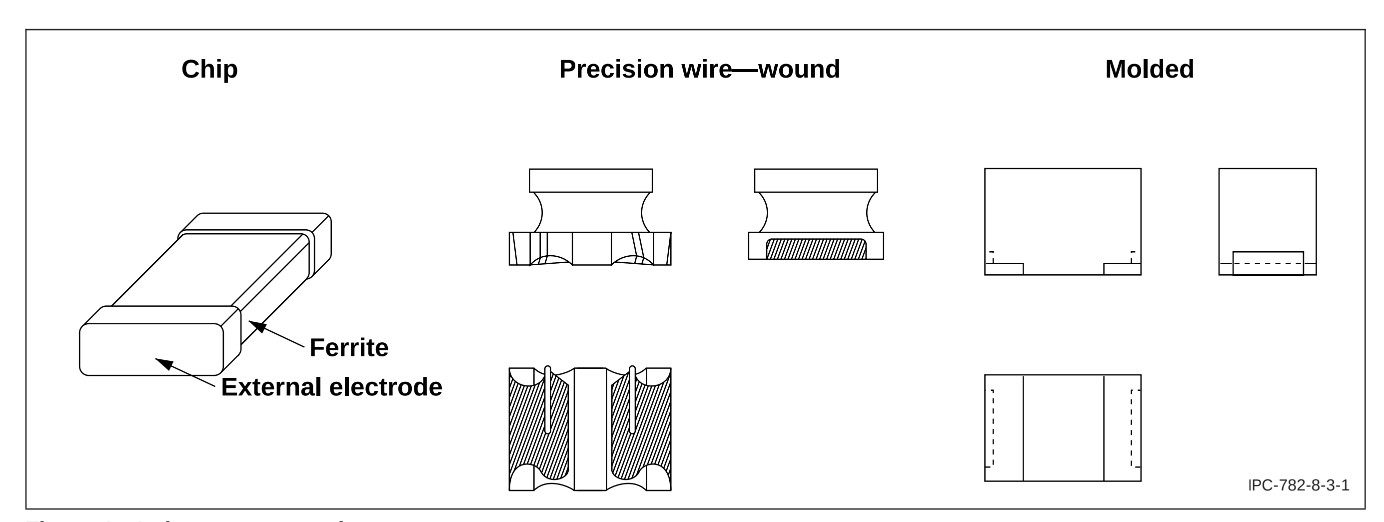
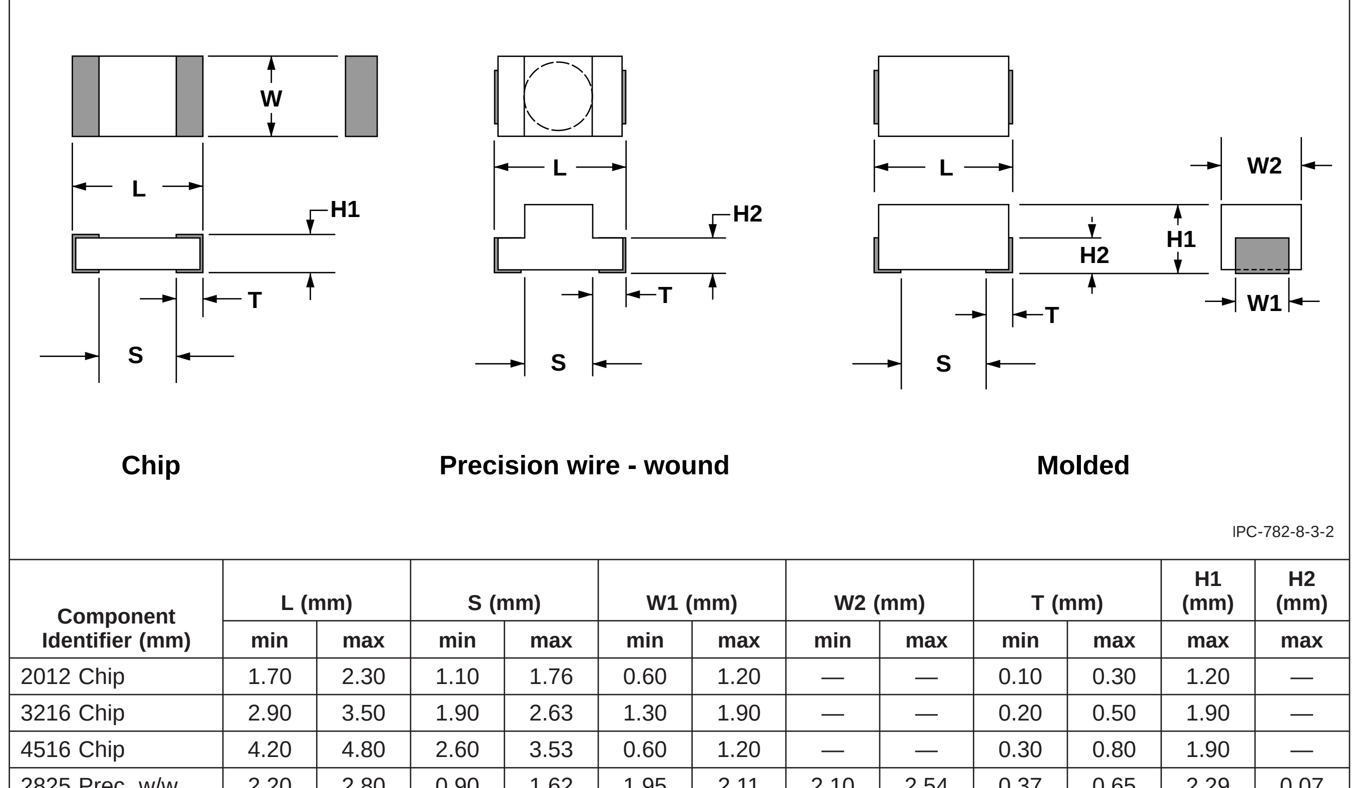


Figure 1 Inductor construction

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for inductors.



Component Identifier (mm)	L (mm)		S (mm)		W1 (mm)		W2 (mm)		T (mm)		H1 (mm)	H2 (mm)
	min	max	min	max	min	max	min	max	min	max	max	max
2012 Chip	1.70	2.30	1.10	1.76	0.60	1.20	—	—	0.10	0.30	1.20	—
3216 Chip	2.90	3.50	1.90	2.63	1.30	1.90	—	—	0.20	0.50	1.90	—
4516 Chip	4.20	4.80	2.60	3.53	0.60	1.20	—	—	0.30	0.80	1.90	—
2825 Prec. w/w	2.20	2.80	0.90	1.62	1.95	2.11	2.10	2.54	0.37	0.65	2.29	0.07
3225 Prec. w/w	2.90	3.50	0.90	1.83	1.40	1.80	—	—	0.50	1.00	2.00	0.50
4532 Prec. w/w	4.20	4.80	2.20	3.13	3.00	3.40	—	—	0.50	1.00	2.80	0.50
5038 Prec. w/w	4.35	4.95	2.81	3.51	2.46	2.62	3.41	3.81	0.51	0.77	3.80	0.76
3225/3230 Molded	3.00	3.40	1.60	2.18	1.80	2.00	2.30	2.70	0.40	0.70	2.40	0.51
4035 Molded	3.81	4.32	0.81	1.60	1.20	1.50	2.92	3.18	1.20	1.50	2.67	1.27
4532 Molded	4.20	4.80	2.30	3.15	2.00	2.20	3.00	3.40	0.65	0.95	3.40	0.50
5650 Molded	5.30	5.50	3.30	4.32	3.80	4.20	4.70	5.30	0.50	1.00	5.80	1.00
8530 Molded	8.25	8.76	5.25	6.04	1.20	1.50	2.92	3.18	1.20	1.50	2.67	1.27

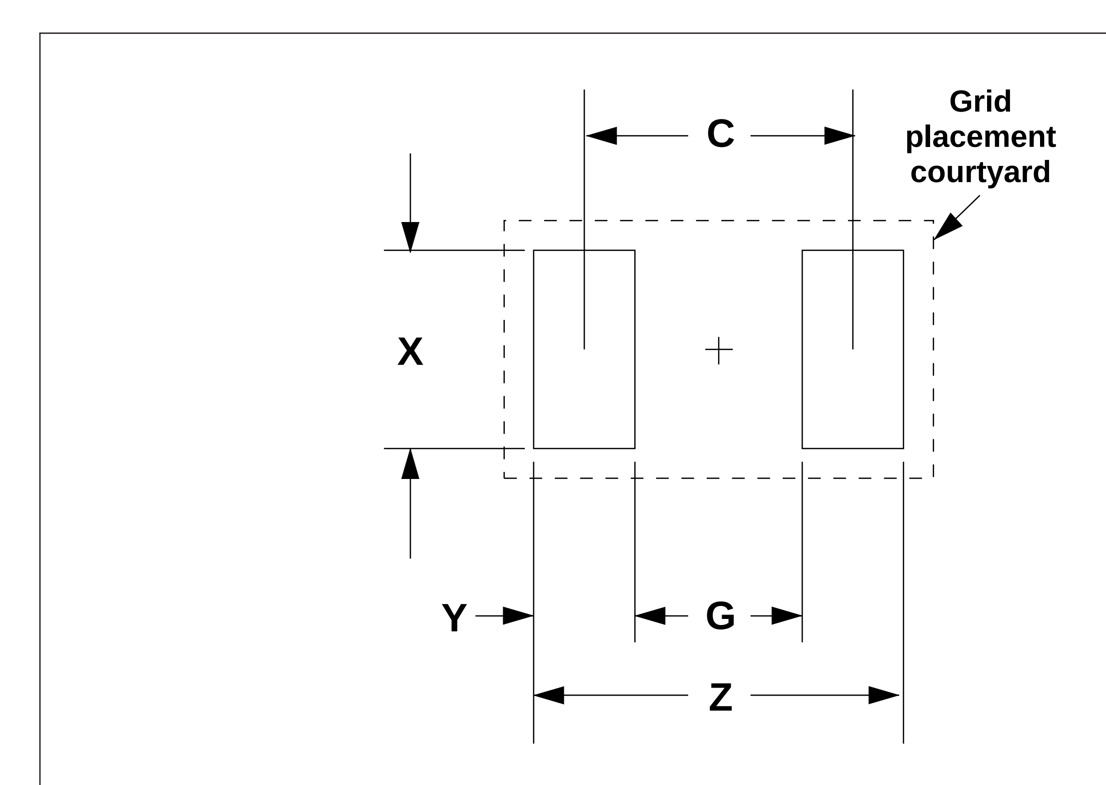
Figure 2 Inductor component dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for inductors. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least mate-rial condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



RLP No.	Component Identifier (mm)	Z (mm)	G (mm)	X (mm)	C (mm) ref	Y (mm) ref	Placement Grid (No. Grid Elements)
160	2012 Chip	3.00	1.00	1.00	2.00	1.00	4x8
161	3216 Chip	4.20	1.80	1.60	3.00	1.20	6x10
162	4516 Chip	5.80	2.60	1.00	4.20	1.60	4x12
163	2825 Prec	3.80	1.00	2.40	2.40	1.40	6x10
164	3225 Prec	4.60	1.00	2.00	2.80	1.80	6x10
165	4532 Prec	5.80	2.20	3.60	4.00	1.80	8x14
166	5038 Prec	5.80	3.00	2.80	4.40	1.40	8x14
167	3225/3230 Molded	4.40	1.20	2.20	2.80	1.60	6x10
168	4035 Molded	5.40	1.00	1.40	3.20	2.20	8x12
169	4532 Molded	5.80	1.80	2.40	3.80	2.00	8x14
170	5650 Molded	6.80	3.20	4.00	5.00	1.80	12x16
171	8530 Molded	9.80	5.00	1.40	7.40	2.40	8x22

Figure 3 Inductor land pattern dimensions

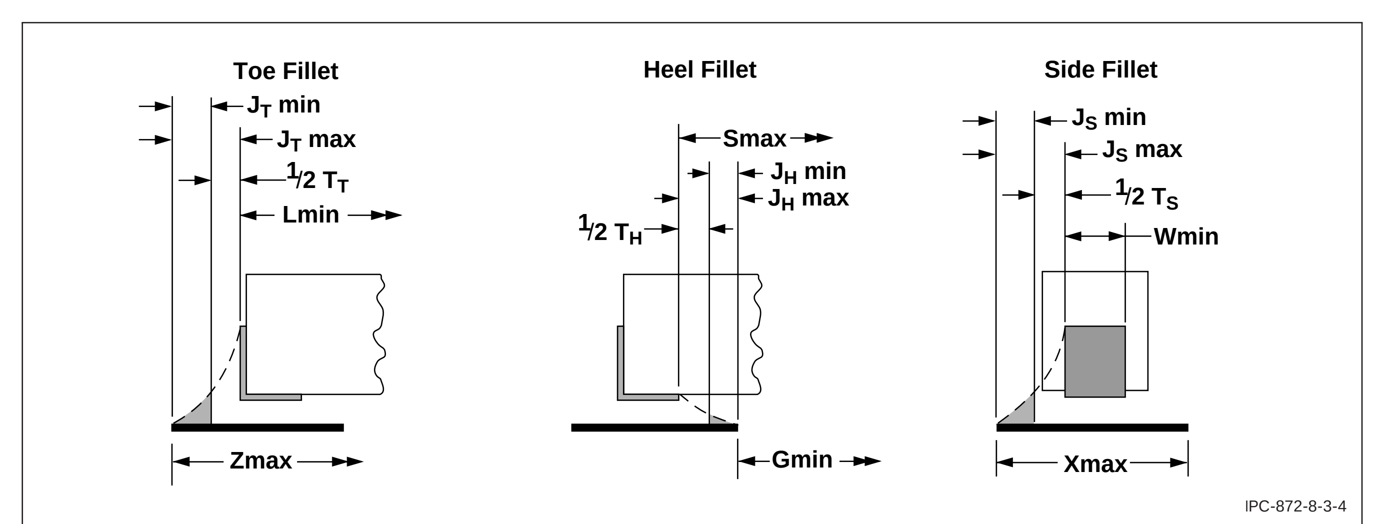
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



RLP No.	Tolerance Assumptions (mm)		Solder Joint: Toe (mm)			Heel (mm)			Side (mm)		
	F	P	C_L	$J_T$min	$J_T$max	C_S	$J_H$min	$J_H$max	C_{WI}	$J_S$min	$J_S$max
160	0.2	0.2	0.663	0.32	0.98	0.721	0.02	0.74	0.663	–0.13	0.53
161	0.2	0.2	0.663	0.32	0.98	0.787	0.02	0.81	0.663	–0.18	0.48
162	0.2	0.2	0.663	0.47	1.13	0.970	–0.02	0.95	0.663	–0.13	0.53
163	0.2	0.2	0.663	0.47	1.13	0.773	–0.08	0.70	0.325	0.06	0.39
164	0.2	0.2	0.663	0.52	1.18	0.970	–0.07	0.90	0.490	0.06	0.54
165	0.2	0.2	0.663	0.47	1.13	0.970	–0.02	0.95	0.490	0.05	0.54
166	0.2	0.2	0.663	0.39	1.06	0.758	–0.12	0.64	0.325	0.01	0.33
167	0.2	0.2	0.490	0.46	0.94	0.648	0.17	0.82	0.346	0.03	0.37
168	0.2	0.2	0.583	0.50	1.09	0.837	–0.12	0.72	0.412	–0.11	0.31
169	0.2	0.2	0.663	0.47	1.13	0.894	0.23	1.12	0.346	0.03	0.37
170	0.2	0.2	0.346	0.58	0.92	1.058	0.03	1.09	0.490	–0.14	0.34
171	0.2	0.2	0.583	0.48	1.07	0.837	0.10	0.94	0.412	–0.11	0.31

Figure 4 Tolerance and solder joint analysis



IPC-SM-782

Surface Mount Design and Land Pattern Standard

Date	Section
5/96	8.4
Revision	Subject
A	Tantalum Capacitors

1.0 SCOPE

Microminiature leadless devices are available to the circuit designer in rectangular form for discrete components such as tantalum capacitors.

This subsection provides the component and land pattern dimensions for tantalum capacitors along with an analysis of tolerance and solder joint assumptions used to arrive at the land pattern dimensions. Basic construction of the inductor is also covered.

2.0 APPLICABLE DOCUMENTS

See Section 8.0 for documents applicable to the subsections.

3.0 COMPONENT DESCRIPTIONS

A variety of values exist for tantalum capacitors. The following sections describe the most common types.

3.1 Basic Construction See Figure 1.

3.1.1 Termination Materials End terminations should be solder coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the termination by hot dipping or by plating from solution. Plated solder terminations should be subjected to a post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

The termination shall be symmetrical, and shall not have nodules lumps, protrusions, etc., that compromise the symmetry or dimensional tolerances of the part. The end termination shall cover the ends of the components, and shall extend out to the top and bottom of the component.

Most common termination materials include palladium-silver alloy, silver, and gold. Solder finish applied over precious metal electrodes shall have a diffusion-barrier layer between the electrode metallization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick.

3.1.2 Marking Parts are available with or without marked capacitance values.

3.1.3 Carrier Package Format Bulk rods, 8 mm tape/4 mm pitch is preferred for best handling. Tape and reel specifications provide additional requirements.

3.1.4 Resistance to Soldering Parts should be capable of withstanding five cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260°C.

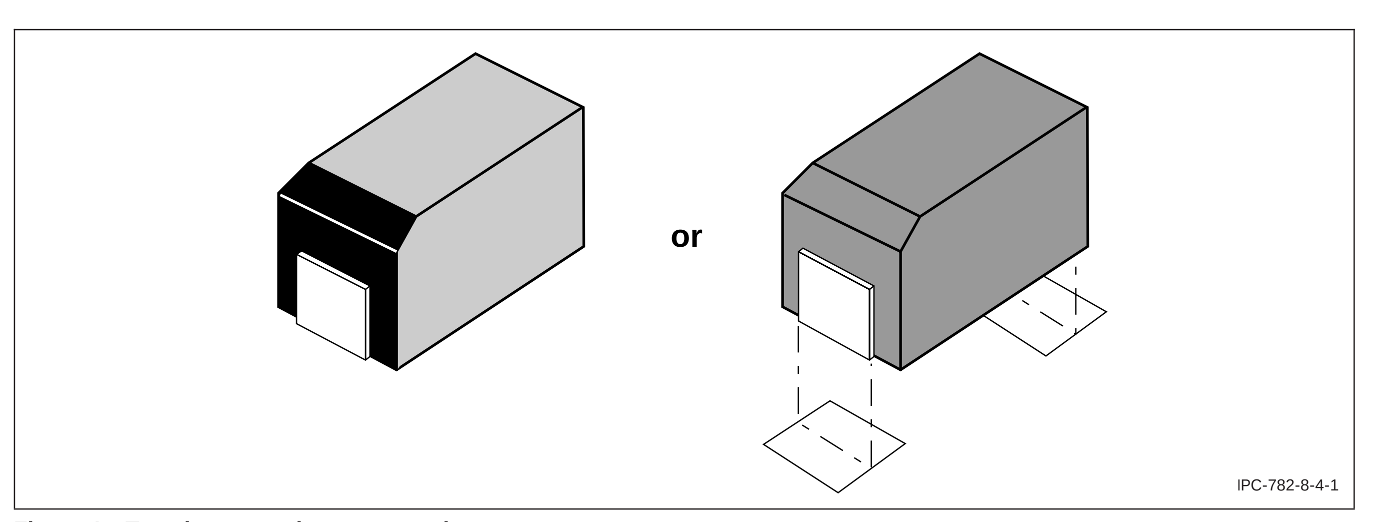
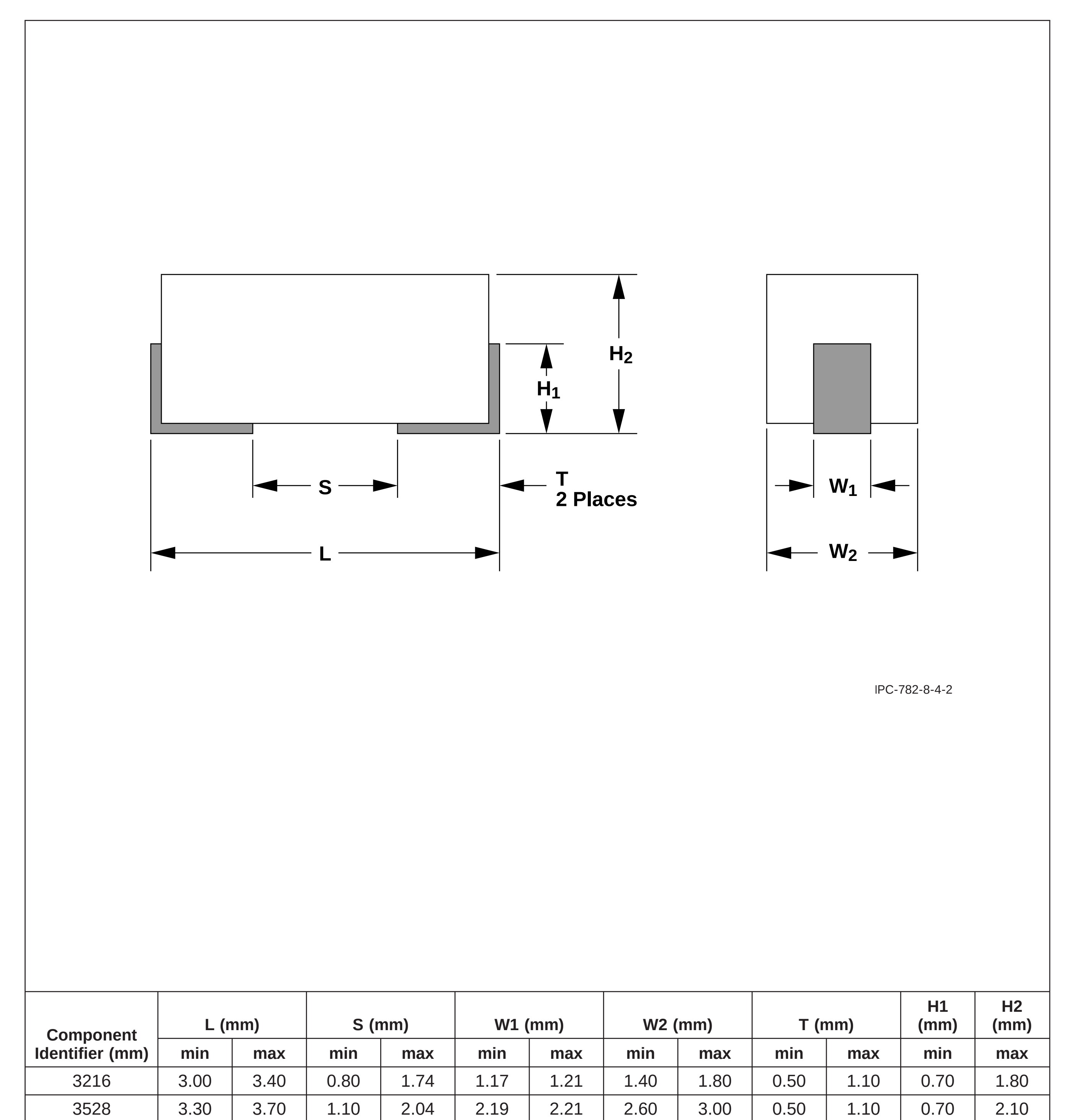


Figure 1 Tantalum capacitor construction

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for tantalum capacitors.



Component Identifier (mm)	L (mm)		S (mm)		W1 (mm)		W2 (mm)		T (mm)		H1 (mm)	H2 (mm)
	min	max	min	max	min	max	min	max	min	max	min	max
3216	3.00	3.40	0.80	1.74	1.17	1.21	1.40	1.80	0.50	1.10	0.70	1.80
3528	3.30	3.70	1.10	2.04	2.19	2.21	2.60	3.00	0.50	1.10	0.70	2.10
6032	5.70	6.30	2.50	3.54	2.19	2.21	2.90	3.50	1.00	1.60	1.00	2.80
7343	7.00	7.60	3.80	4.84	2.39	2.41	4.00	4.60	1.00	1.60	1.00	3.10

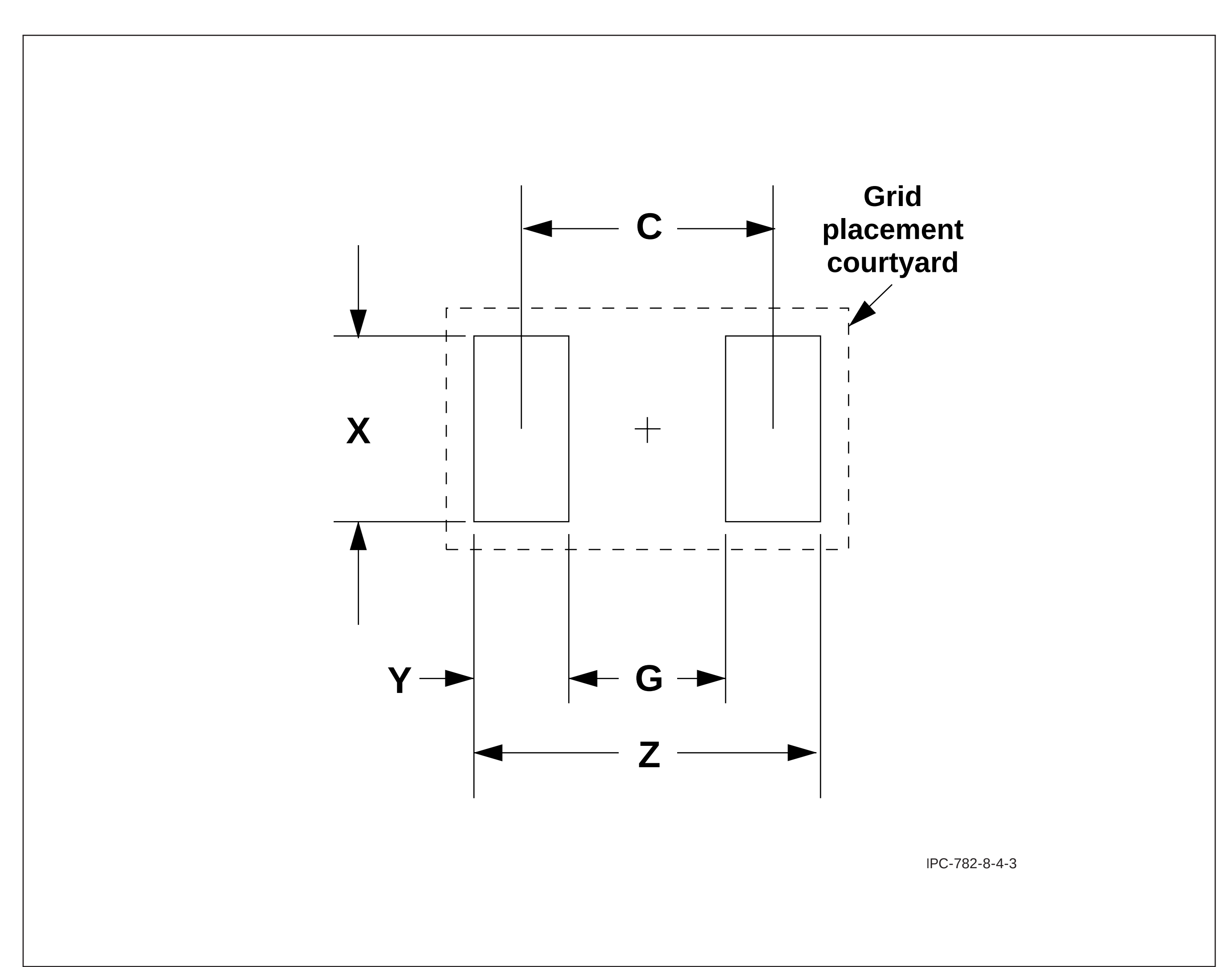
Figure 2 Tantalum capacitor component dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for tantalum capacitors. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



RLP No.	Component Identifier (mm)	Z (mm)	G (mm)	X (mm)	Y (mm) ref	C (mm) ref	Placement Grid (No. of Grid Elements)
180A	3216	4.80	0.80	1.20	2.00	2.80	6x12
181A	3528	5.00	1.00	2.20	2.00	3.00	8x12
182A	6032	7.60	2.40	2.20	2.60	5.00	8x18
183A	7343	9.00	3.80	2.40	2.60	6.40	10x20

Figure 3 Tantalum capacitor land pattern dimensions

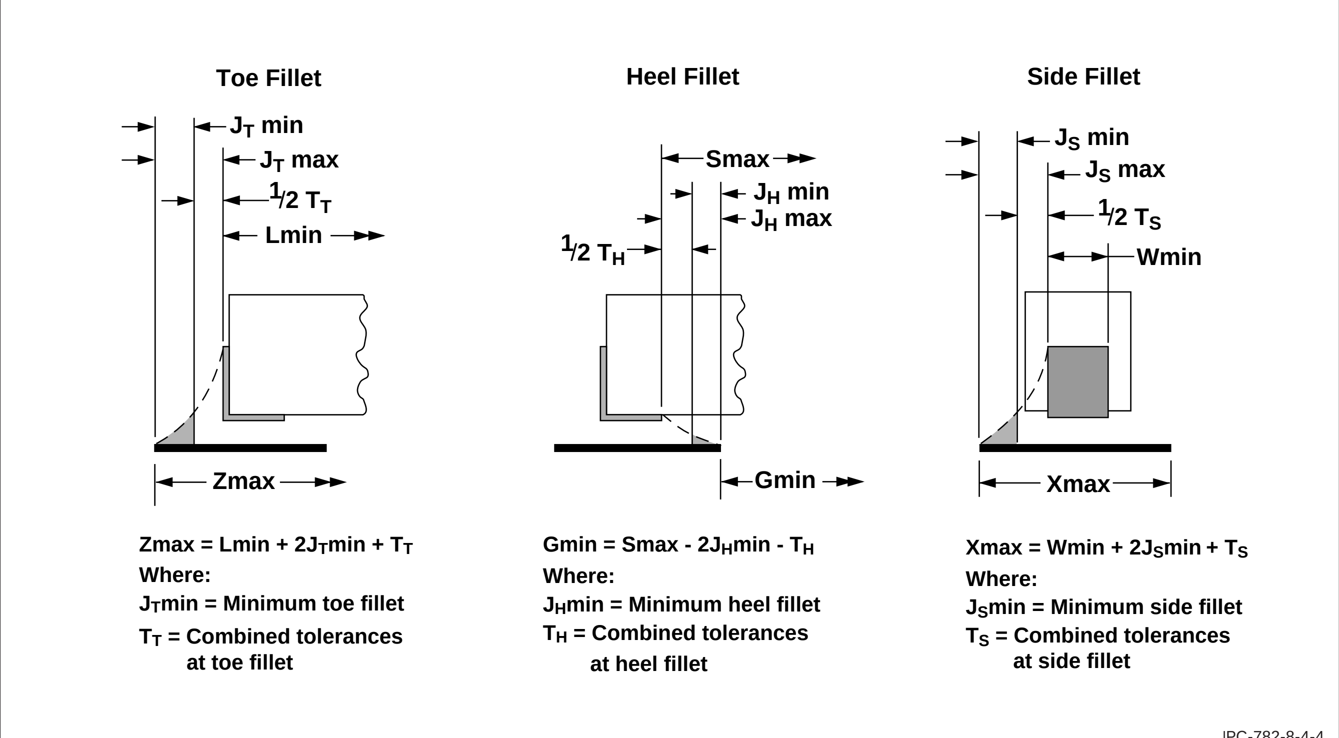
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



RLP No.	Tolerance Assumptions (mm)		Solder Joint Toe (mm)			Heel (mm)			Side (mm)		
	F	P	C_L	$J_T$min	$J_T$max	C_S	$J_H$min	$J_H$max	C_W	$J_S$min	$J_S$max
180A	0.10	0.10	0.40	0.69	1.11	0.94	–0.01	0.94	0.40	–0.20	0.23
181A	0.10	0.10	0.40	0.64	1.06	0.94	0.04	0.99	0.40	–0.21	0.22
182A	0.10	0.10	0.60	0.64	1.26	1.04	0.05	1.09	0.60	–0.30	0.31
183A	0.10	0.10	0.60	0.69	1.31	1.04	–0.00	1.04	0.60	–0.30	0.31

Figure 4 Tolerance and solder joint analysis

1.0 SCOPE

This subsection provides the component and land pattern dimensions for metal electrode face components (MELFs). Basic construction of the MELF device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

2.0 APPLICABLE DOCUMENTS

See Section 8.0 for documents applicable to the subsections.

3.0 COMPONENT DESCRIPTIONS

Resistors, ceramic capacitors, and tantalum capacitors may all be packaged in these tubular shapes.

3.1 Basic Construction See Figures 1a and 1b.

3.1.1 Termination Materials End terminations should be solder-coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the termination by hot dipping or by plating from solution. Plated solder terminations should be subjected to post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in] thick. The terminations should be symmetrical, and should not have nodules, lumps, protrusions, etc., that compromise the symmetry or dimensional tolerances of the part.

The most common termination materials include palladium-silver alloy, silver, and gold. Solder finish applied over precious metal electrodes should have a diffusion barrier layer between the electrode metallization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick. The end termination shall cover the ends of the components, and shall extend around the entire periphery.

3.1.2 Marking Parts are available with or without marked values.

3.1.3 Carrier Package Format Bulk rods, 8 mm tape/4 mm pitch is preferred for best handling. Tape and reel specifications provide additional requirements.

3.1.4 Resistance to Soldering Parts should be capable of withstanding five cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260°C.

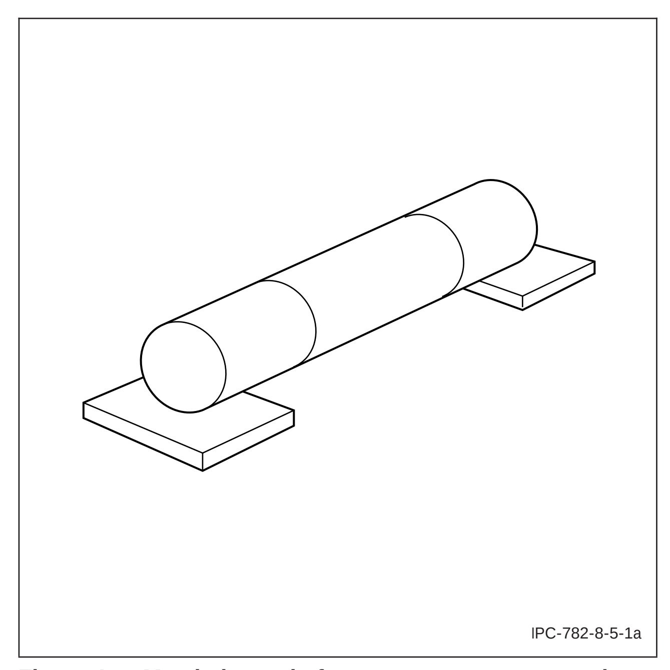


Figure 1a Metal electrode face component construction

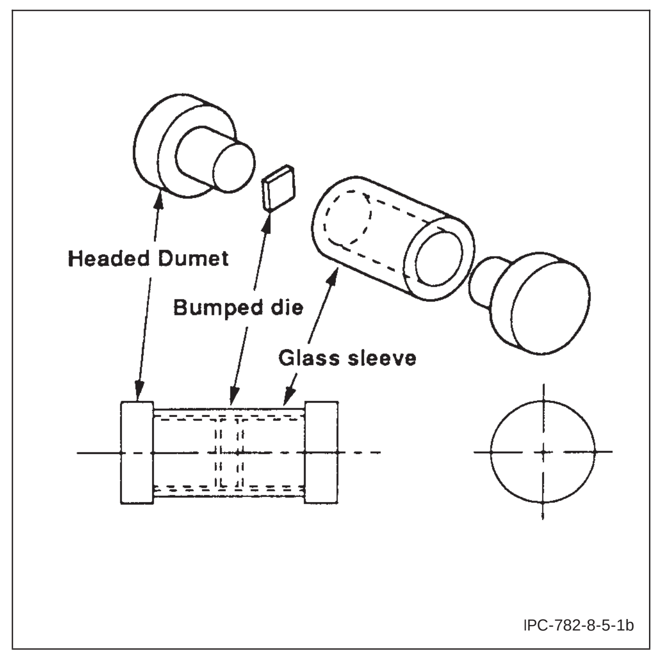
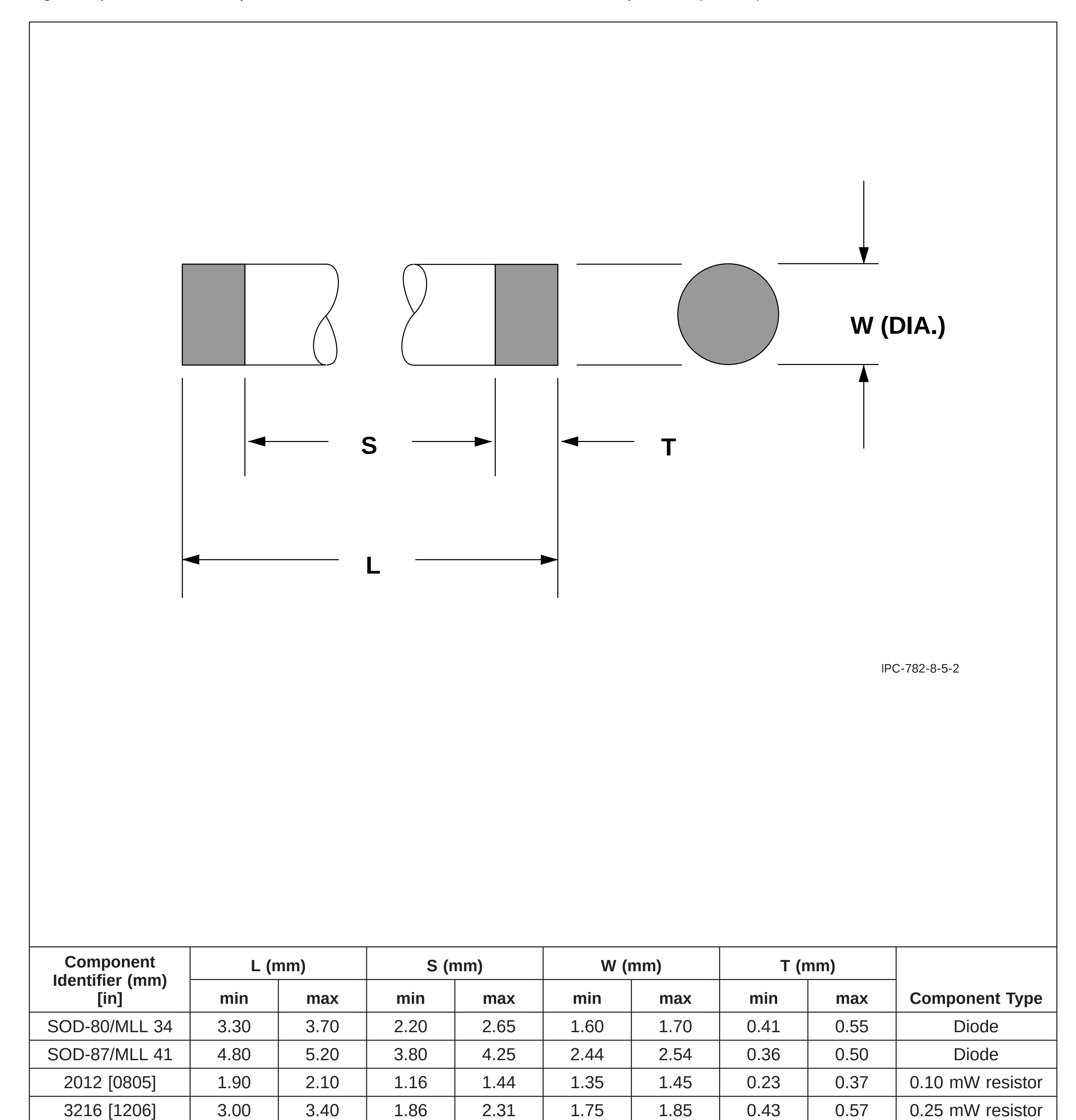


Figure 1b Break-away diagram of MELF components

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for metal electrode face components (MELFs).



Component Identifier (mm) [in]	L (mm)		S (mm)		W (mm)		T (mm)		Component Type
	min	max	min	max	min	max	min	max	
SOD-80/MLL 34	3.30	3.70	2.20	2.65	1.60	1.70	0.41	0.55	Diode
SOD-87/MLL 41	4.80	5.20	3.80	4.25	2.44	2.54	0.36	0.50	Diode
2012 [0805]	1.90	2.10	1.16	1.44	1.35	1.45	0.23	0.37	0.10 mW resistor
3216 [1206]	3.00	3.40	1.86	2.31	1.75	1.85	0.43	0.57	0.25 mW resistor
3516 [1406]	3.30	3.70	2.16	2.61	1.55	1.65	0.43	0.57	0.12 W resistor
5923 [2309]	5.70	6.10	4.36	4.81	2.40	2.50	0.53	0.67	0.25 W resistor

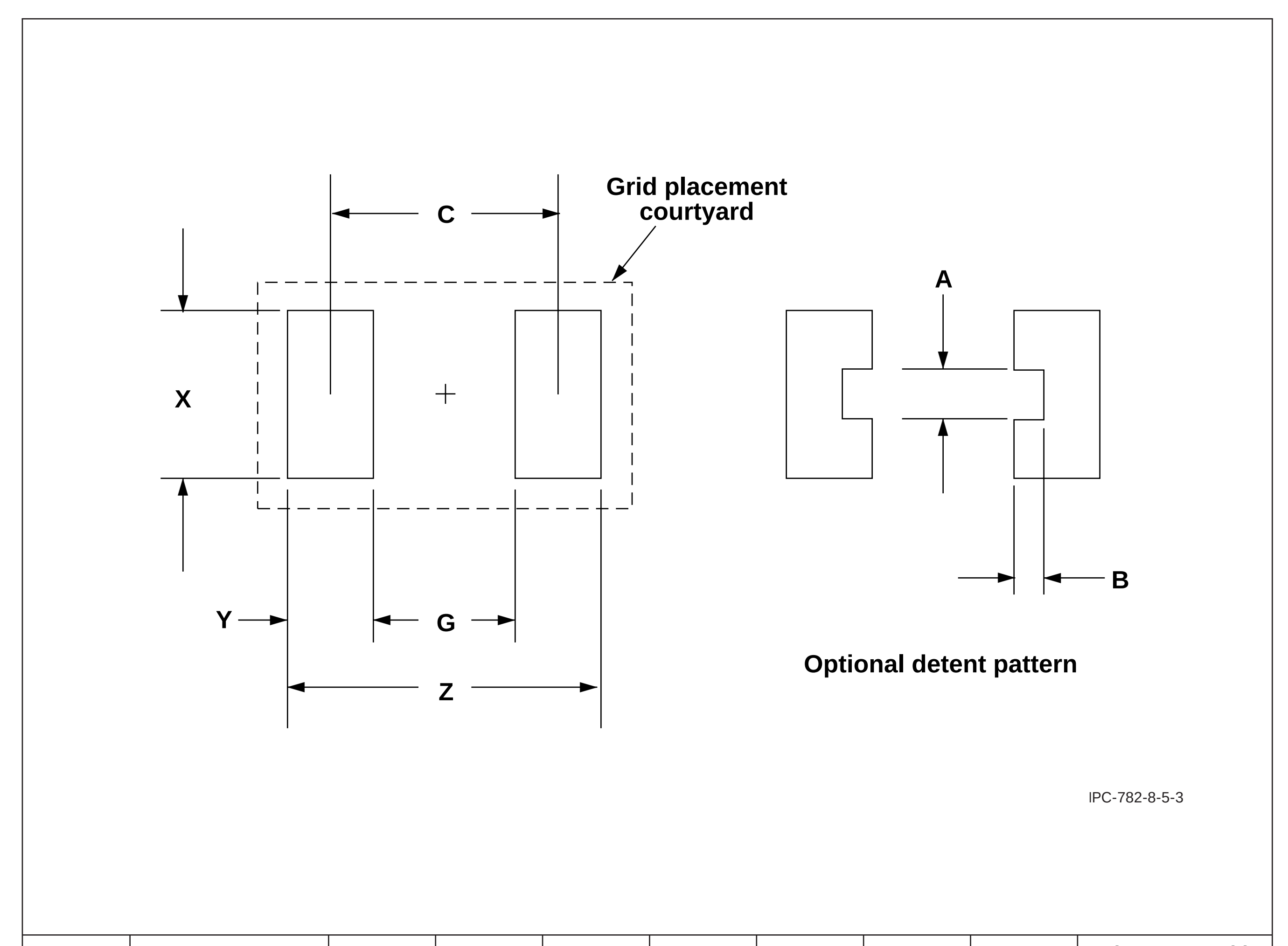
Figure 2 Metal electrode face component dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for metal electrode face components (MELFs). These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



RLP No.	Component Identifier (mm) [in]	Z (mm)	G (mm)	X (mm)	Y (mm) ref	C (mm) ref	A	B	Placement Grid (No. of Grid Elements)
200A	SOD-80/MLL-34	4.80	2.00	1.80	1.40	3.40	0.50	0.50	6x12
201A	SOD-87/MLL-41	6.30	3.40	2.60	1.45	4.85	0.50	0.50	6x14
202A	2012 [0805]	3.20	0.60	1.60	1.30	1.90	0.50	0.35	4x8
203A	3216 [1206]	4.40	1.20	2.00	1.60	2.80	0.50	0.55	6x10
204A	3516 [1406]	4.80	2.00	1.80	1.40	3.40	0.50	0.55	6x12
205A	5923 [2309]	7.20	4.20	2.60	1.50	5.70	0.50	0.65	6x18

Figure 3 Metal electrode face component land pattern dimensions

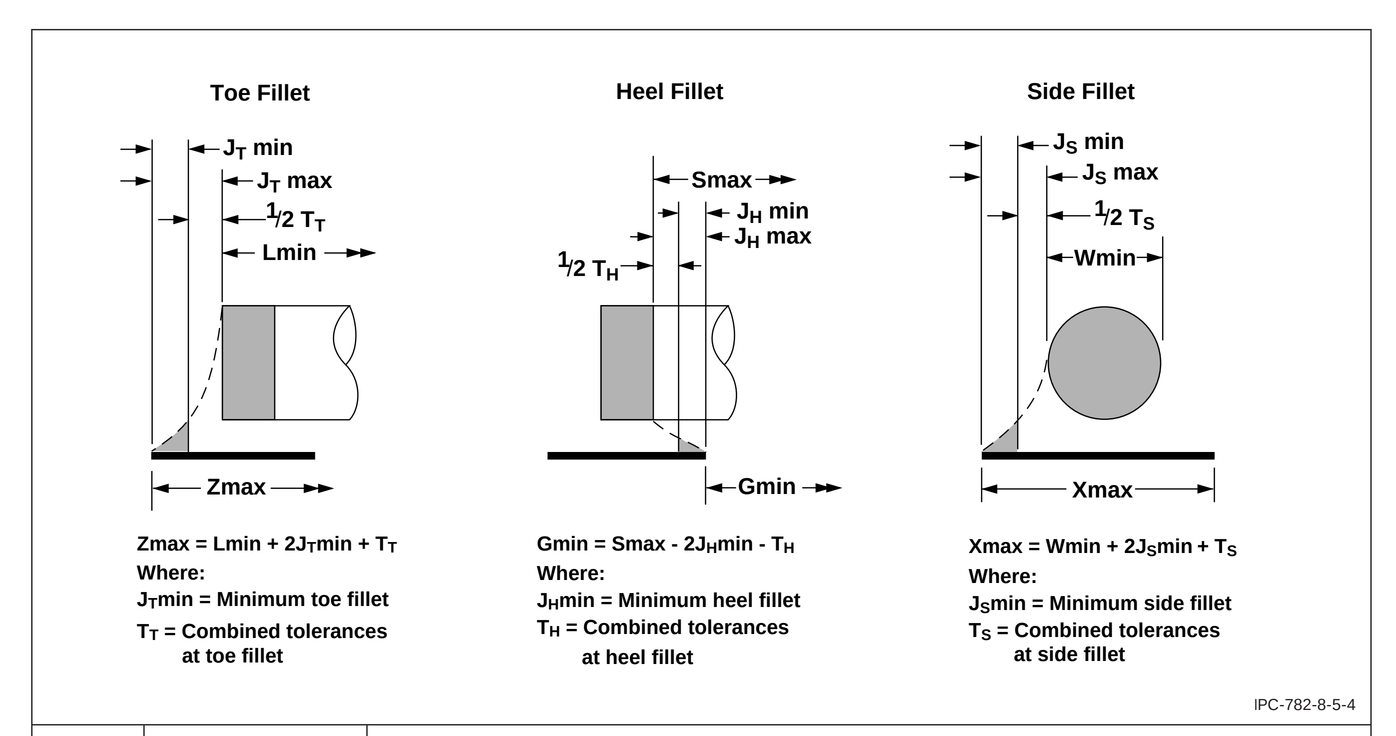
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



RLP No.	Tolerance Assumptions (mm)		Solder Joint								
			Toe (mm)			Heel (mm)			Side (mm)		
	F	P	C_L	$J_T$min	$J_T$max	C_S	$J_H$min	$J_H$max	C_W	$J_S$min	$J_S$max
200A	0.10	0.10	0.40	0.54	0.96	0.45	0.09	0.56	0.10	0.01	0.19
201A	0.10	0.10	0.40	0.54	0.96	0.45	0.19	0.66	0.10	-0.01	0.17
202A	0.10	0.10	0.20	0.53	0.77	0.28	0.26	0.58	0.10	0.04	0.21
203A	0.10	0.10	0.40	0.49	0.91	0.45	0.32	0.79	0.10	0.04	0.21
204A	0.10	0.10	0.40	0.54	0.96	0.45	0.07	0.54	0.10	0.04	0.21
205A	0.10	0.10	0.40	0.54	0.96	0.45	0.07	0.54	0.10	0.01	0.19

Figure 4 Tolerance and solder joint analysis

1.0 SCOPE

This subsection provides the component and land pattern dimensions for SOT 23 (small outline transistor) components. Basic construction of the SOT 23 device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

2.0 APPLICABLE DOCUMENTS

See Section 8.0 for documents applicable to the subsections.

3.0 COMPONENT DESCRIPTIONS

One of the first active devices in packaged form for surface mounting was the SOT device. Plastic encapsulated three terminal devices with leads formed out from the body were surface mounted to overcome some of the problems and difficulties in handling dip transistors. In general, SOT packages are used with diodes, transistors, and small I/O devices.

The SOT 23 package is the most common three-lead surface mount configuration.

3.1 Basic Construction The SOT 23 package has had several redesigns to meet the needs of both hybrid and printed board surface mount industries. These changes resulted in low, medium and high profile characteristics which basically reflect the clearance that the body is from the mounting surface. See Figure 1 for construction characteristics and Figure 2 for dimensions.

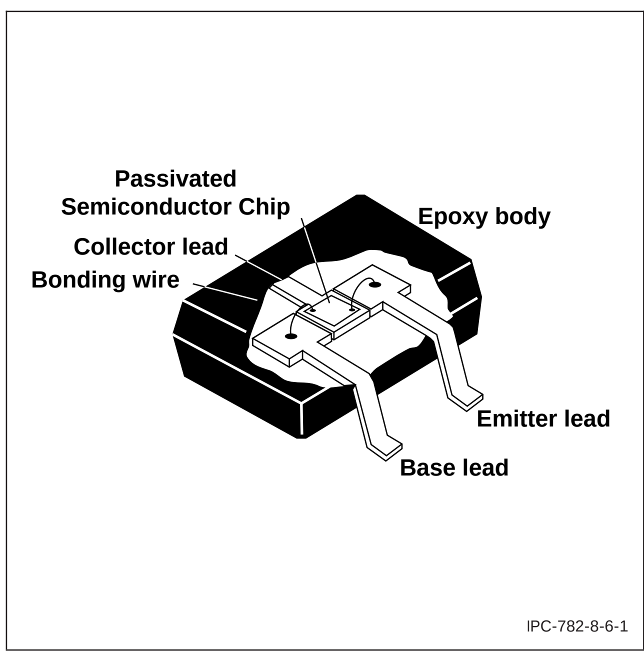


Figure 1 SOT 23 construction

3.1.1 Termination Materials Leads should be solder-coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the leads by hot dipping or by plating from solution. Plated solder terminations should be subjected to post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

Solder finish applied over precious metal electrodes should have a diffusion barrier layer between the electrode metallization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick.

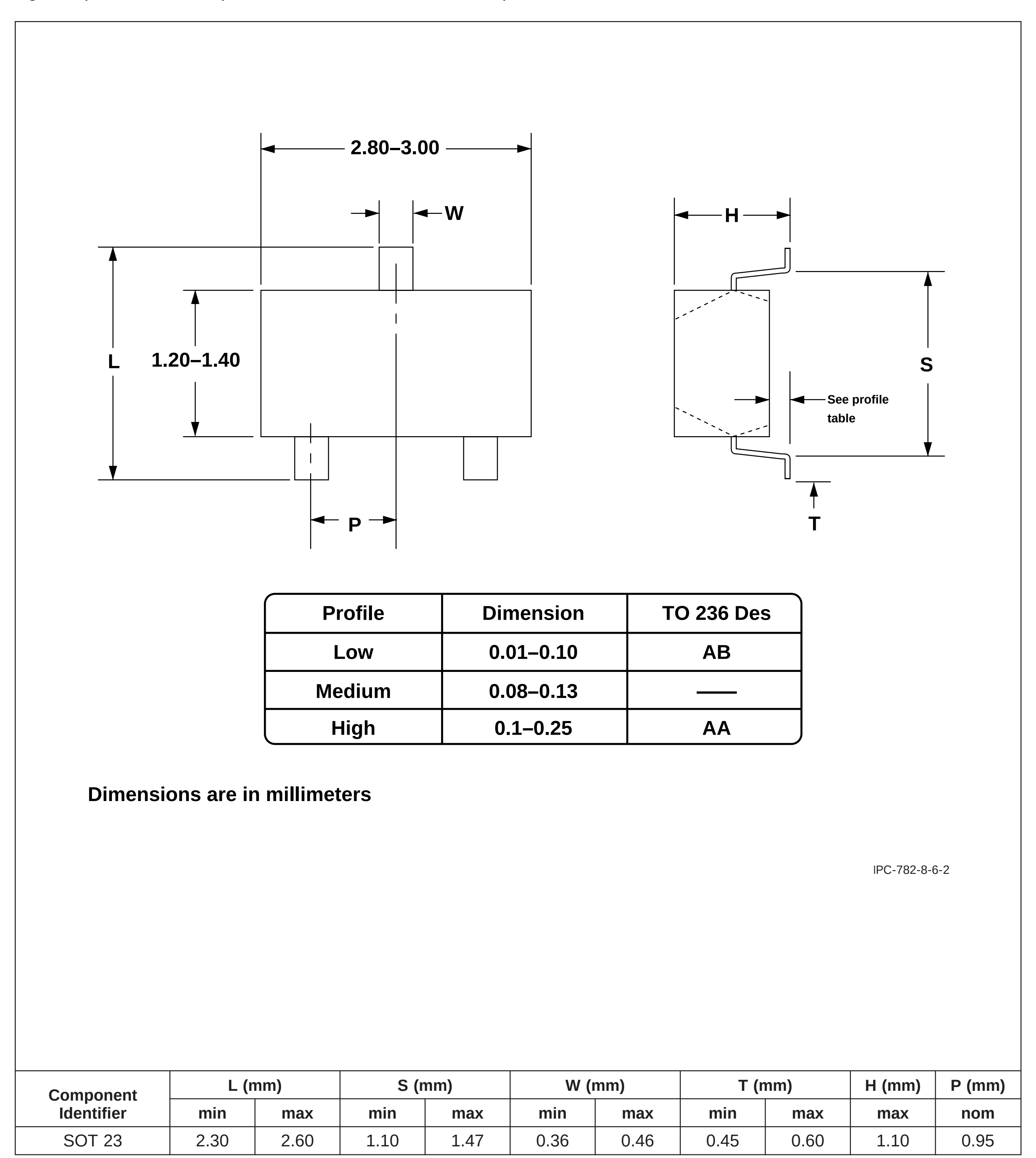
3.1.2 Marking Parts are available with or without marked values.

3.1.3 Carrier Package Format Carrier package format shall be according to the following: body type TO-236, 8 mm tape/4 mm pitch.

3.1.4 Resistance to Soldering Parts should be capable of withstanding five cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260°C.

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for SOT 23 components.



Profile	Dimension	TO 236 Des
Low	0.01–0.10	AB
Medium	0.08–0.13	——
High	0.1–0.25	AA

Component Identifier	L (mm)		S (mm)		W (mm)		T (mm)		H (mm)	P (mm)
	min	max	min	max	min	max	min	max	max	nom
SOT 23	2.30	2.60	1.10	1.47	0.36	0.46	0.45	0.60	1.10	0.95

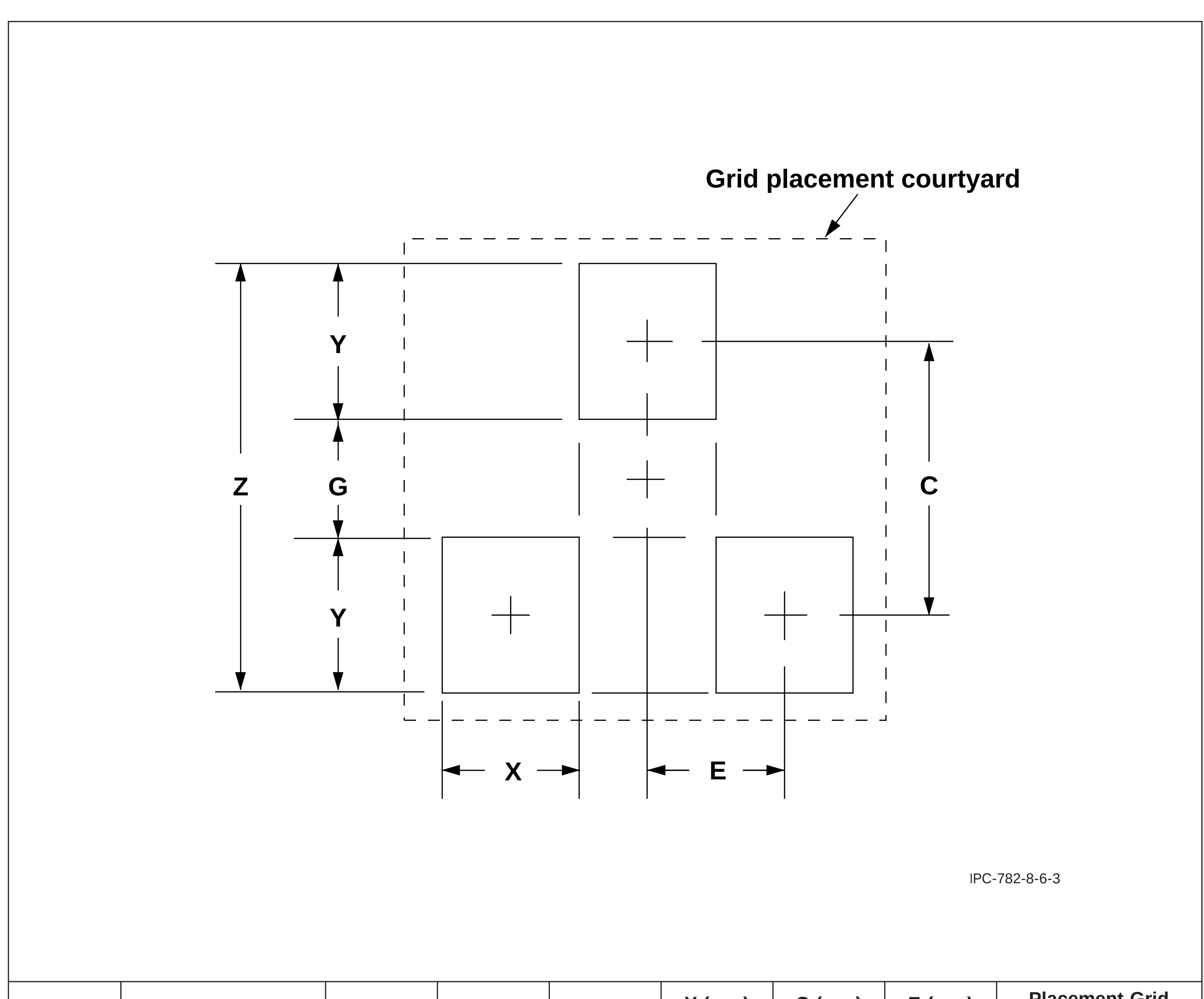
Figure 2 SOT 23 component dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for SOT 23 components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



RLP No.	Component Identifier	Z (mm)	G (mm)	X (mm)	Y (mm) ref	C (mm) ref	E (mm) ref	Placement Grid (No. of Grid Elements)
210	SOT 23 (reflow solder)	3.60	0.80	1.00	1.40	2.20	0.95	8x8

*Note: If a more robust pattern is desired for wave soldering, add 0.2 mm to “Z” and identify as RLP 210W.

Figure 3 SOT 23 land pattern dimensions

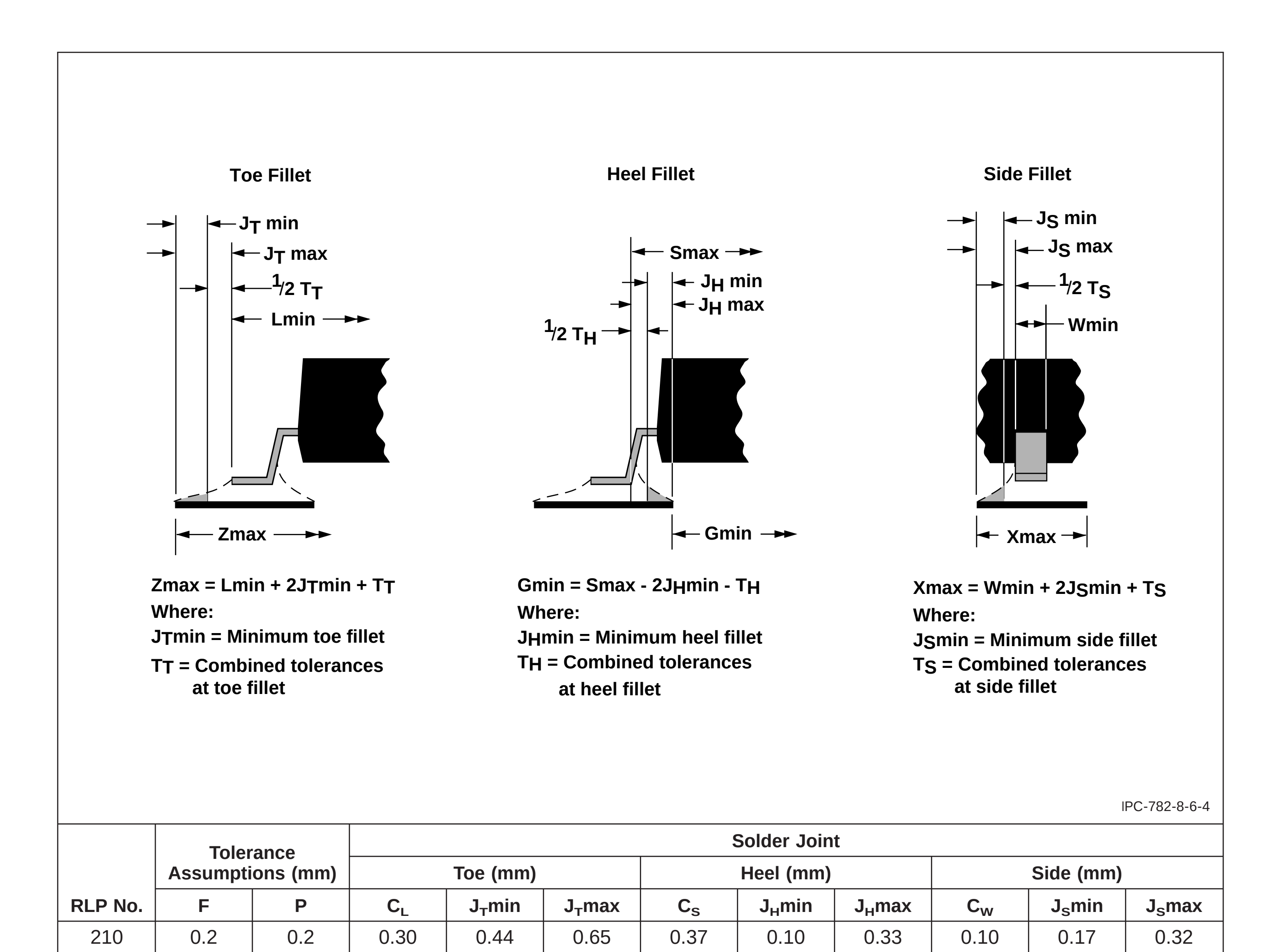
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



RLP No.	Tolerance Assumptions (mm)		Solder Joint								
			Toe (mm)			Heel (mm)			Side (mm)		
	F	P	C_L	$J_T$min	$J_T$max	C_S	$J_H$min	$J_H$max	C_W	$J_S$min	$J_S$max
210	0.2	0.2	0.30	0.44	0.65	0.37	0.10	0.33	0.10	0.17	0.32

Figure 4 Tolerance and solder joint analysis



IPC-SM-782

Surface Mount Design and Land Pattern Standard

Date	Section
8/93	8.7
Revision	Subject
	SOT 89

1.0 SCOPE

This subsection provides the component and land pattern dimensions for SOT 89 (small outline transistor) components. Basic construction of the SOT 89 device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

2.0 APPLICABLE DOCUMENTS

See Section 8.0 for documents applicable to the subsections.

2.1 Electronic Industries Association (EIA) JEDEC Pubication 95 Registered and Standard Outlines for Solid State and Related Products, TO-243, Issue ''C'' dated 7/15/86

Application for copies should be addressed to:
Global Engineering Documents
1990 M Street N.W.
Washington, DC

3.0 COMPONENT DESCRIPTIONS

These parts are for high power transistors and diodes. These parts are used where heat transfer to a supporting structure is important.

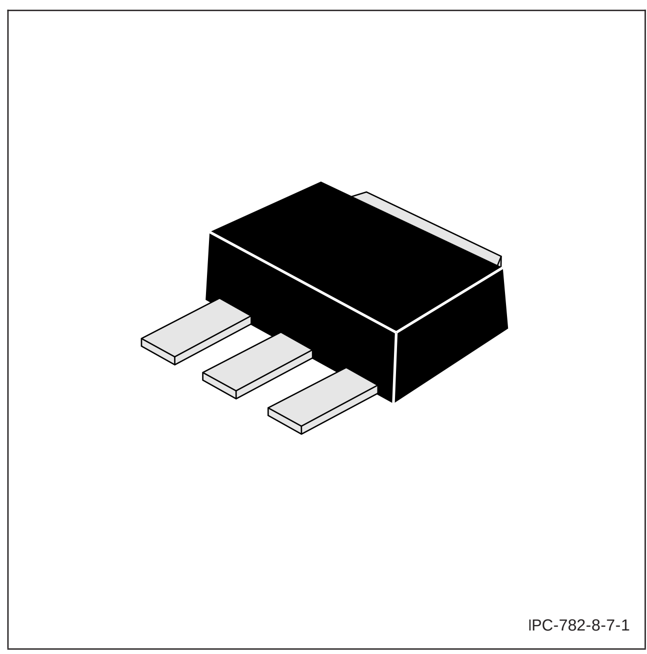


Figure 1 SOT 89 construction

3.1 Basic Construction See Figure 1. The SOT 89 package dimensions are designed to meet the needs of both the hybrid and printed board surface mount industries. In order to provide an adequate heat transfer path, there is no clearance between the body of the component and the packaging and interconnect structure. This design may accommodate the reflow or wave soldering processes.

3.1.1 Termination Materials Leads must be solder-coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the leads by hot dipping or by plating from solution. Plated solder terminations should be subjected to post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

Solder finish applied over precious metal electrodes should have a diffusion barrier layer between the electrode metallization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick.

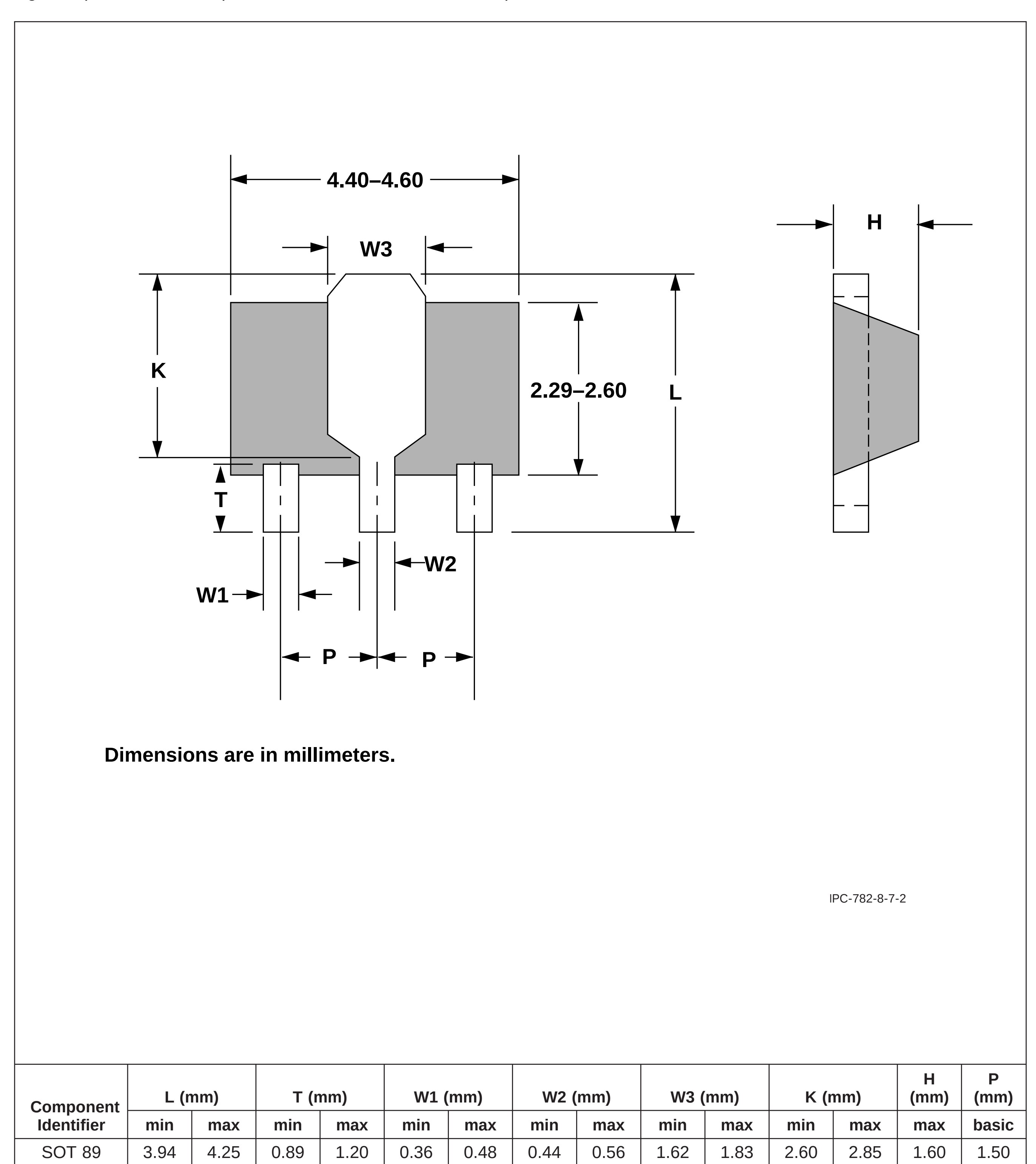
3.1.2 Marking Parts are available with or without marked values.

3.1.3 Carrier Package Format Carrier package format shall be according to the following: body type TO-243, 12 mm tape/8 mm pitch.

3.1.4 Resistance to Soldering Parts should be capable of withstanding ten cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260°C.

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for SOT 89 components.



Component Identifier	L (mm)		T (mm)		W1 (mm)		W2 (mm)		W3 (mm)		K (mm)		H (mm)	P (mm)
	min	max	min	max	min	max	min	max	min	max	min	max	max	basic
SOT 89	3.94	4.25	0.89	1.20	0.36	0.48	0.44	0.56	1.62	1.83	2.60	2.85	1.60	1.50

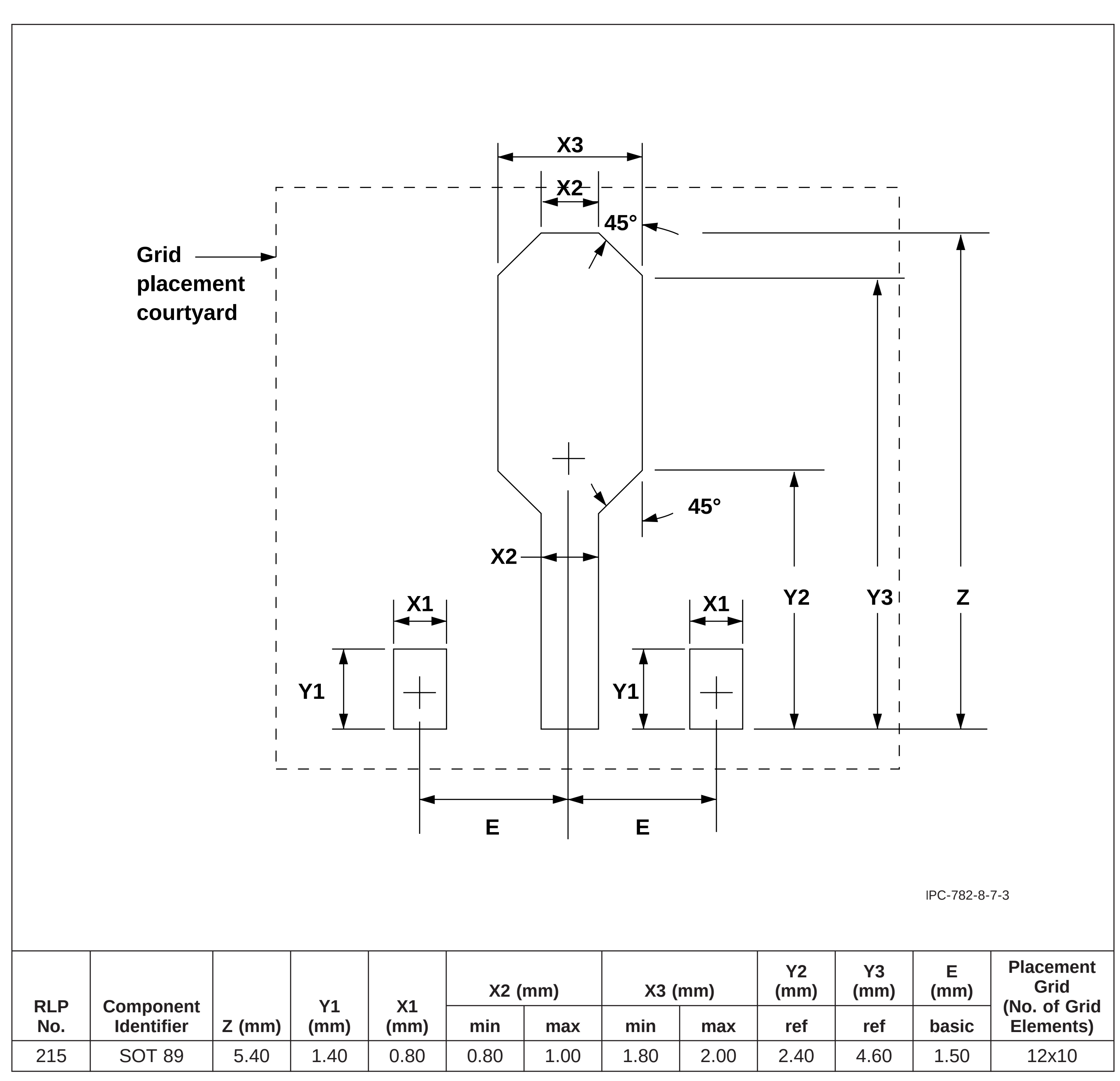
Figure 2 SOT 89 component dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for SOT 89 components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



RLP No.	Component Identifier	Z (mm)	Y1 (mm)	X1 (mm)	X2 (mm)		X3 (mm)		Y2 (mm)	Y3 (mm)	E (mm)	Placement Grid (No. of Grid Elements)
					min	max	min	max	ref	ref	basic	
215	SOT 89	5.40	1.40	0.80	0.80	1.00	1.80	2.00	2.40	4.60	1.50	12x10

Figure 3 SOT 89 land pattern dimensions

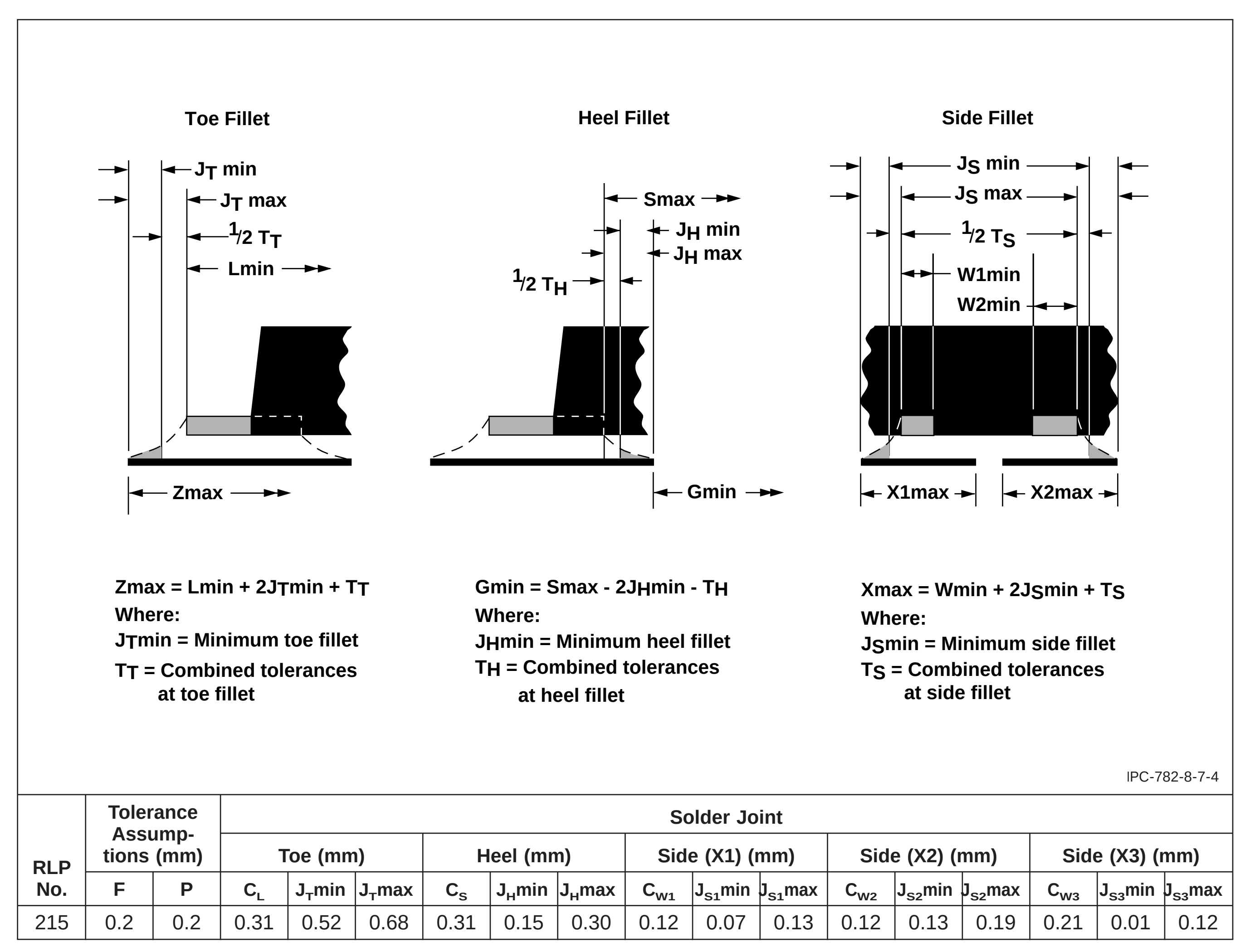
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



RLP No.	Tolerance Assumptions (mm)		Solder Joint															
			Toe (mm)			Heel (mm)			Side (X1) (mm)			Side (X2) (mm)			Side (X3) (mm)		
	F	P	C_L	$J_T$min	$J_T$max	C_S	$J_H$min	$J_H$max	C_{W1}	J_{S1}min	J_{S1}max	C_{W2}	J_{S2}min	J_{S2}max	C_{W3}	J_{S3}min	J_{S3}max
215	0.2	0.2	0.31	0.52	0.68	0.31	0.15	0.30	0.12	0.07	0.13	0.12	0.13	0.19	0.21	0.01	0.12

Figure 4 Tolerance and solder joint analysis



IPC-SM-782

Surface Mount Design and Land Pattern Standard

Date	Section
5/96	8.8
Revision	Subject
A	SOD 123

1.0 SCOPE

This subsection provides the component and land pattern dimensions for SOD 123 (small outline diode) components. Basic construction of the SOD 123 device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

2.0 APPLICABLE DOCUMENTS

See Section 8.0 for documents applicable to the subsections.

2.1 Electronic Industries Association (EIA) JEDEC Publication 95 Registered and Standard Outlines for Solid State and Related Products, DO-214, Issue ''B'' dated 3/91

Application for copies should be addressed to:
Global Engineering Documents
1990 M Street N.W.
Washington, DC

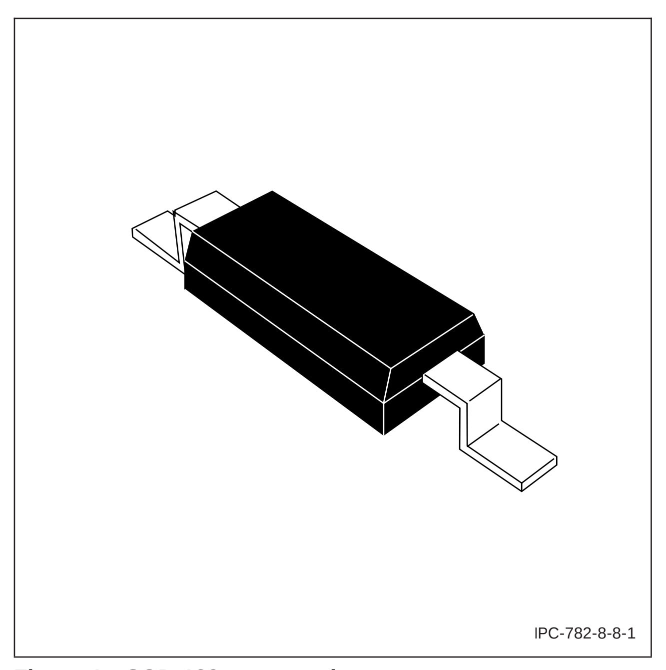


Figure 1 SOD 123 construction

3.0 COMPONENT DESCRIPTIONS

3.1 Basic Construction The small outline diode comes in two configurations. One is gullwing-leaded as shown in Figure 1. The other is molded with terminations as dimensioned in Figure 2.

3.1.1 Termination Materials Leads should be solder-coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the leads by hot dipping or by plating from solution. Plated solder terminations should be subjected to post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

Solder finish applied over precious metal electrodes should have a diffusion barrier layer between the electrode metallization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick.

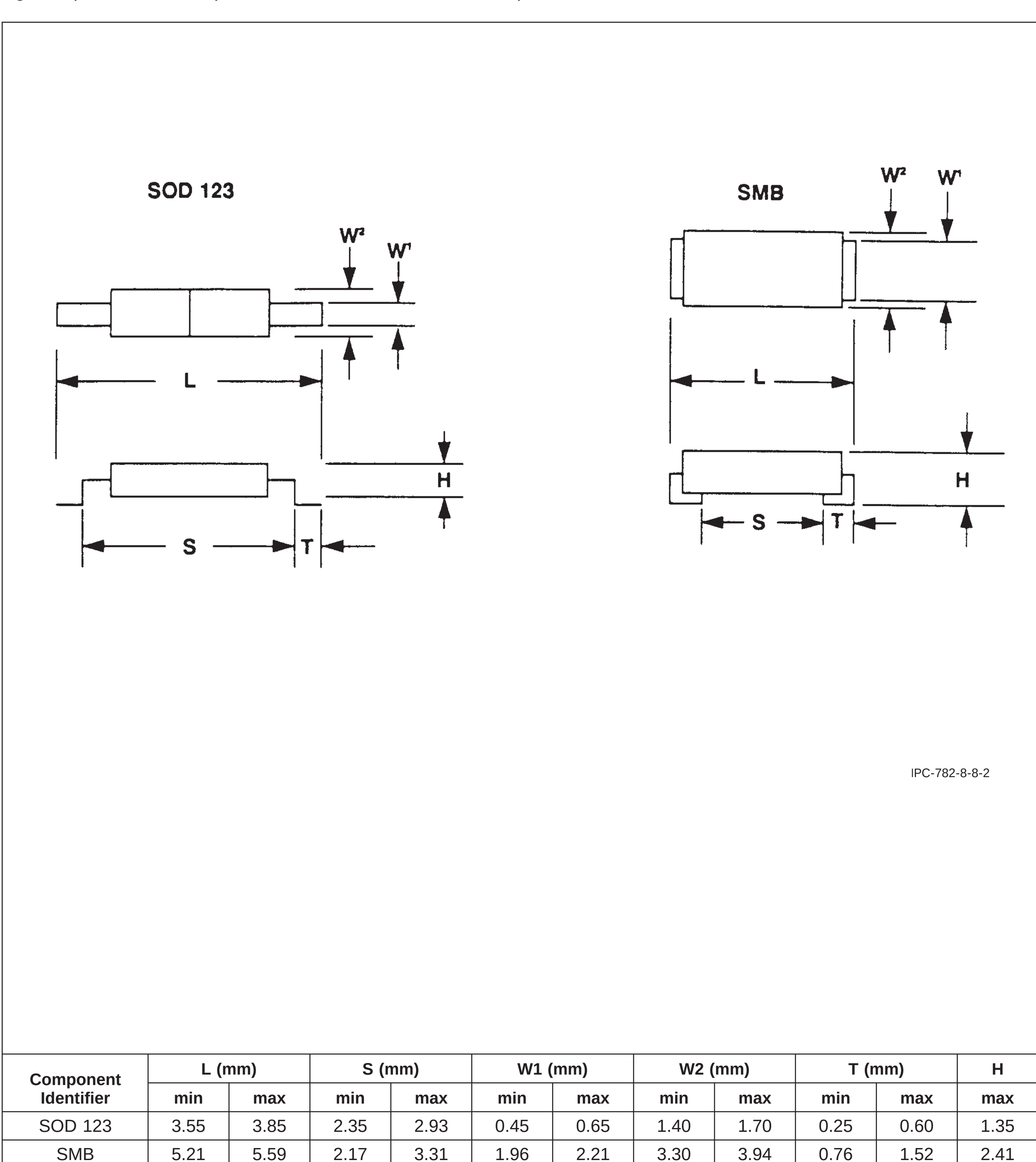
3.1.2 Marking Parts are available with or without marked values.

3.1.3 Carrier Package Format Carrier package formats are tape and reel; 12 mm tape/8 mm pitch.

3.1.4 Resistance to Soldering Parts should be capable of withstanding ten cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260°C.

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for SOD 123 components.



Component Identifier	L (mm)		S (mm)		W1 (mm)		W2 (mm)		T (mm)		H
	min	max	min	max	min	max	min	max	min	max	max
SOD 123	3.55	3.85	2.35	2.93	0.45	0.65	1.40	1.70	0.25	0.60	1.35
SMB	5.21	5.59	2.17	3.31	1.96	2.21	3.30	3.94	0.76	1.52	2.41

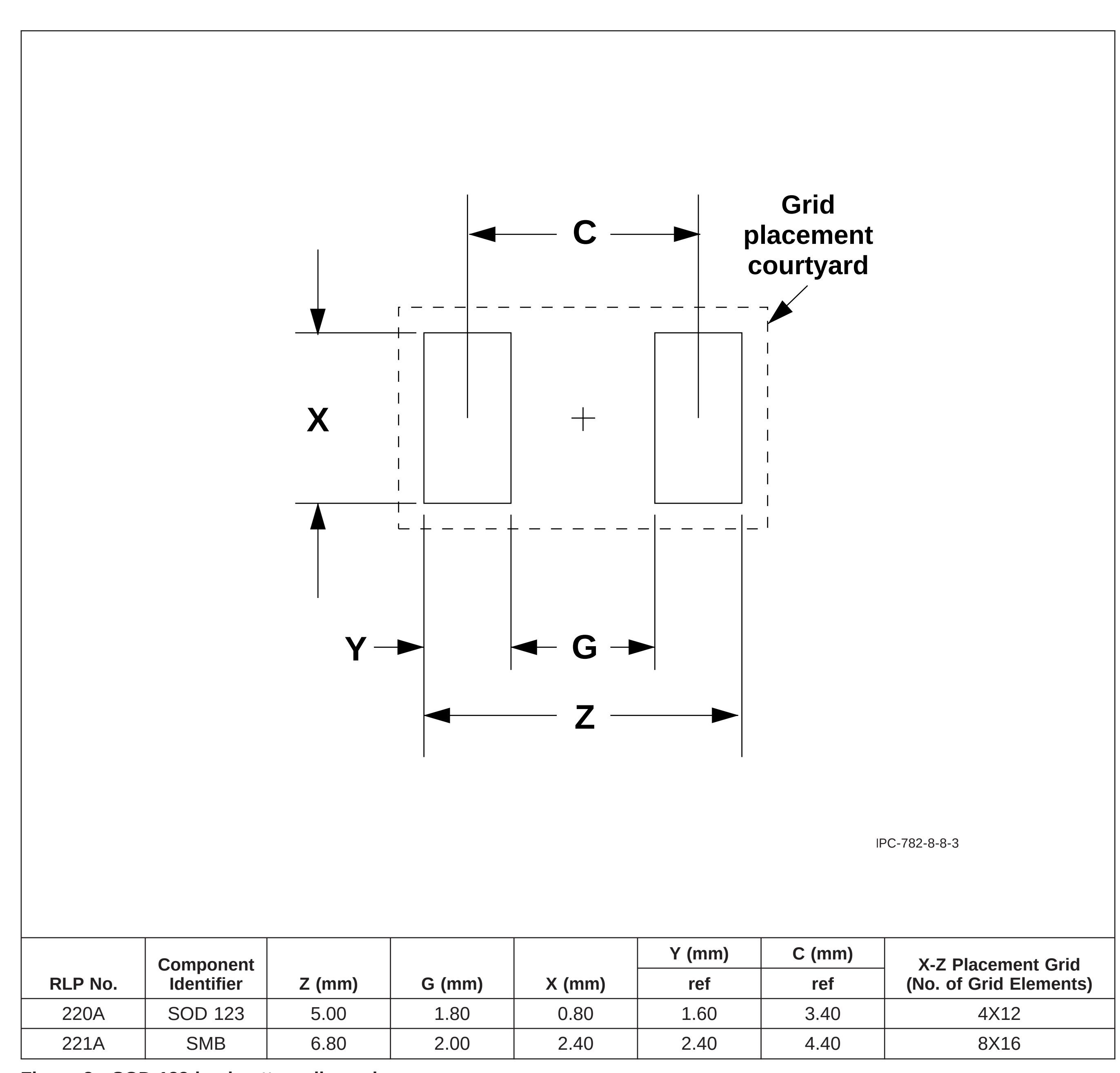
Figure 2 SOD 123 component dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for SOD 123 components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



RLP No.	Component Identifier	Z (mm)	G (mm)	X (mm)	Y (mm) ref	C (mm) ref	X-Z Placement Grid (No. of Grid Elements)
220A	SOD 123	5.00	1.80	0.80	1.60	3.40	4X12
221A	SMB	6.80	2.00	2.40	2.40	4.40	8X16

Figure 3 SOD 123 land pattern dimensions

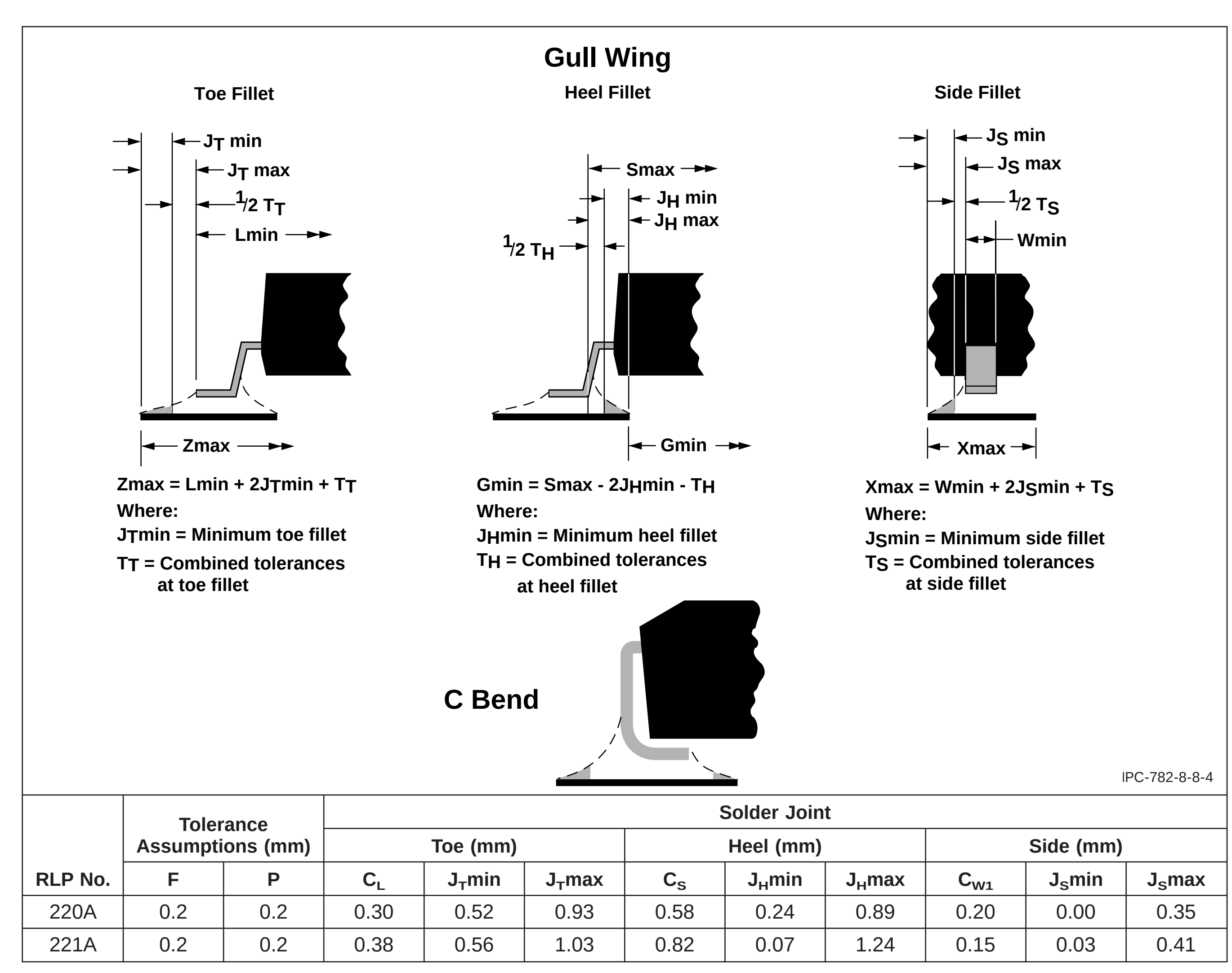
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



RLP No.	Tolerance Assumptions (mm)		Solder Joint								
			Toe (mm)			Heel (mm)			Side (mm)		
	F	P	C_L	$J_T$min	$J_T$max	C_S	$J_H$min	$J_H$max	C_{W1}	$J_S$min	$J_S$max
220A	0.2	0.2	0.30	0.52	0.93	0.58	0.24	0.89	0.20	0.00	0.35
221A	0.2	0.2	0.38	0.56	1.03	0.82	0.07	1.24	0.15	0.03	0.41

Figure 4 Tolerance and solder joint analysis

1.0 SCOPE

This subsection provides the component and land pattern dimensions for SOT 143 (small outline transistor) components. Basic construction of the SOT 143 device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

2.0 APPLICABLE DOCUMENTS

See Section 8.0 for documents applicable to the subsections.

2.1 Electronic Industries Association (EIA) JEDEC Publication 95 Registered and Standard Outlines for Solid State and Related Products, TO-253, Issue ‘‘C’’ dated 11/14/90

Application for copies should be addressed to:
Global Engineering Documents
1990 M Street N.W.
Washington, DC

3.0 COMPONENT DESCRIPTIONS

These parts are for dual diodes and Darlington transistors.

3.1 Basic Construction See Figure 1. The dimensional characteristics are designed to meet the needs of the surface mount industry. The clearance between the body of the component and the packaging and interconnect structure is specified at 0.05 to 0.13 mm [0.002 to 0.005 in] to accommodate reflow or wave soldering processes.

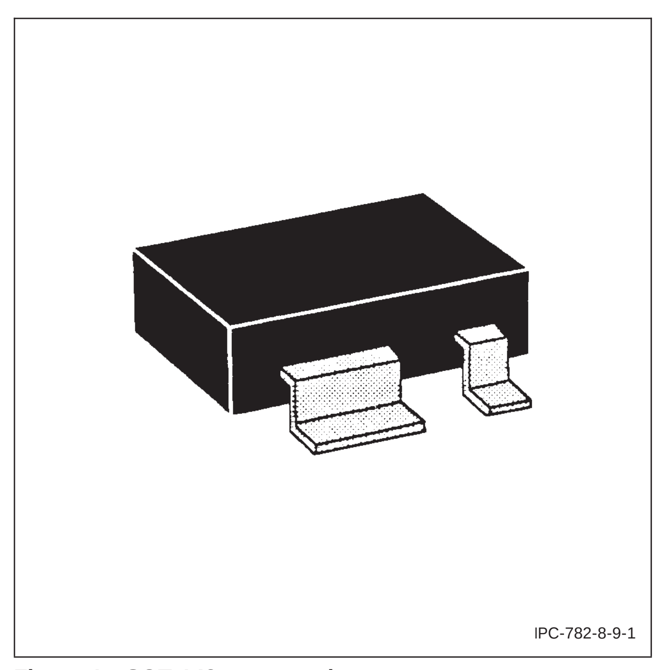


Figure 1 SOT 143 construction

3.1.1 Termination Materials Leads must be solder-coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the leads by hot dipping or by plating from solution. Plated solder terminations should be subjected to post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

Solder finish applied over precious metal electrodes should have a diffusion barrier layer between the electrode metallization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick.

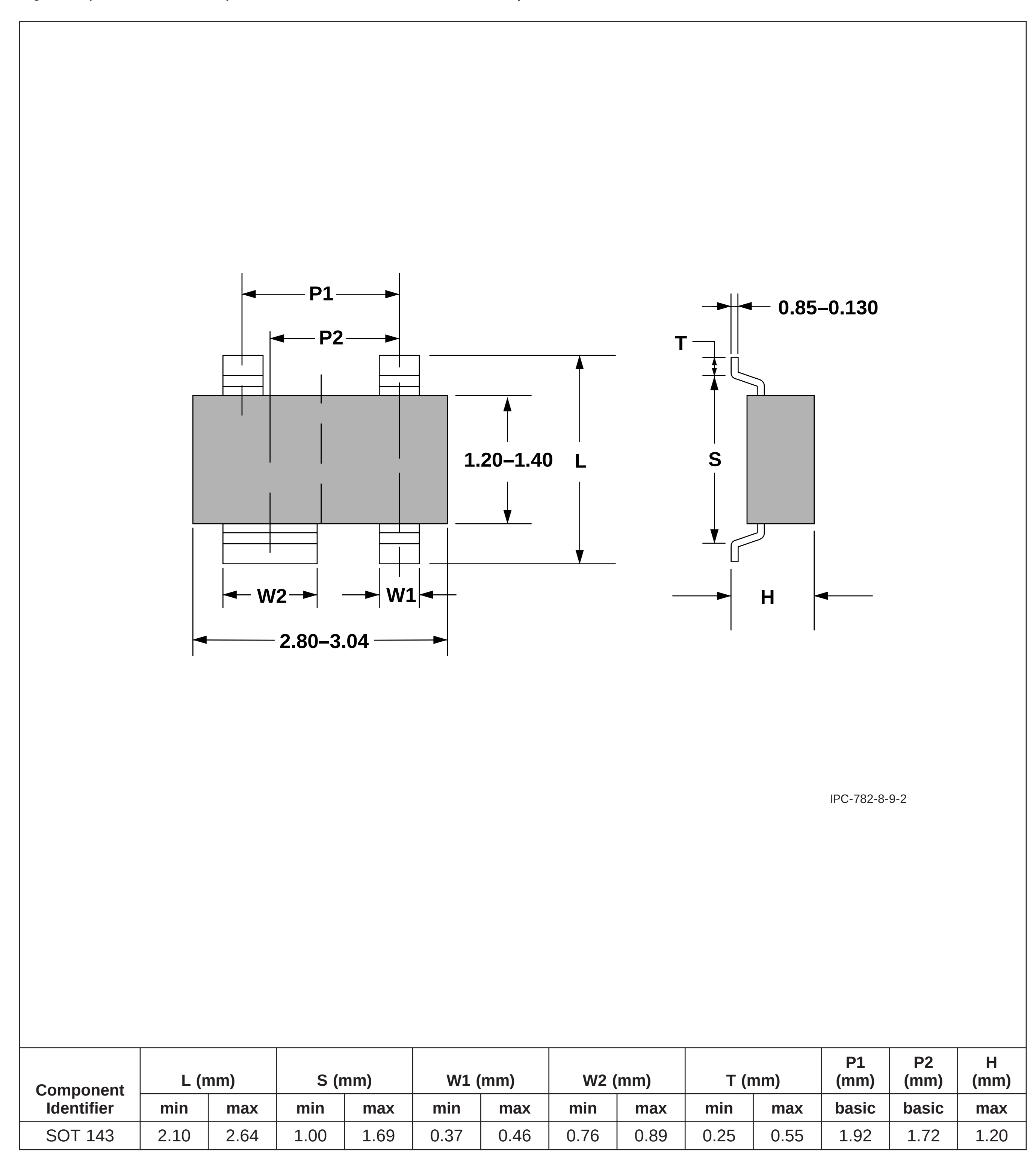
3.1.2 Marking Parts are available with or without marked values.

3.1.3 Carrier Package Format Carrier package format shall be according to the following: body type TO-253, 8 mm tape/4 mm pitch.

3.1.4 Resistance to Soldering Parts should be capable of withstanding five cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260°C.

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for SOT 143 components.



Component Identifier	L (mm)		S (mm)		W1 (mm)		W2 (mm)		T (mm)		P1 (mm)	P2 (mm)	H (mm)
	min	max	min	max	min	max	min	max	min	max	basic	basic	max
SOT 143	2.10	2.64	1.00	1.69	0.37	0.46	0.76	0.89	0.25	0.55	1.92	1.72	1.20

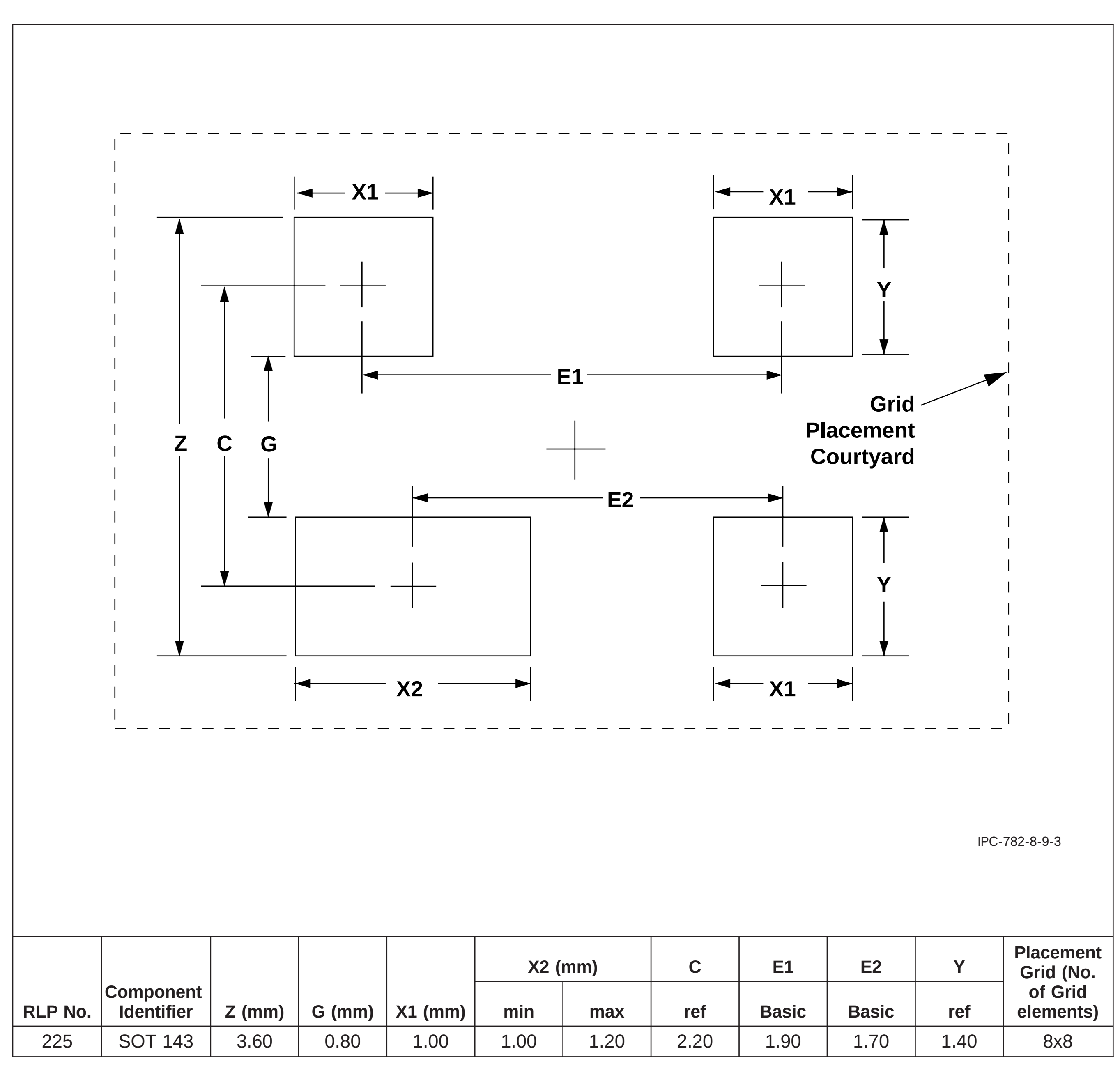
Figure 2 SOT 143 component dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for SOT 143 components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



RLP No.	Component Identifier	Z (mm)	G (mm)	X1 (mm)	X2 (mm)		C	E1	E2	Y	Placement Grid (No. of Grid elements)
					min	max	ref	Basic	Basic	ref	
225	SOT 143	3.60	0.80	1.00	1.00	1.20	2.20	1.90	1.70	1.40	8x8

Figure 3 SOT 143 land pattern dimensions

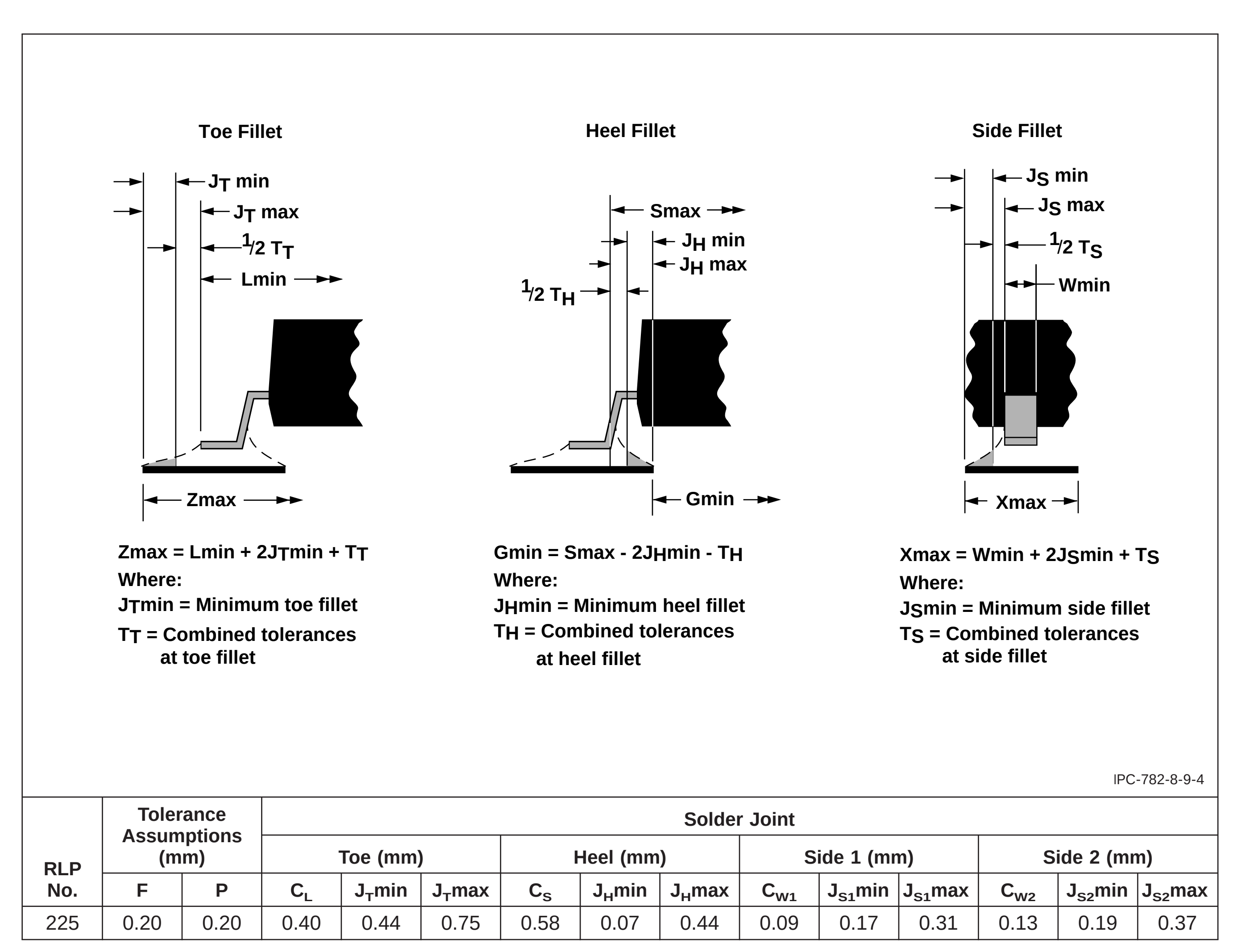
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



RLP No.	Tolerance Assumptions (mm)		Solder Joint											
			Toe (mm)			Heel (mm)			Side 1 (mm)			Side 2 (mm)		
	F	P	C_L	$J_T$min	$J_T$max	C_S	$J_H$min	$J_H$max	C_{W1}	J_{S1}min	J_{S1}max	C_{W2}	J_{S2}min	J_{S2}max
225	0.20	0.20	0.40	0.44	0.75	0.58	0.07	0.44	0.09	0.17	0.31	0.13	0.19	0.37

Figure 4 Tolerance and solder joint analysis

1.0 SCOPE

This subsection provides the component and land pattern dimensions for SOT 223 (small outline transistor) components. Basic construction of the SOT 223 device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

2.0 APPLICABLE DOCUMENTS

See Section 8.0 for documents applicable to the subsections.

2.1 Electronic Industries Association (EIA) JEDEC Publication 95 Registered and Standard Outlines for Solid State and Related Products, TO-261, Issue ''C'' dated 1/90

Application for copies should be addressed to:
Global Engineering Documents
1990 M Street N.W.
Washington, DC

3.0 COMPONENT DESCRIPTIONS

These parts are for dual diodes and Darlington transistors.

3.1 Basic Construction See Figure 1. The dimensional characteristics are designed to meet the needs of the surface mount industry. The clearance between the body of the component and the packaging and interconnect structure is specified at 0.06 mm (basic) to accommodate reflow or wave soldering processes.

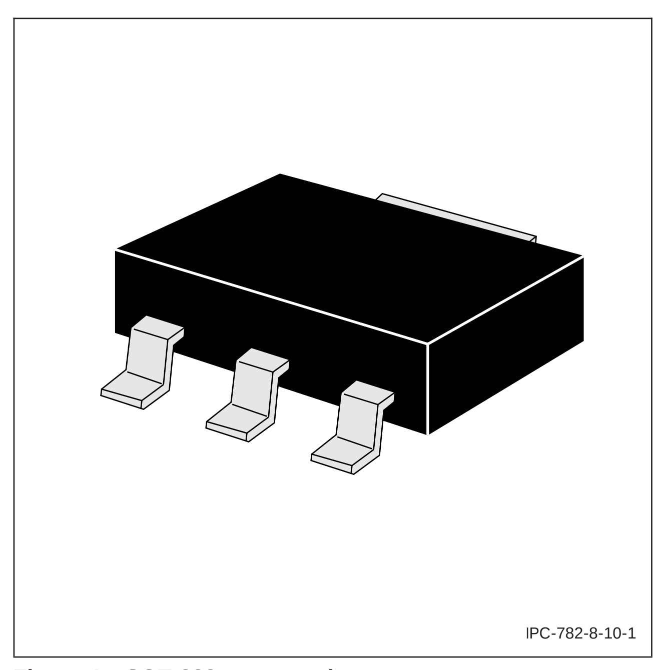


Figure 1 SOT 223 construction

3.1.1 Termination Materials Leads should be solder-coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the leads by hot dipping or by plating from solution. Plated solder terminations should be subjected to post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

Solder finish applied over precious metal electrodes should have a diffusion barrier layer between the electrode metallization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick.

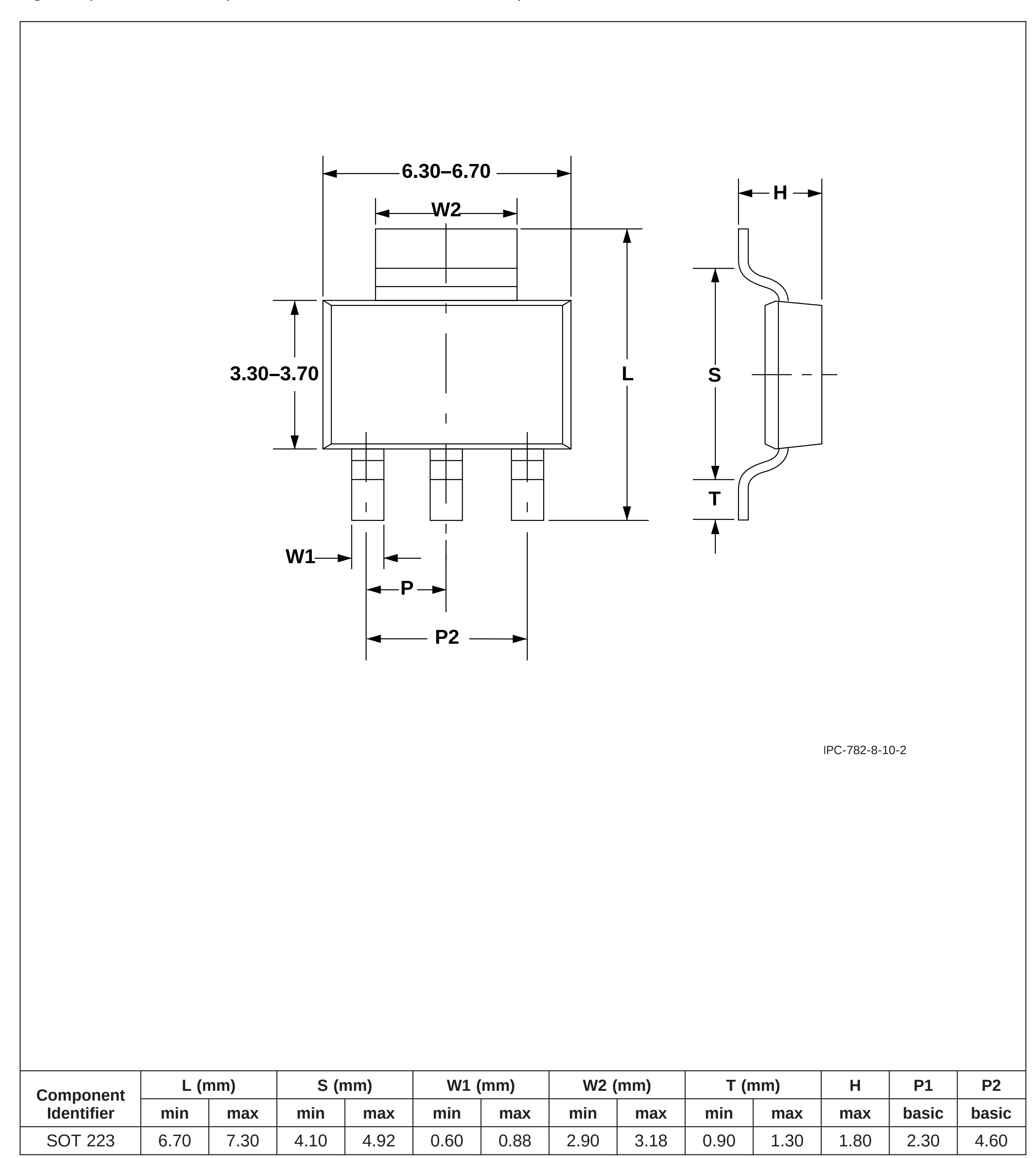
3.1.2 Marking Parts are available with or without marked values.

3.1.3 Carrier Package Format Carrier package format shall be according to the following: body type TO-261, 12 mm tape/8 mm pitch.

3.1.4 Resistance to Soldering Parts should be capable of withstanding five cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260°C.

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for SOT 223 components.



Component Identifier	L (mm)		S (mm)		W1 (mm)		W2 (mm)		T (mm)		H	P1	P2
	min	max	min	max	min	max	min	max	min	max	max	basic	basic
SOT 223	6.70	7.30	4.10	4.92	0.60	0.88	2.90	3.18	0.90	1.30	1.80	2.30	4.60

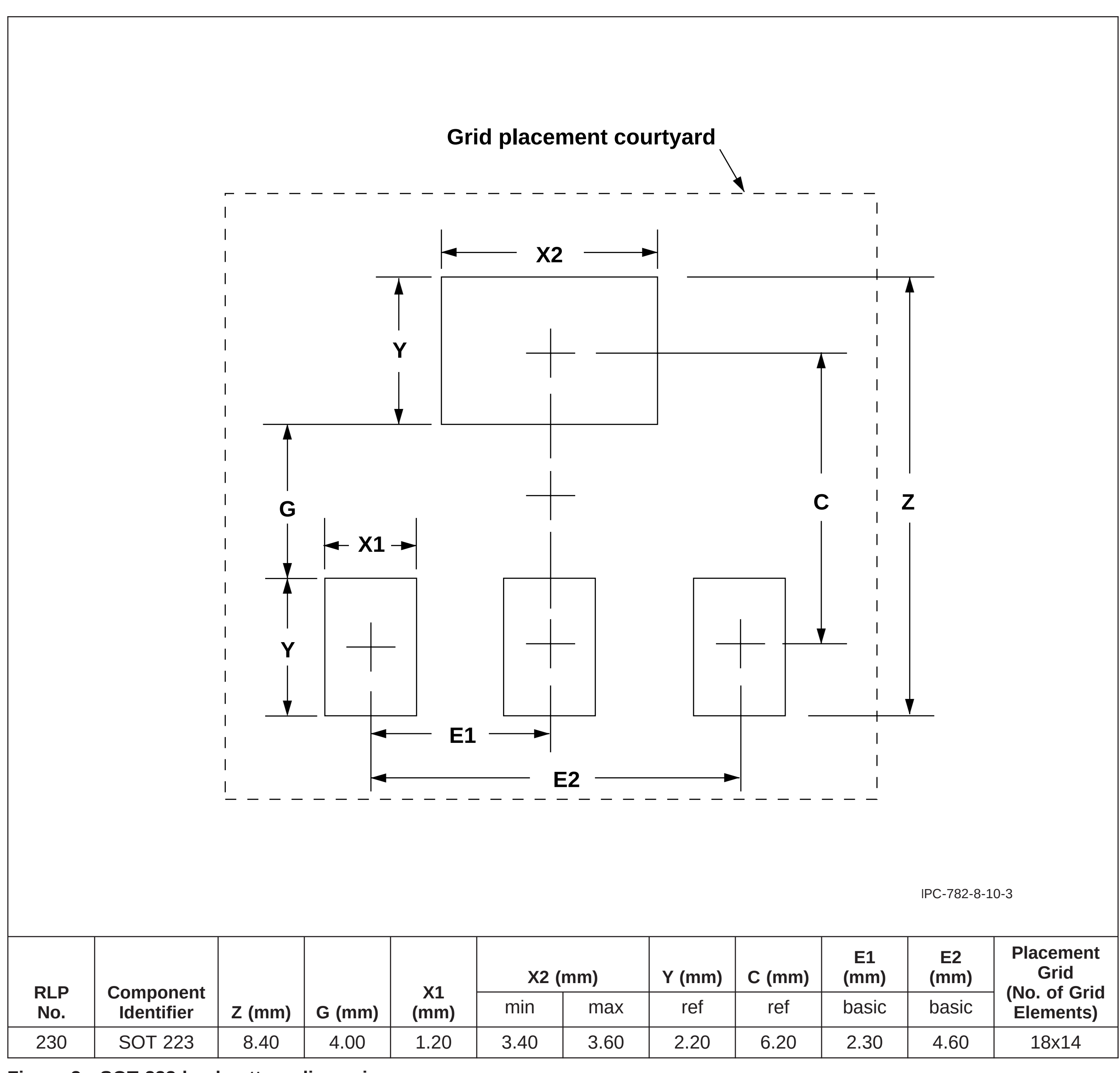
Figure 2 SOT 223 component dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for SOT 223 components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



RLP No.	Component Identifier	Z (mm)	G (mm)	X1 (mm)	X2 (mm)		Y (mm)	C (mm)	E1 (mm)	E2 (mm)	Placement Grid (No. of Grid Elements)
					min	max	ref	ref	basic	basic	
230	SOT 223	8.40	4.00	1.20	3.40	3.60	2.20	6.20	2.30	4.60	18x14

Figure 3 SOT 223 land pattern dimensions

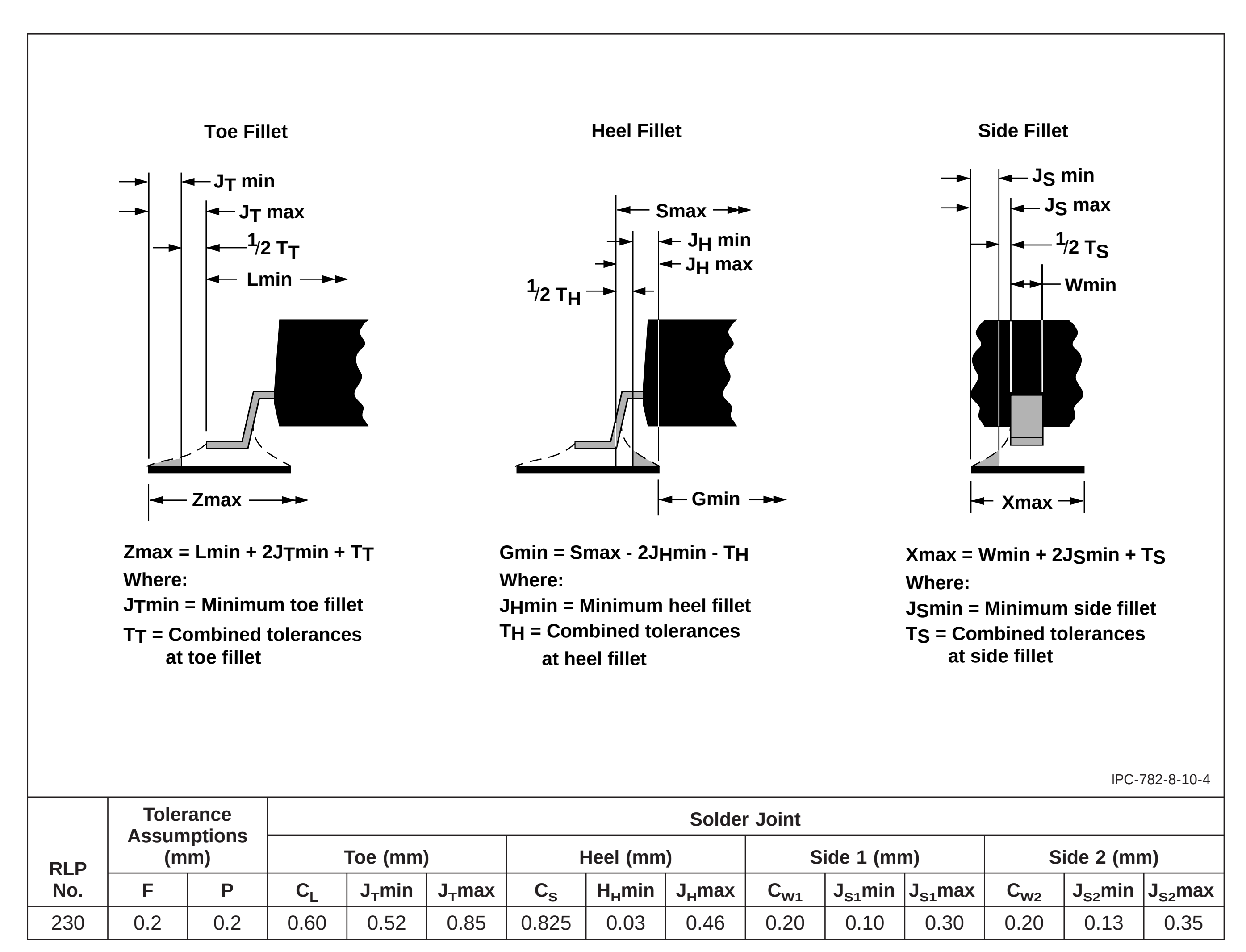
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



RLP No.	Tolerance Assumptions (mm)		Solder Joint											
			Toe (mm)			Heel (mm)			Side 1 (mm)			Side 2 (mm)		
	F	P	C_L	$J_T$min	$J_T$max	C_S	$H_H$min	$J_H$max	C_{W1}	J_{S1}min	J_{S1}max	C_{W2}	J_{S2}min	J_{S2}max
230	0.2	0.2	0.60	0.52	0.85	0.825	0.03	0.46	0.20	0.10	0.30	0.20	0.13	0.35

Figure 4 Tolerance and solder joint analysis

1.0 SCOPE

This subsection provides the component and land pattern dimensions for TO 252 (small outline transistor) components. Basic construction of the TO 252 device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

2.0 APPLICABLE DOCUMENTS

See Section 8.0 for documents applicable to the subsections.

2.1 Electronic Industries Association (EIA) JEDEC Publication 95 Registered and Standard Outlines for Solid State and Related Products, TO-252, Issue ''B'' dated 9/88

Application for copies should be addressed to:
Global Engineering Documents
1990 M Street N.W.
Washington, DC

3.0 COMPONENT DESCRIPTIONS

These parts are for dual diodes and Darlington transistors.

3.1 Basic Construction See Figure 1.

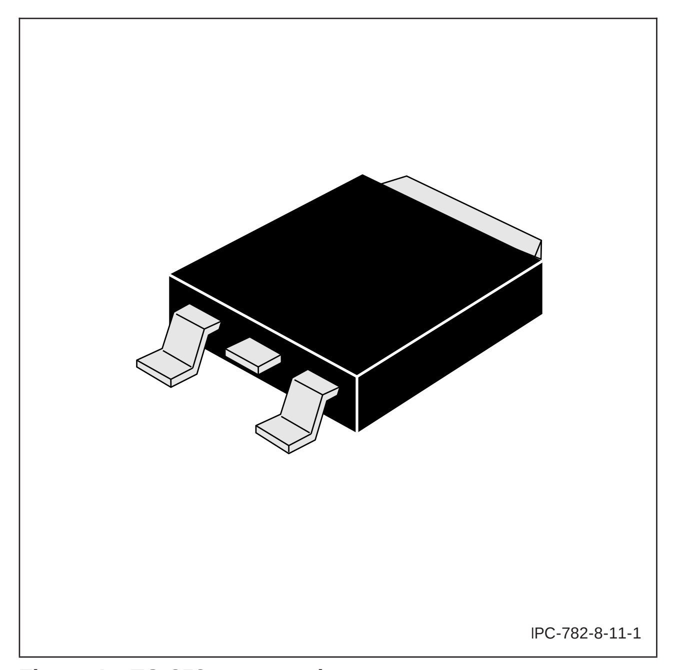


Figure 1 TO 252 construction

3.1.1 Termination Materials Leads should be solder-coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the leads by hot dipping or by plating from solution. Plated solder terminations should be subjected to post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

Solder finish applied over precious metal electrodes should have a diffusion barrier layer between the electrode metallization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick.

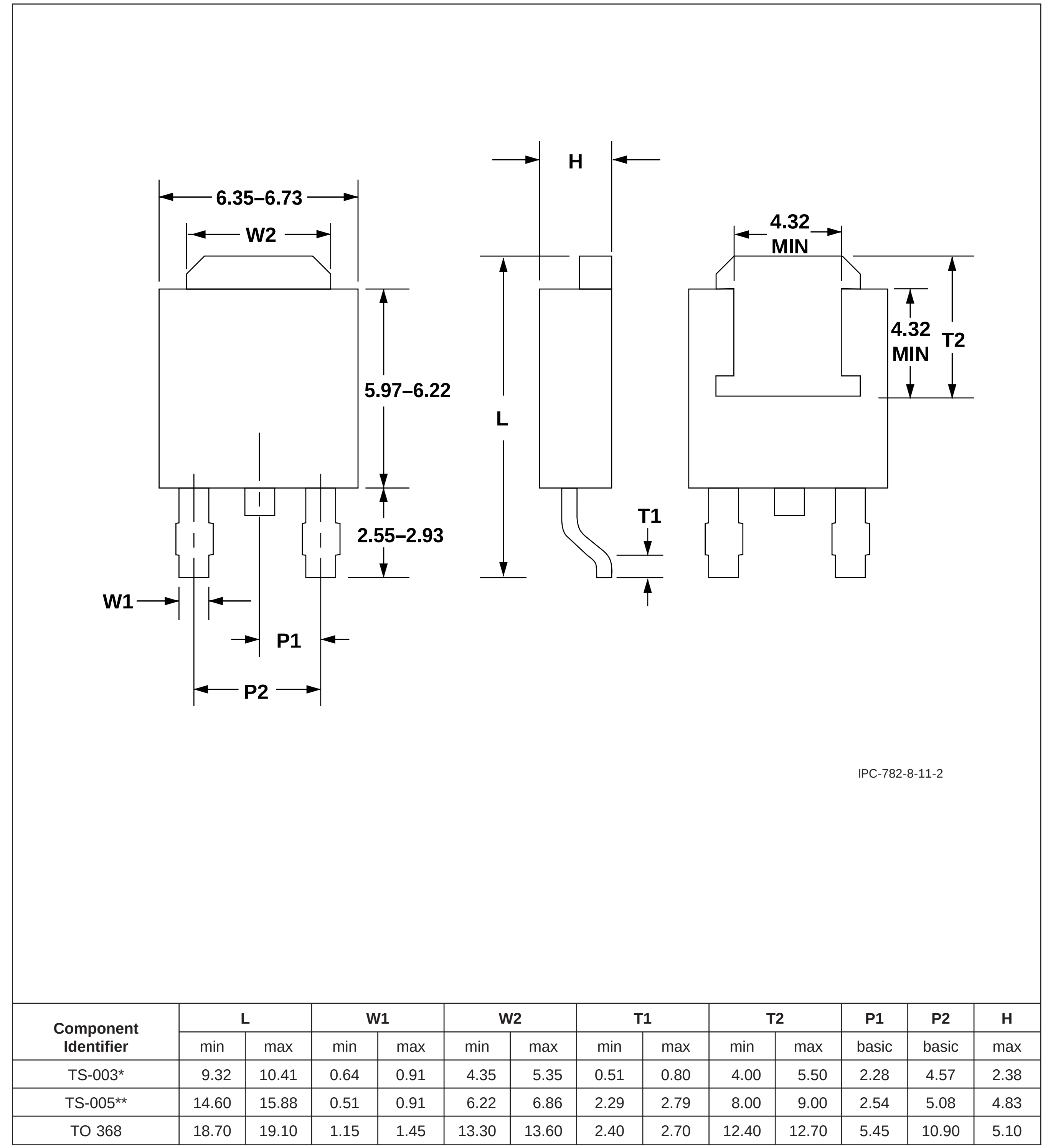
3.1.2 Marking Parts are available with or without marked values.

3.1.3 Carrier Package Format Carrier package format shall be according to the following: body type TO-252, 12 mm tape/8 mm pitch.

3.1.4 Resistance to Soldering Parts should be capable of withstanding five cycles through a relow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260°C.

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for TO 252 components.



Component Identifier	L		W1		W2		T1		T2		P1	P2	H
	min	max	min	max	min	max	min	max	min	max	basic	basic	max
TS-003*	9.32	10.41	0.64	0.91	4.35	5.35	0.51	0.80	4.00	5.50	2.28	4.57	2.38
TS-005**	14.60	15.88	0.51	0.91	6.22	6.86	2.29	2.79	8.00	9.00	2.54	5.08	4.83
TO 368	18.70	19.10	1.15	1.45	13.30	13.60	2.40	2.70	12.40	12.70	5.45	10.90	5.10

Figure 2 TO 252 component dimensions

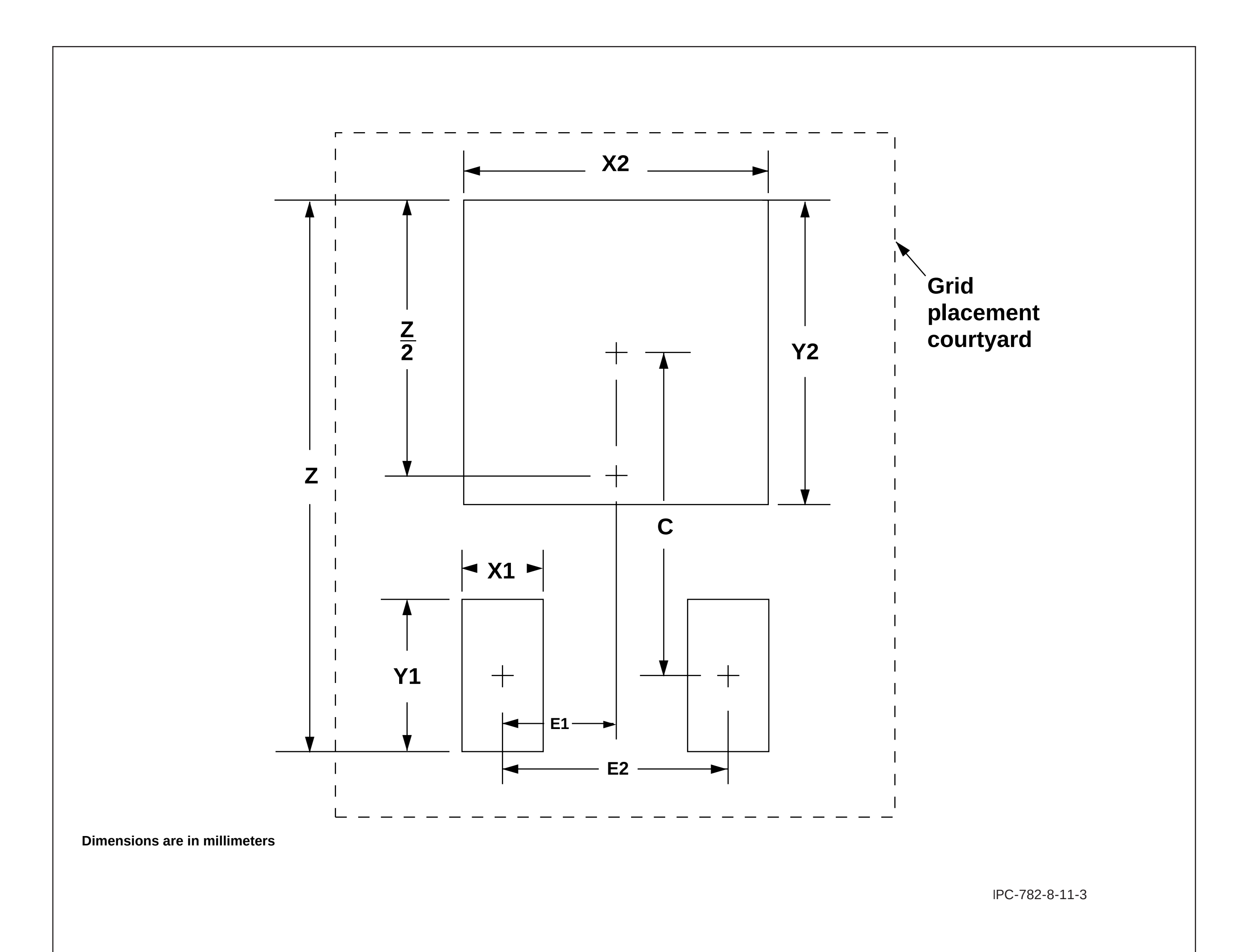
*Formerly TO 252
**Formerly TO 263

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for TO 252 components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



RLP No.	Component Identifier	Z (mm)	Y1 (mm)	Y2 (mm)	X1 (mm)	X2 (mm)	C (mm) ref	Placement Grid (No. of Grid Elements)
235A	TS-003*	11.20	1.60	6.20	1.00	5.40	7.30	24x16
236	TS-005**	16.60	3.40	9.60	1.00	6.80	10.10	36x24
237	TO 268	19.80	3.40	13.40	1.40	13.60	11.40	42x34

Figure 3 TO 252 land pattern dimensions

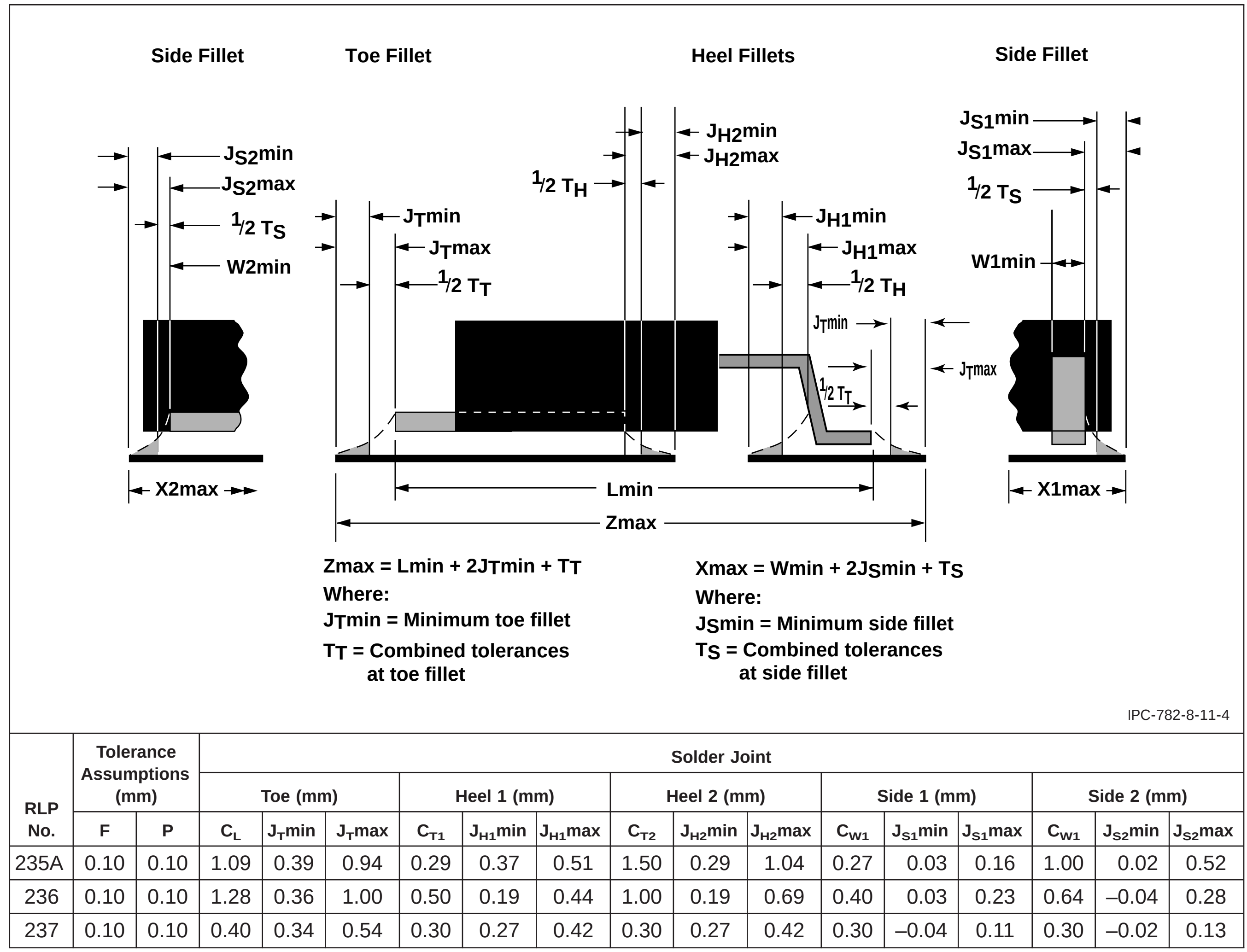
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



RLP No.	Tolerance Assumptions (mm)		Solder Joint														
			Toe (mm)			Heel 1 (mm)			Heel 2 (mm)			Side 1 (mm)			Side 2 (mm)		
	F	P	C_L	$J_T$min	$J_T$max	C_{T1}	J_{H1}min	J_{H1}max	C_{T2}	J_{H2}min	J_{H2}max	C_{W1}	J_{S1}min	J_{S1}max	C_{W1}	J_{S2}min	J_{S2}max
235A	0.10	0.10	1.09	0.39	0.94	0.29	0.37	0.51	1.50	0.29	1.04	0.27	0.03	0.16	1.00	0.02	0.52
236	0.10	0.10	1.28	0.36	1.00	0.50	0.19	0.44	1.00	0.19	0.69	0.40	0.03	0.23	0.64	–0.04	0.28
237	0.10	0.10	0.40	0.34	0.54	0.30	0.27	0.42	0.30	0.27	0.42	0.30	–0.04	0.11	0.30	–0.02	0.13

Figure 4 Tolerance and solder joint analysis

1.0 INTRODUCTION This section covers land patterns for components with gullwings on two sides. Each subsection contains information in accordance with the following format:

1.0 Scope
2.0 Applicable Documents
3.0 General Component Description (Figure 1)
4.0 Component Dimensions (Figure 2)
5.0 Land Pattern Dimensions (Figure 3)
6.0 Tolerance and Solder Joint Analysis (Figure 4)

The following is the table of contents for this section:

Table of Contents
Components with Gullwing Leads on Two Sides

2.0 APPLICABLE DOCUMENTS

The following documents, of the issue in effect on the revision date of this section, form a part of this specification to the extent specified herein.

2.1 Electronic Industries Association (EIA)[1]

EIA-481-A Taping of Surface Mount Components for Automatic Placement

2.2 International Electrotechnical Commission (IEC)[2]

IEC 97 Grid Elements

2.3 Electronic Industries Association of Japan[3]

IC-74-1 General Rules for Preparation of Outline Drawings of Integrated Circuits

IC-74-2 General Rules for Preparation of Outline Drawings of Integrated Circuits, Thin Small Outline Packages

3.0 General Information

3.1 General Component Description The two-sided gull wing family has a number of generic package sizes in the family. The body sizes are varied, but the basic family is characterized by 1.27 mm or 0.63 mm lead centers with leads on the long side of a rectangular body. The family has been expanded to include a limited number of 0.80, 0.65, 0.50, 0.40, and 0.3 mm pitch devices.

Within the component families, body width and lead span are constant, while body length changes as the lead count changes.

A major advantage of this package style is that it can be pretested prior to substrate assembly while still offering relatively high density. Its small area, low height, and minimal weight are its major advantages over DIPs. The package has orientation features on the edge of the package to aid in handling and identification.

Coplanarity is an issue for all components with gullwings on two sides. In general, the leads must be coplanar within 0.1 mm. That is, when the component is placed on a flat surface, (e.g., a granite block), no lead may be more than 0.1 mm off the flat surface.

3.2 Process Considerations Some members of the SOIC family are processed on the secondary side and wave soldered. When parts are processed by wave solder, correct part orientation must be observed. Consult your manufacturer before placing SOIC's on the wave solder side of the board.

High lead count packages and fine pitch parts, 0.63 mm or less, should be processed by infrared reflow, conduction reflow, or hot bar soldering, and should not be wave soldered.

1. Application for copies of EIA and EIAJ documents should be addressed to EIA, 2001 Pennsylvania Ave N.W., Washington, DC, 20006-1813 or Global Engineering Documents, 1990 M St. N.W., Washington, DC 20036.
2. Application for copies should be addressed to IEC, 3 rue de Varembe, PO Box 131 - 1211 Geneva 20, Switzerland

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IPC-SM-782

Surface Mount Design and Land Pattern Standard

Date	Section
5/96	9.1
Revision	**Subject**
A	SOIC

1.0 SCOPE

This subsection provides the component and land pattern dimensions for small outline integrated circuits (SOIC components) with gullwing leads. Basic construction of the SOIC device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

2.0 APPLICABLE DOCUMENTS

See Section 9.0 for documents applicable to the subsections.

3.0 COMPONENT DESCRIPTIONS

These components are all on 1.27 mm pitch, and are available in narrow body (3.90 mm), wide body (7.50 mm) and extra wide body (8.90 mm) sizes, ranging from 8 to 36 pins.

3.1 Basic Construction See Figure 1. Basic construction consists of a plastic body and metallic leads.

3.1.1 Termination Materials Leads should be solder-coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the termination by hot dipping or by plating from solution. Plated solder terminations should be subjected to a post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.00075 mm [0.0003 in] thick.

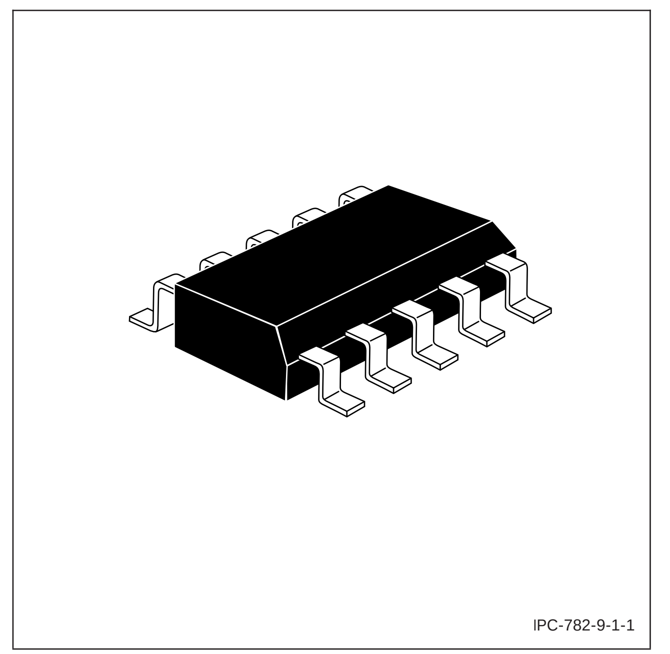


Figure 1 SOIC construction

Solder finish applied over precious-metal leads shall have a diffusion-barrier layer between the lead metallization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick.

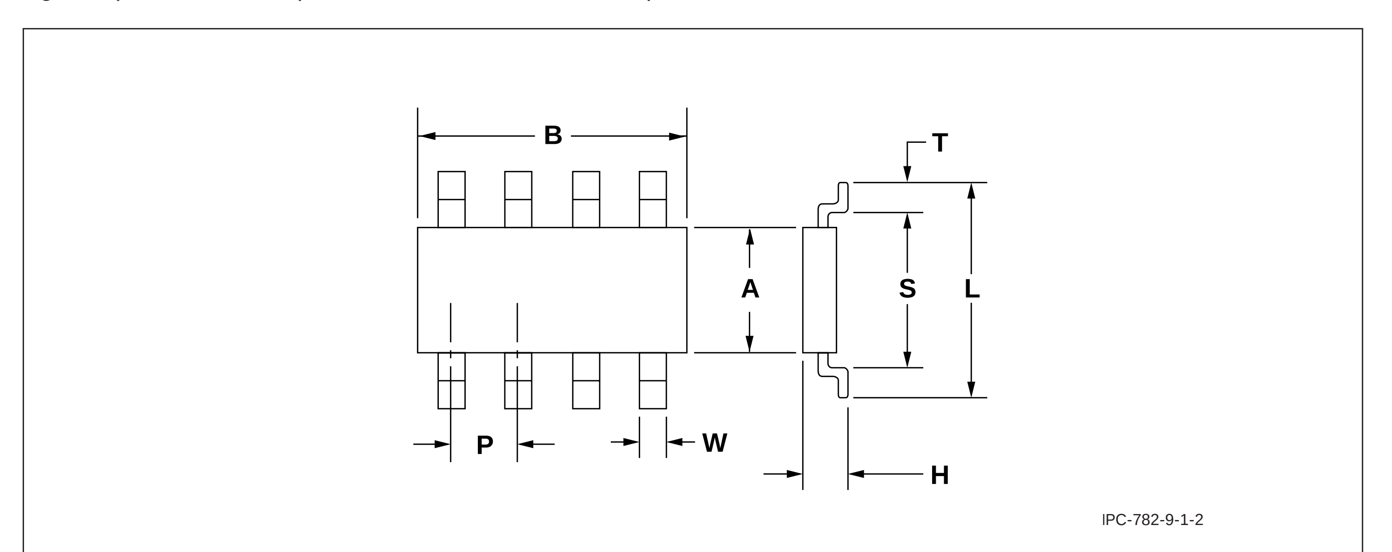
3.1.2 Marking All parts shall be marked with a part number and ‘‘Pin 1’’ location. ‘‘Pin 1’’ location may be molded into the plastic body.

3.1.3 Carrier Package Format Bulk rods, 24 mm tape/ 8–12 mm pitch is preferred for best handling. Tube carriers are also used.

3.1.4 Resistance to Soldering Parts should be capable of withstanding ten cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260°C.

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for SOIC components.



Component Identifier	JEDEC Number	L (mm)		S (mm)		W (mm)		T (mm)		A (mm)		B (mm)		H (mm)		P (mm)
		min	max	min	max	min	max	min	max	min	max	min	max	min	max	basic
S08	MS-012 AA	5.80	6.20	3.26	4.55	0.33	0.51	0.40	1.27	3.80	4.00	4.80	5.00	1.35	1.75	1.27
S08W	—	10.00	10.65	7.46	8.85	0.33	0.51	0.40	1.27	7.40	7.60	5.05	5.45	2.35	2.65	1.27
S014	MS-012 AB	5.80	6.20	3.26	4.55	0.33	0.51	0.40	1.27	3.80	4.00	8.55	8.75	1.35	1.75	1.27
S014 W	—	10.00	10.65	7.46	8.85	0.33	0.51	0.40	1.27	7.40	7.60	8.80	9.20	2.35	2.65	
S016	MS-012 AC	5.80	6.20	3.26	4.55	0.33	0.51	0.40	1.27	3.80	4.00	9.80	10.00	1.35	1.75	1.27
S016W	MS-013 AA	10.00	10.65	7.46	8.85	0.33	0.51	0.40	1.27	7.40	7.60	10.10	10.50	2.35	2.65	1.27
S020W	MS-013 AC	10.00	10.65	7.46	8.85	0.33	0.51	0.40	1.27	7.40	7.60	12.60	13.00	2.35	2.65	1.27
S024W	MO-119 AA	10.29	10.64	8.21	9.01	0.36	0.51	0.53	1.04	7.40	7.60	15.54	15.85	2.34	2.64	1.27
S024X	MO-120 AA	11.81	12.17	9.73	10.54	0.36	0.51	0.53	1.04	8.76	9.02	15.54	15.85	2.34	2.64	1.27
S028W	MO-119 AB	10.29	10.64	8.21	9.01	0.36	0.51	0.53	1.04	7.40	7.60	18.08	18.39	2.34	2.64	1.27
S028X	MO-120 AB	11.81	12.17	9.73	10.54	0.36	0.51	0.53	1.04	8.76	9.02	18.08	18.39	2.34	2.64	1.27
S032W	MO-119 AC	10.29	10.64	8.21	9.01	0.36	0.51	0.53	1.04	7.40	7.60	20.62	20.93	2.34	2.64	1.27
S032X	MO-120 AC	11.81	12.17	9.73	10.54	0.36	0.51	0.53	1.04	8.76	9.02	20.62	20.93	2.34	2.64	1.27
S036W	MO-119 AD	10.29	10.64	8.21	9.01	0.36	0.51	0.53	1.04	7.40	7.60	23.16	23.47	2.34	2.64	1.27
S036X	MO-120 AD	11.81	12.17	9.73	10.54	0.36	0.51	0.53	1.04	8.76	9.02	23.16	23.47	2.34	2.64	1.27

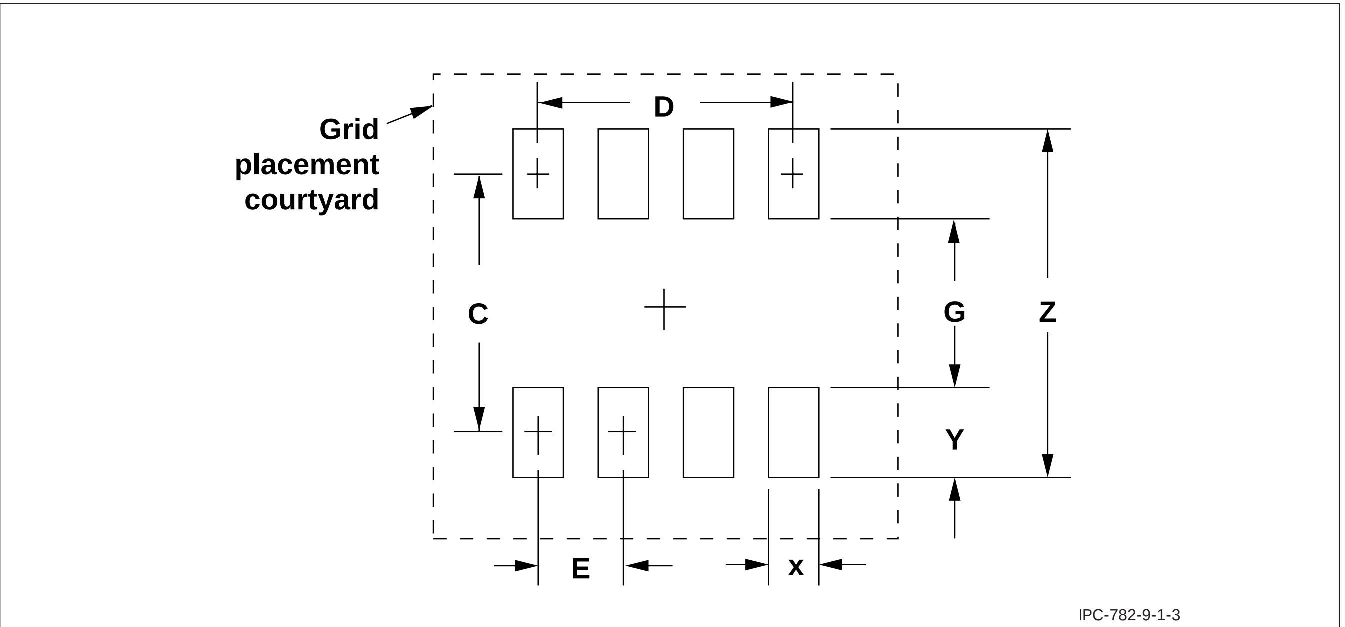
Figure 2 SOIC component dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for SOIC components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



RLP No.	Component Identifier	Z (mm)	G (mm)	X (mm)	Y (mm) ref	C (mm) ref	D (mm) ref	E (mm) ref	Placement Grid (No. Grid Elements)
300A	S08	7.40	3.00	0.60	2.20	5.20	3.81	1.27	16x12
301A	S08W	11.40	7.00	0.60	2.20	9.20	3.81	1.27	24x12
302A	S014	7.40	3.00	0.60	2.20	5.20	7.62	1.27	16x20
303A	S014W	11.40	7.00	0.60	2.20	9.20	7.62	1.27	24x20
304A	S016	7.40	3.00	0.60	2.20	5.20	8.89	1.27	16x22
305A	S016W	11.40	7.00	0.60	2.20	9.20	8.89	1.27	24x22
306A	S020W	11.40	7.00	0.60	2.20	9.20	11.43	1.27	24x28
307A	S024W	11.40	7.00	0.60	2.20	9.20	13.97	1.27	24x32
308A	S024X	13.00	8.60	0.60	2.20	10.80	13.97	1.27	28x32
309A	S028W	11.40	7.00	0.60	2.20	9.20	16.51	1.27	24x38
310A	S028X	13.00	8.60	0.60	2.20	10.80	16.51	1.27	28x38
311A	S032W	11.40	7.00	0.60	2.20	9.20	19.05	1.27	24x44
312A	S032X	13.00	8.60	0.60	2.20	10.80	19.05	1.27	28x44
313A	S036W	11.40	7.00	0.60	2.20	9.20	21.59	1.27	24x48
314A	S036X	13.00	8.60	0.60	2.20	10.80	21.59	1.27	28x48

Figure 3 SOIC land pattern dimensions

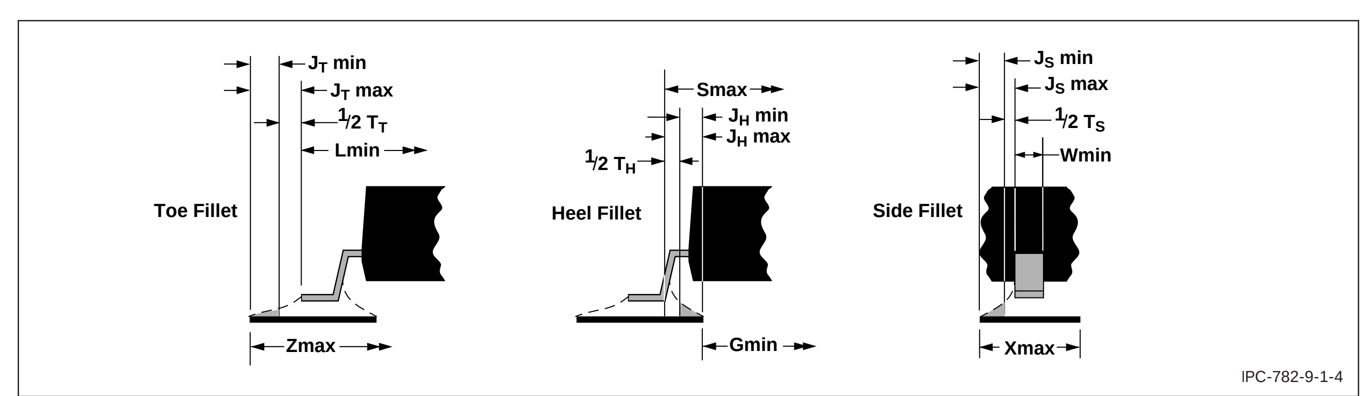
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



RLP No.	Tolerance Assumptions (mm)		Solder Joint: Toe (mm)			Heel (mm)			Side (mm)		
	F	P	C_L	$J_T$min	$J_T$max	C_S	$J_H$min	$J_H$max	C_W	$J_S$min	$J_S$max
300A	0.10	0.10	0.40	0.59	0.80	1.29	0.13	0.78	0.18	0.02	0.14
301A	0.10	0.10	0.65	0.37	0.70	1.39	0.23	0.93	0.18	0.02	0.14
302A	0.10	0.10	0.40	0.59	0.80	1.29	0.13	0.78	0.18	0.02	0.14
303A	0.10	0.10	0.65	0.37	0.70	1.39	0.23	0.93	0.18	0.02	0.14
304A	0.10	0.10	0.40	0.59	0.80	1.29	0.13	0.78	0.18	0.02	0.14
305A	0.10	0.10	0.65	0.37	0.70	1.39	0.23	0.93	0.18	0.02	0.14
306A	0.10	0.10	0.65	0.37	0.70	1.39	0.23	0.93	0.18	0.02	0.14
307A	0.10	0.10	0.35	0.37	0.56	0.80	0.60	1.01	0.15	0.02	0.12
308A	0.10	0.10	0.36	0.40	0.60	0.81	0.56	0.97	0.15	0.02	0.12
309A	0.10	0.10	0.35	0.37	0.56	0.80	0.60	1.01	0.15	0.02	0.12
310A	0.10	0.10	0.36	0.40	0.60	0.81	0.56	0.97	0.15	0.02	0.12
311A	0.10	0.10	0.35	0.37	0.56	0.80	0.60	1.01	0.15	0.02	0.12
312A	0.10	0.10	0.36	0.40	0.60	0.81	0.56	0.97	0.15	0.02	0.12
313A	0.10	0.10	0.35	0.37	0.56	0.80	0.60	1.01	0.15	0.02	0.12
314A	0.10	0.10	0.36	0.40	0.60	0.81	0.56	0.97	0.15	0.02	0.12

Figure 4 Tolerance and solder joint analysis



IPC-SM-782

Surface Mount Design and Land Pattern Standard

Date	Section
5/96	9.2
Revision	Subject
A	SSOIC

1.0 SCOPE

This subsection provides the component and land pattern dimensions for small outline integrated circuits (SSOIC components) with gullwing leads. Basic construction of the SSOIC device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

2.0 APPLICABLE DOCUMENTS

See Section 9.0 and the following for documents applicable to this subsection.

2.1 Electronic Industries Association

JEDEC Publication 95 Registered and Standard Outlines for Solid State and Related Products, ''Small Outline Gullead, 12 mm Body, 0.80 mm lead Spacing,'' Outline M0-117, issue ''A,'' and ''Shrink Small Outline Package Family, 7.62 mm body, 0.635 mm,'' Outline MO-018, issue ''A''

Application for copies should be addressed to:
Global Engineering Documents
1990 M Street N.W.,
Washington,DC

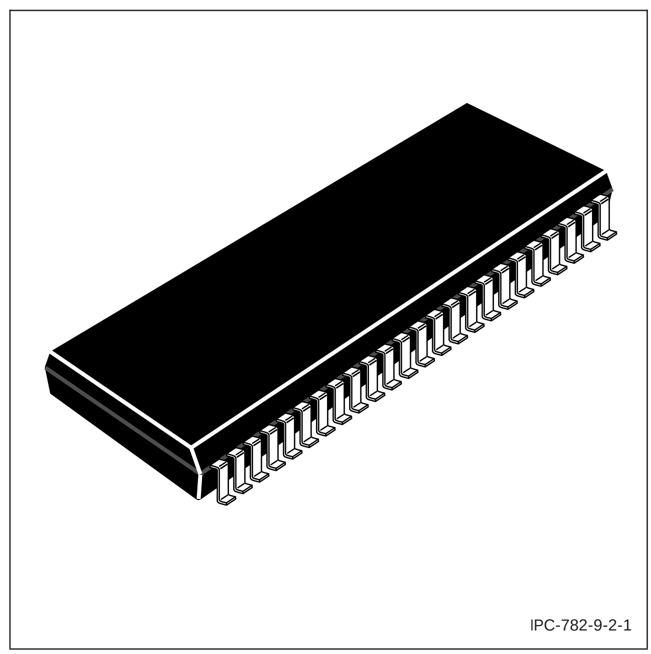


Figure 1 SSOIC construction

3.0 COMPONENT DESCRIPTIONS

These components are all on 0.635 mm pitch, and are available in wide body (7.50 mm) and extra wide body (12.00 mm) sizes, ranging from 48 to 64 pins.

3.1 Basic Construction See Figure 1. Basic construction consists of a plastic body and metallic leads.

3.1.1 Termination Materials Leads should be solder-coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the termination by hot dipping or by plating from solution. Plated solder terminations should be subjected to a post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.00075 mm [0.0003 in] thick.

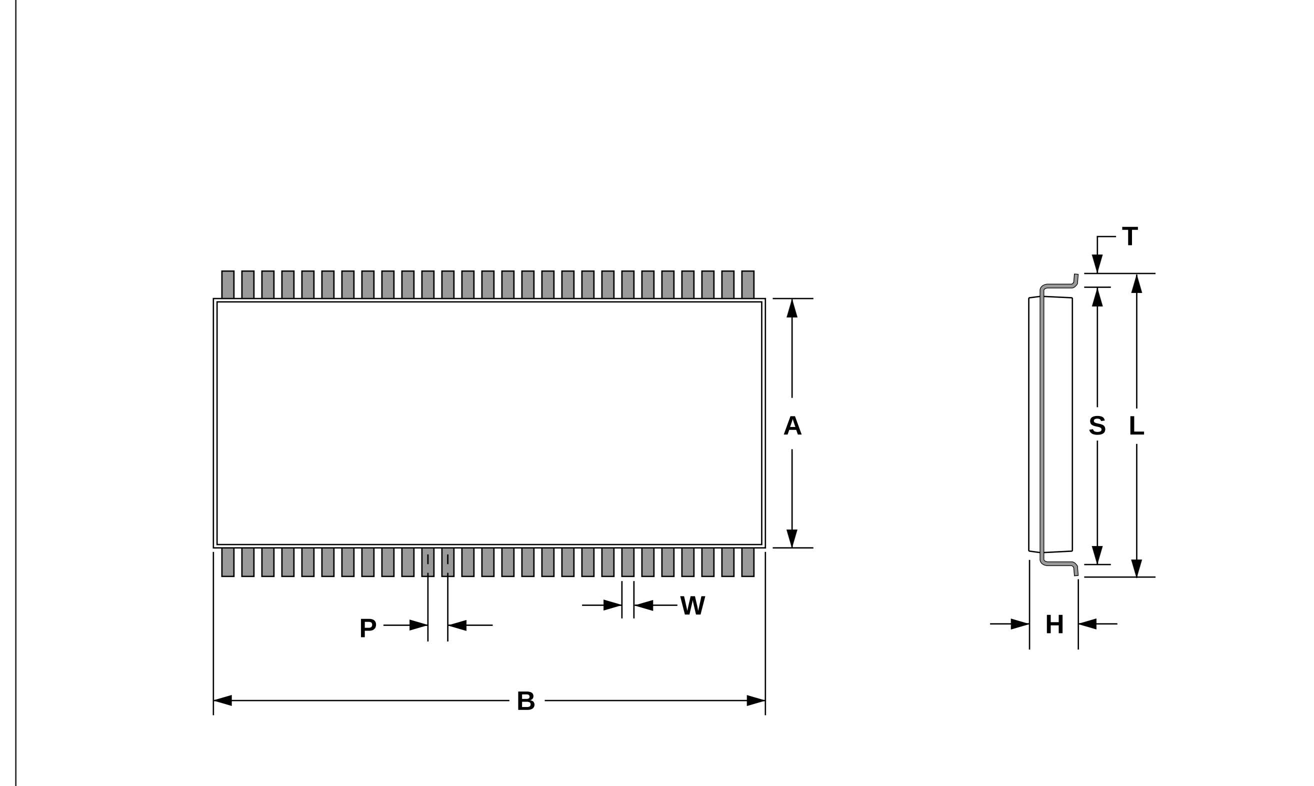
3.1.2 Marking All parts shall be marked with a part number and ''Pin 1'' location. ''Pin 1'' location may be molded into the plastic body.

3.1.3 Carrier Package Format Bulk rods, 24 mm tape/ 8–12 mm pitch is preferred for best handling. Tube carriers are also used.

3.1.4 Resistance to Soldering Parts should be capable of withstanding ten cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260°C.

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for SSOIC components.



Component Identifier	JEDEC Number	L (mm)		S (mm)		W (mm)		A (mm)		B (mm)		H (mm)		T (mm)		P (mm)
		min	max	min	max	min	max	min	max	min	max	min	max	min	max	basic
SS048	M0118 AA	10.03	10.67	7.99	8.95	0.20	0.30	7.40	7.60	15.75	16.00	2.41	2.20	0.51	1.02	0.635
SS056	M0118 AB	10.03	10.67	7.99	8.95	0.20	0.30	7.40	7.60	18.29	18.54	2.41	2.20	0.51	1.02	0.635
S064	M0117	14.00	14.50	12.40	13.05	0.30	0.45	11.90	12.10	26.17	26.43	1.92	2.00	0.51	0.80	0.800

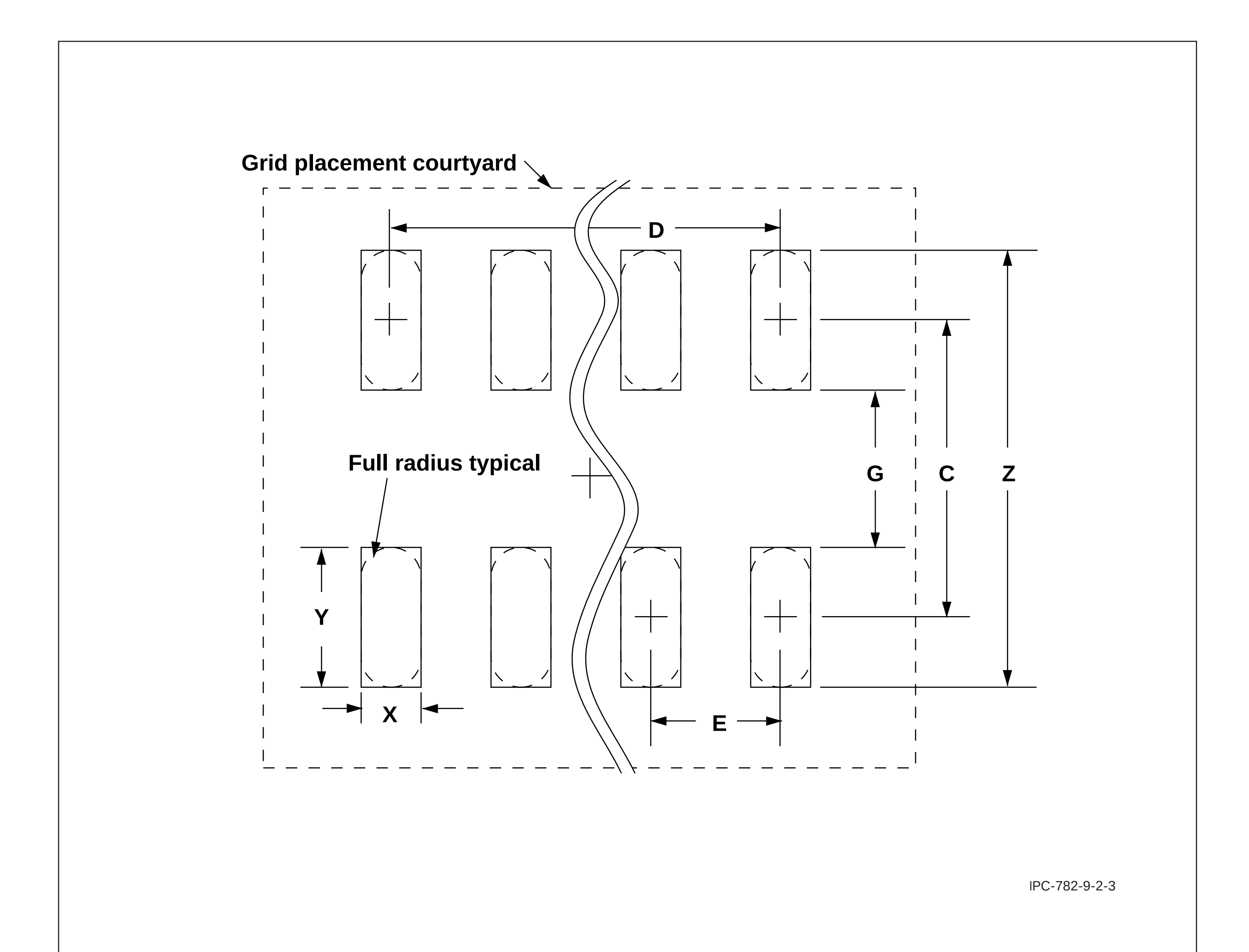
Figure 2 SSOIC component dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for SSOIC components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



RLP No.	Component Identifier	Z (mm)	G (mm)	X (mm)	Y ref (mm)	C ref (mm)	D ref (mm)	E ref (mm)	Placement Grid (No. Grid Elements)
330A	SS048	11.60	7.20	0.40	2.20	9.40	14.61	0.64	24x34
331A	SS056	11.60	7.20	0.40	2.20	9.40	17.15	0.64	24x38
332A	S064	15.40	11.40	0.50	2.00	13.40	24.80	0.80	32x54

Figure 3 SSOIC land pattern dimensions

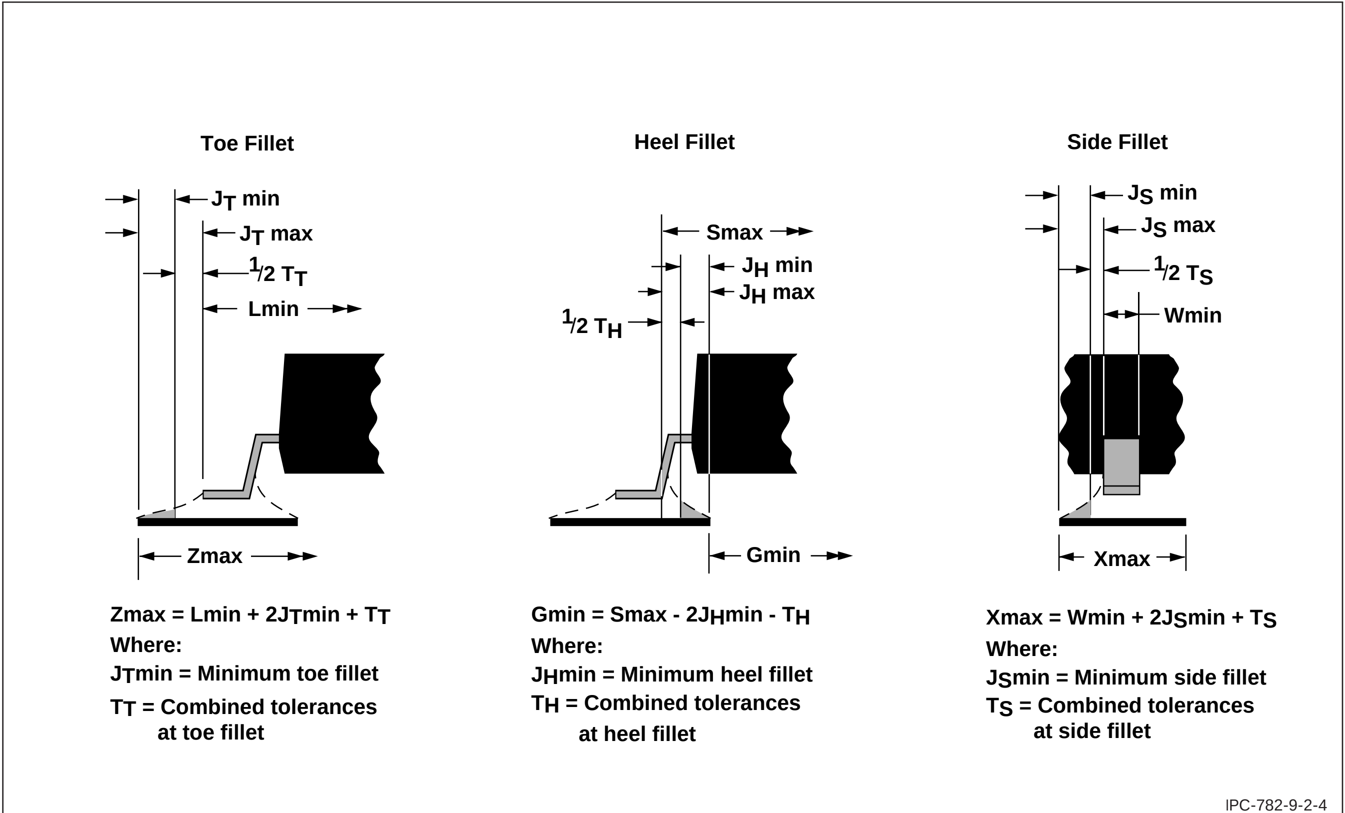
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



RLP No.	Tolerance Assumptions (mm)		Solder Joint								
			Toe (mm)			Heel (mm)			Side (mm)		
	F	P	C_L	$T_T$min	$J_T$max	C_S	$J_H$min	$J_H$max	C_W	$J_S$min	$J_S$max
330A	0.10	0.10	0.64	0.46	0.79	0.96	0.39	0.88	0.10	0.01	0.10
331A	0.10	0.10	0.64	0.46	0.79	0.96	0.39	0.88	0.10	0.01	0.10
332A	0.10	0.10	0.50	0.44	0.70	0.65	0.49	0.82	0.15	0.00	0.10

Figure 4 Tolerance and solder joint analysis

Surface Mount Design and Land Pattern Standard

1.0 SCOPE

This subsection provides component and land pattern dimensions for small outline packages (SOP components) with gullwing leads on two sides. Basic construction of the SOP device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

2.0 APPLICABLE DOCUMENTS

See Section 9.0 and the following for documents applicable to this subsection.

2.1 Electronic Industries Association of Japan (EIAJ)

EIAJ-7402-1 General Rules for the Preparation of Outine Drawings of Integrated Circuits Small Outline Packages

3.0 COMPONENT DESCRIPTIONS

3.1 Basic Construction IPC-SM-782 has defined center-to-center spacing for the land pattern slightly differently than is indicated in the EIAJ specification ED 7402-1.

This specification allows for 6 families of the SOP. EIAJ classifies the families by the center-to-center distance of the land patterns and the outer extremities of the leads (dimension ‘‘L’’ in IPC-SM-782). The basic construction of the SOP specified by EIAJ is the same construction as for SOIC specified by JEDEC. Both have gullwing leads on 1.27 mm centers.

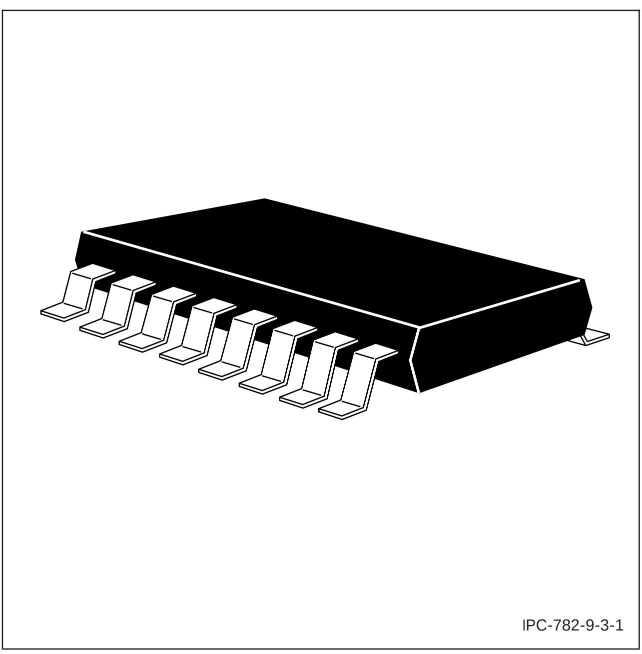


Figure 1 SOPIC construction

The EIAJ specification allows for a number of positions of the components to be in any of the families (e.g., body width). The sizes shown in Figure 2 are the most common, however, there are Type II SOP 14s and there are also Type I SOP 16s. See Figure 2.

3.1.1 Termination Materials Leads must be solder-coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the leads by hot dipping or by plating from solution. Plated solder terminations should be subjected to post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

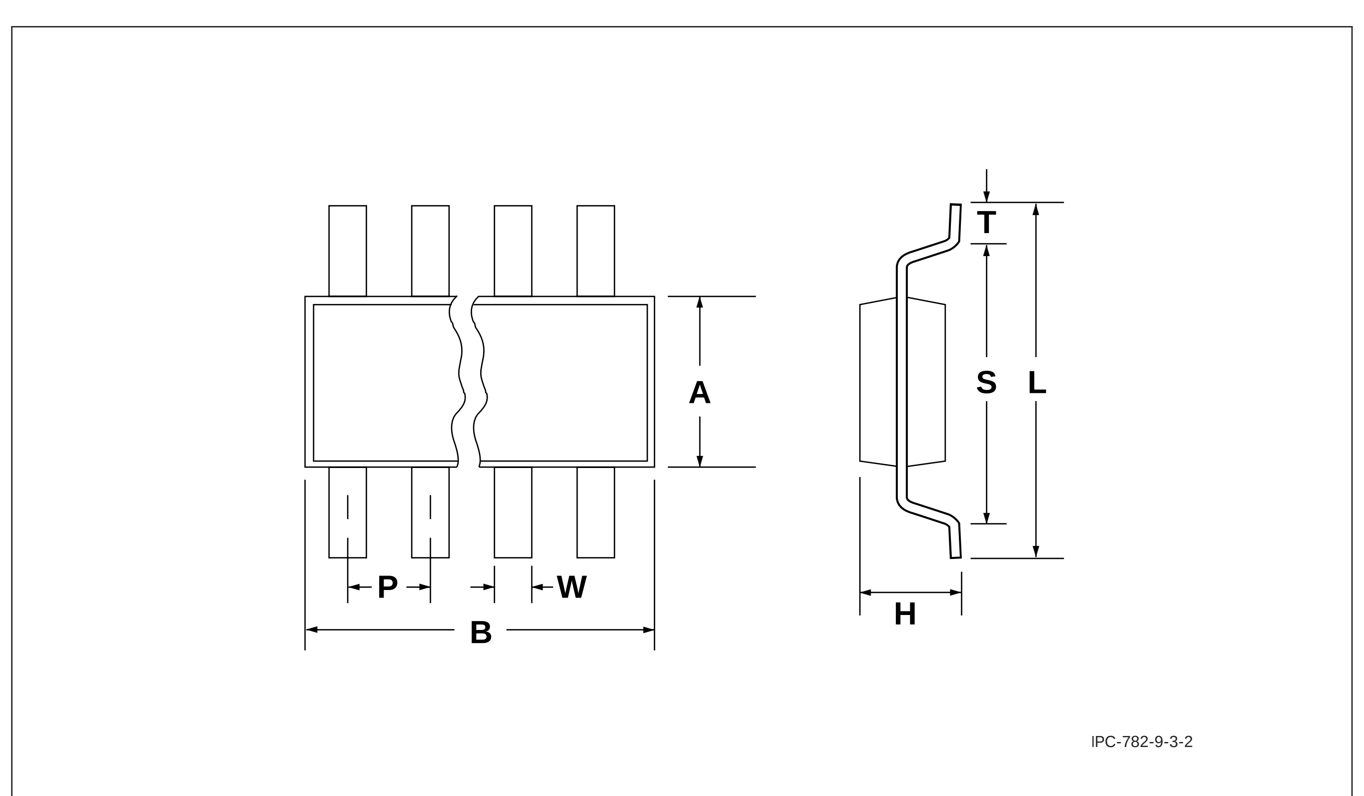
3.1.2 Marking Parts are available with or without part number markings. Usually an index mark indicates pin 1.

3.1.3 Carrier Package Format Bulk rods, 24 mm tape/8–12 mm pitch is preferred for best handling. Tube carriers are also used.

3.1.4 Resistance to Solder Parts should be capable of withstanding ten cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260°C.

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for SOPIC components.



Component Identifier (mm)	Type	L (mm)		S (mm)		W (mm)		T (mm)		A (mm)		B (mm)	H (mm)	P (mm)
		min	max	min	max	min	max	min	max	min	max	max	max	basic
SOP 6	I	5.72	6.99	3.72	5.11	0.35	0.51	0.60	1.00	3.92	4.72	6.35	1.5	1.27
SOP 8	I	5.72	6.99	3.72	5.11	0.35	0.51	0.60	1.00	3.92	4.72	6.35	1.5	1.27
SOP 10	I	5.72	6.99	3.72	5.11	0.35	0.51	0.60	1.00	3.92	4.72	8.89	1.5	1.27
SOP 12	I	5.72	6.99	3.72	5.11	0.35	0.51	0.60	1.00	3.92	4.72	8.89	1.5	1.27
SOP 14	I	5.72	6.99	3.72	5.11	0.35	0.51	0.60	1.00	3.92	4.72	11.43	1.5	1.27
SOP 16	II	7.62	8.89	5.62	7.01	0.35	0.51	0.60	1.00	5.02	6.22	11.43	2.0	1.27
SOP 18	II	7.62	8.89	5.62	7.01	0.35	0.51	0.60	1.00	5.02	6.22	13.97	2.0	1.27
SOP 20	II	7.62	8.89	5.62	7.01	0.35	0.51	0.60	1.00	5.02	6.22	13.97	2.0	1.27
SOP 22	III	9.53	10.80	7.53	8.92	0.35	0.51	0.60	1.00	6.33	8.13	16.51	2.5	1.27
SOP 24	III	9.53	10.80	7.53	8.92	0.35	0.51	0.60	1.00	6.33	8.13	16.51	2.5	1.27
SOP 28	IV	11.43	12.70	9.43	10.82	0.35	0.51	0.60	1.00	8.23	10.03	19.05	3.0	1.27
SOP 30	IV	11.43	12.70	9.43	10.82	0.35	0.51	0.60	1.00	8.23	10.03	21.59	3.0	1.27
SOP 32	V	13.34	14.61	11.34	12.73	0.35	0.51	0.60	1.00	10.14	11.94	21.59	3.5	1.27
SOP 36	V	13.34	14.61	11.34	12.73	0.36	0.51	0.60	1.00	10.14	11.94	24.13	3.5	1.27
SOP 40	VI	15.24	16.51	13.24	14.63	0.35	0.51	0.60	1.00	12.04	13.84	27.94	4.0	1.27
SOP 42	VI	15.24	16.51	13.24	14.63	0.35	0.51	0.60	1.00	12.04	13.84	27.94	4.0	1.27

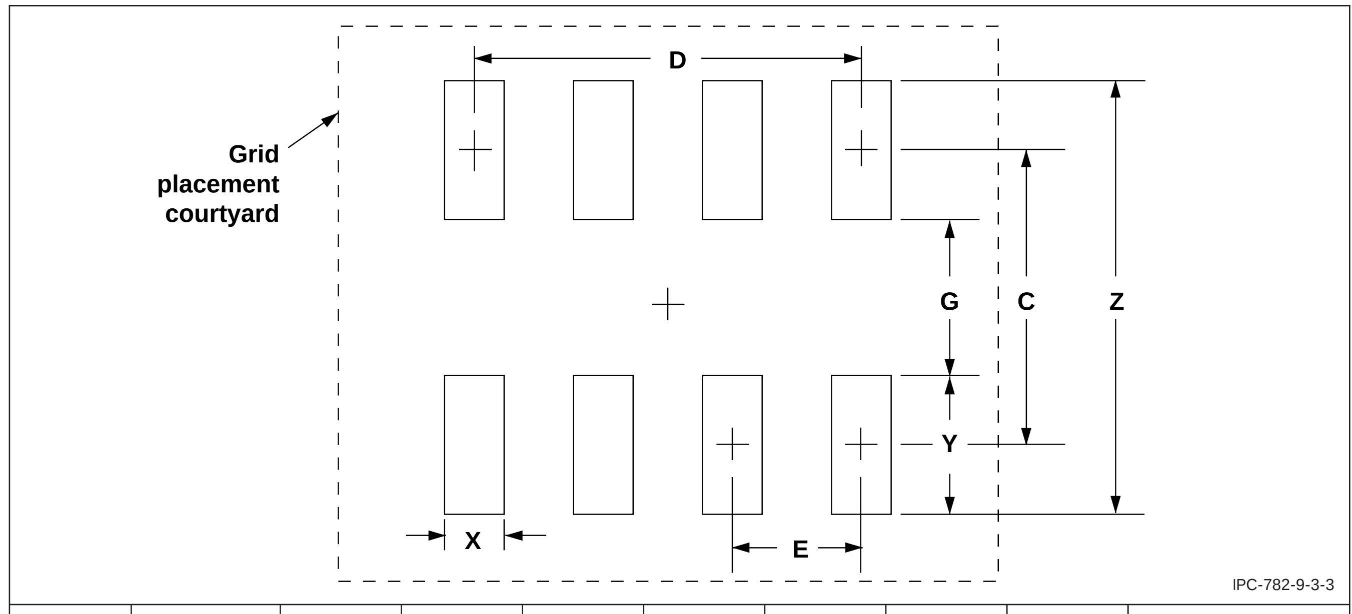
Figure 2 SOPIC component dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for SOPIC components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



RLP No.	Component Identifier	Z (mm)	G (mm)	X (mm)	Y (mm) ref	C (mm) ref	D (mm) ref	E (mm) basic	Placement Grid (No. Grid Elements)
360A	SOP 6	7.40	3.00	0.60	2.20	5.20	2.54	1.27	16x14
361A	SOP 8	7.40	3.00	0.60	2.20	5.20	3.81	1.27	16x14
362A	SOP 10	7.40	3.00	0.60	2.20	5.20	5.08	1.27	16x18
363A	SOP 12	7.40	3.00	0.60	2.20	5.20	6.35	1.27	16x18
364A	SOP 14	7.40	3.00	0.60	2.20	5.20	7.62	1.27	16x24
365A	SOP 16	9.40	5.00	0.60	2.20	7.20	8.89	1.27	20x24
366A	SOP 18	9.40	5.00	0.60	2.20	7.20	10.16	1.27	20x28
367A	SOP 20	9.40	5.00	0.60	2.20	7.20	11.43	1.27	20x28
368A	SOP 22	11.20	6.80	0.60	2.20	9.00	13.97	1.27	24x34
369A	SOP 24	11.20	6.80	0.60	2.20	9.00	13.97	1.27	24x34
370A	SOP 28	13.20	8.80	0.60	2.20	11.00	16.51	1.27	28x40
371A	SOP 30	13.20	8.80	0.60	2.20	11.00	17.78	1.27	28x44
372A	SOP 32	15.00	10.60	0.60	2.20	12.80	19.05	1.27	32x44
373A	SOP 36	15.00	10.60	0.60	2.20	12.80	21.59	1.27	32x50
374A	SOP 40	17.00	12.60	0.60	2.20	14.80	24.13	1.27	36x56
375A	SOP 42	17.00	12.60	0.60	2.20	14.80	25.40	1.27	36x56

Figure 3 SOPIC land pattern dimensions

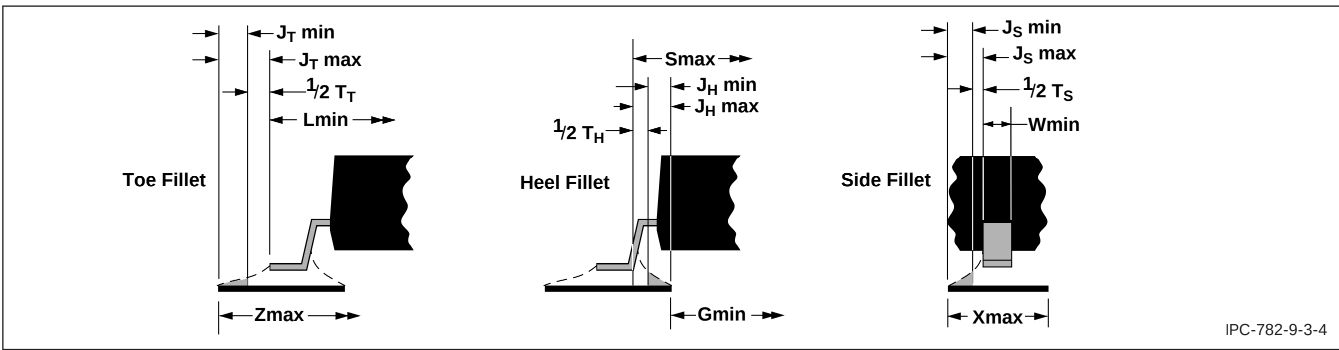
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



RLP No.	Tolerance Assumptions (mm)		Solder Joint								
			Toe (mm)			Heel (mm)			Side (mm)		
	F	P	C_L	$J_T$min	$J_T$max	C_S	$J_H$min	$J_H$max	C_W	$J_S$min	$J_S$max
360A	0.10	0.10	1.27	0.20	0.84	1.26	0.36	1.06	0.16	0.02	0.13
361A	0.10	0.10	1.27	0.20	0.84	1.26	0.36	1.06	0.16	0.02	0.13
362A	0.10	0.10	1.27	0.20	0.84	1.26	0.36	1.06	0.16	0.02	0.13
363A	0.10	0.10	1.27	0.20	0.84	1.26	0.36	1.06	0.16	0.02	0.13
364A	0.10	0.10	1.27	0.20	0.84	1.26	0.36	1.06	0.16	0.02	0.13
365A	0.10	0.10	1.27	0.25	0.89	1.26	0.31	1.01	0.16	0.02	0.13
366A	0.10	0.10	1.27	0.25	0.89	1.26	0.31	1.01	0.16	0.02	0.13
367A	0.10	0.10	1.27	0.25	0.89	1.26	0.31	1.01	0.16	0.02	0.13
368A	0.10	0.10	1.27	0.20	0.84	1.26	0.36	1.06	0.16	0.02	0.13
369A	0.10	0.10	1.27	0.20	0.84	1.26	0.36	1.06	0.16	0.02	0.13
370A	0.10	0.10	1.27	0.25	0.89	1.26	0.31	1.01	0.16	0.02	0.13
371A	0.10	0.10	1.27	0.25	0.89	1.26	0.31	1.01	0.16	0.02	0.13
372A	0.10	0.10	1.27	0.19	0.83	1.26	0.37	1.07	0.16	0.02	0.13
373A	0.10	0.10	1.27	0.19	0.83	1.26	0.37	1.07	0.16	0.02	0.13
374A	0.10	0.10	1.27	0.24	0.88	1.26	0.32	1.02	0.16	0.02	0.13
375A	0.10	0.10	1.27	0.24	0.88	1.26	0.32	1.02	0.16	0.02	0.13

Figure 4 Tolerance and solder joint analysis

1.0 SCOPE

This subsection provides the component and land pattern dimensions for thin small outline packages (TSOP components) with gullwing leads on two sides. Basic construction of the TSOP device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

2.0 APPLICABLE DOCUMENTS

See Section 9.0 and the following for documents applicable to this subsection.

2.1 Electronic Industries Association of Japan (EIAJ)

EIAJ-ED-7402-3 General Rules for the Preparation of Outline Drawings of Integrated Circuits Thin Small Outline Packages

3.0 COMPONENT DESCRIPTIONS

3.1 Basic Construction The TSOP package is unique among the component families of this section becaue its leads protrude from the short side of the plastic body. The TSOP components are available in four different pitches: 0.3, 0.4, 0.5, and 0.65 mm. They are typically specified by their two largest dimensions—the plastic body size (in the short dimension), and the nominal toe-to-toe length (in the long dimension). Their use has grown because their height (less than 1.27 mm) allows them to be used in memory card technology.

EIAJ ED-7402-3 outlines sixteen different body sizes with pin counts ranging from 16–76 pins. In general, as the long dimension increases, the pitch decreases. See Figure 1.

3.1.1 Termination Materials Leads must be solder-coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the leads by hot dipping or by plating from solution. Plated solder terminations should be subjected to post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

3.1.2 Marking Parts are available with or without part number markings. Usually an index mark indicates pin 1.

3.1.3 Carrier Packages Format Trays are usually used for handling TSOP's.

3.1.4 Resistance to Soldering Parts should be capable of withstanding ten cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260°C.

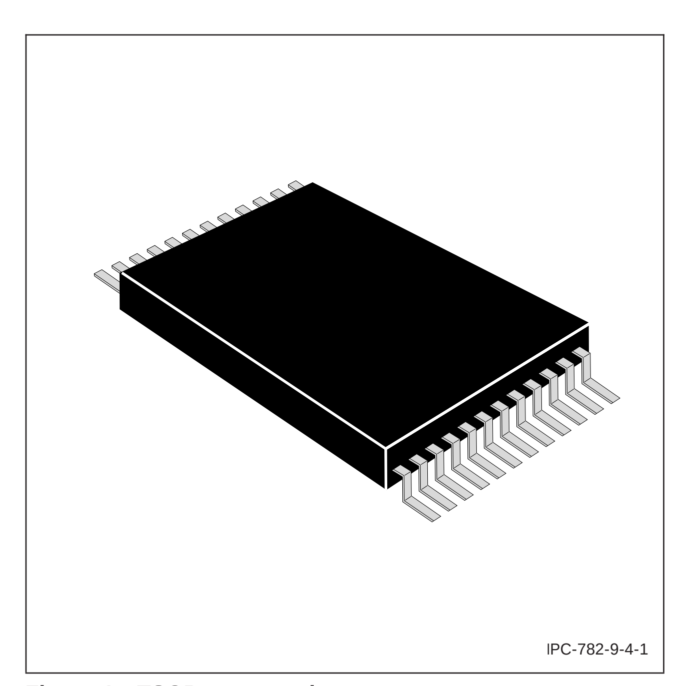
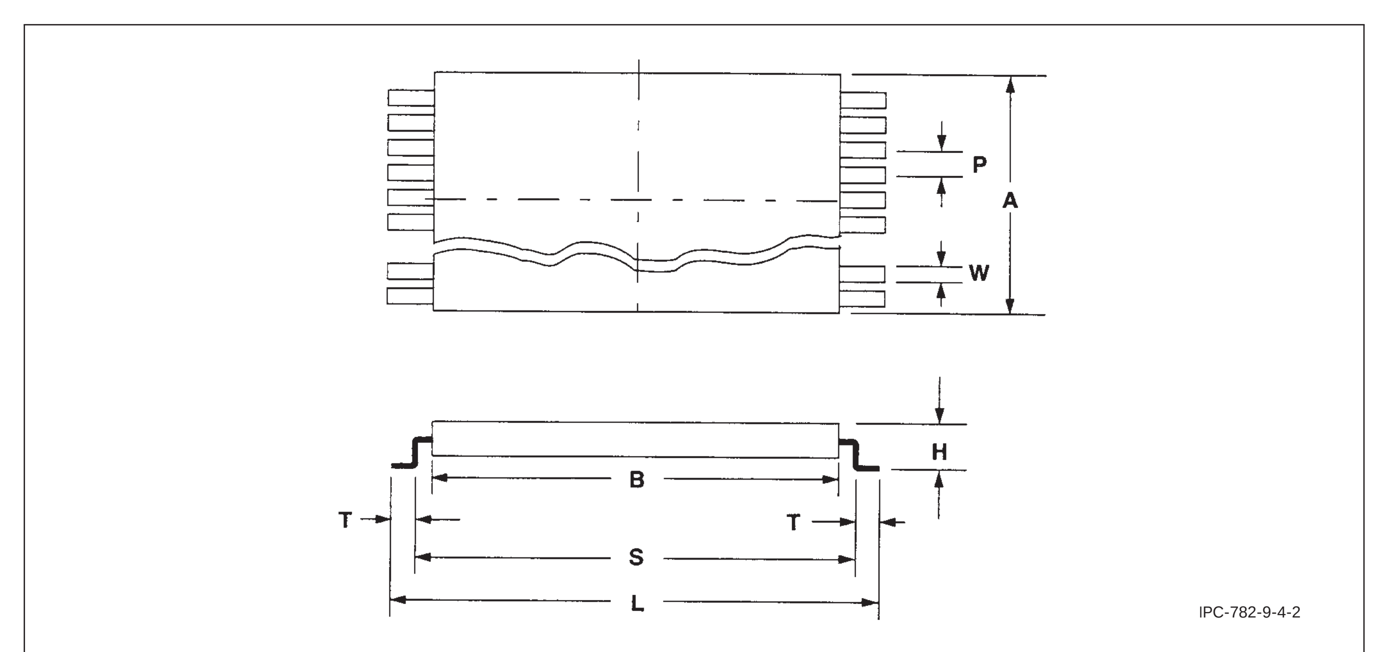


Figure 1 TSOP construction

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for TSOP components.



Component Identifier (mm)	Pin Count	L (mm)		S (mm)		W (mm)		T (mm)		A (mm)		B (mm)		H (mm)	P (mm)
		min	max	min	max	min	max	m in	max	min	max	min	max	max	basic
TSOP 6x14	16	13.80	14.20	12.40	12.98	0.20	0.40	0.40	0.70	5.80	6.20	12.20	12.60	1.27	0.65
TSOP 6x16	24	15.80	16.20	14.40	14.98	0.10	0.30	0.40	0.70	5.80	6.20	14.20	14.60	1.27	0.50
TSOP 6x18	28	17.80	18.20	16.40	16.78	0.05	0.22	0.40	0.70	5.80	6.20	16.20	16.60	1.27	0.40
TSOP 6x20	36	19.80	20.20	18.40	18.98	0.05	0.15	0.40	0.70	5.80	6.20	18.20	18.60	1.27	0.30
TSOP 8x14	24	13.80	14.20	12.40	12.98	0.20	0.40	0.40	0.70	7.80	8.20	12.20	12.60	1.27	0.65
TSOP 8x16	32	15.80	16.20	14.40	14.98	0.10	0.30	0.40	0.70	7.80	8.20	14.20	14.60	1.27	0.50
TSOP 8x18	40	17.80	18.20	16.40	16.98	0.05	0.22	0.40	0.70	7.80	8.20	16.20	16.60	1.27	0.40
TSOP 8x20	52	19.80	20.20	18.40	18.98	0.05	0.15	0.40	0.70	7.80	8.20	18.20	18.60	1.27	0.30
TSOP 10x14	28	13.80	14.20	12.40	12.98	0.20	0.40	0.40	0.70	9.80	10.20	12.20	12.60	1.27	0.65
TSOP 10x16	40	15.80	16.20	14.40	14.98	0.10	0.30	0.40	0.70	9.80	10.20	14.20	14.60	1.27	0.50
TSOP 10x18	48	17.80	18.20	16.40	16.98	0.05	0.22	0.40	0.70	9.80	10.20	16.20	16.60	1.27	0.40
TSOP 10x20	64	19.80	20.20	18.40	18.98	0.05	0.15	0.40	0.70	9.80	10.20	18.20	18.60	1.27	0.30
TSOP 12x14	36	13.80	14.20	12.40	12.98	0.20	0.40	0.40	0.70	11.80	12.20	12.20	12.60	1.27	0.65
TSOP 12x16	48	15.80	16.20	14.40	14.98	0.10	0.30	0.40	0.70	11.80	12.20	14.20	14.60	1.27	0.50
TSOP 12x18	60	17.80	18.20	16.40	16.98	0.05	0.22	0.40	0.70	11.80	12.20	16.20	16.60	1.27	0.40
TSOP 12x20	76	19.80	20.20	18.40	18.98	0.05	0.15	0.40	0.70	11.80	12.20	18.20	18.60	1.27	0.30

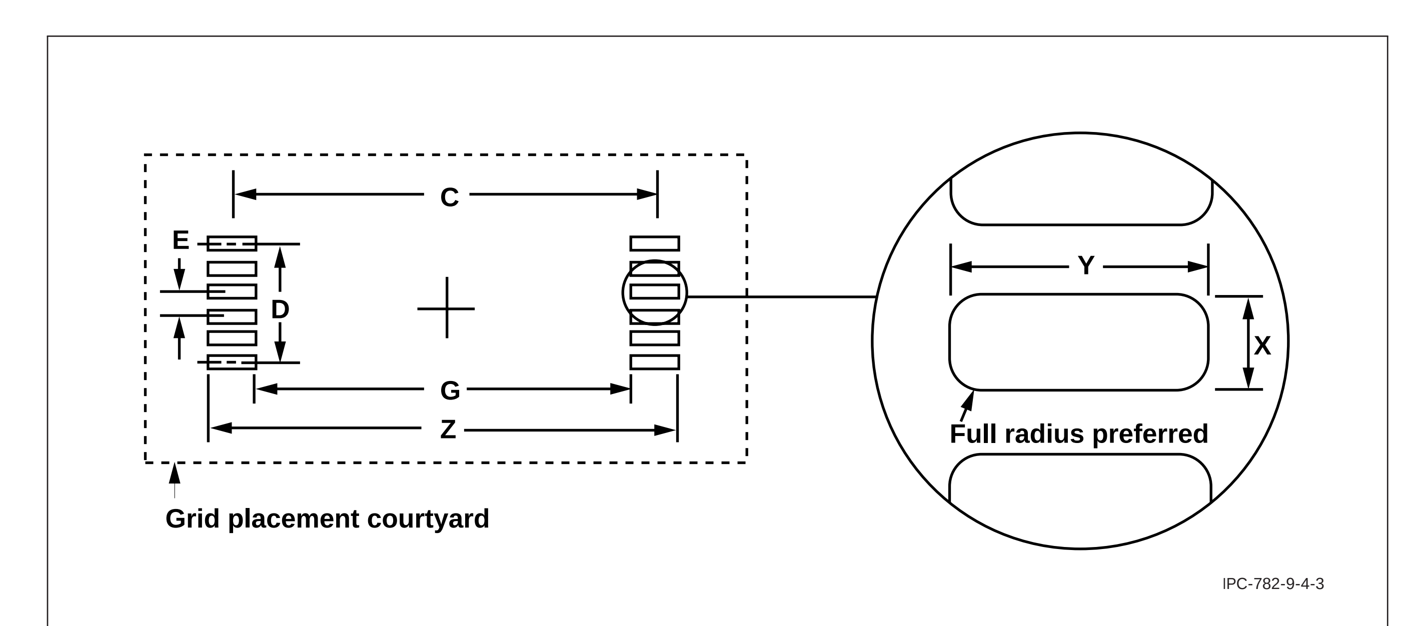
Figure 2 TSOP component dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for TSOP components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



RLP No.	Component Identifier (mm)	Z (mm)	G (mm)	X (mm)	Y (mm) ref	C (mm) ref	D (mm) ref	E (mm) basic	Pin Count	Placement Grid (No. of Grid Elements)
390A	6x14	14.80	11.60	0.40	1.60	13.20	4.55	0.65	16	14x32
391A	6x16	16.80	13.60	0.30	1.60	15.20	5.50	0.50	24	14x36
392A	6x18	18.80	15.60	0.25	1.60	17.20	5.20	0.40	28	14x40
393A	6x20	20.80	17.60	0.17	1.60	19.20	5.10	0.30	36	14x44
394A	8x14	14.80	11.60	0.40	1.60	13.20	7.15	0.65	24	18x32
395A	8x16	16.80	13.60	0.30	1.60	15.20	7.50	0.50	32	18x36
396A	8x18	18.80	15.60	0.25	1.60	17.20	7.60	0.40	40	18x40
397A	8x20	20.80	17.60	0.17	1.60	19.20	7.50	0.30	52	18x44
398A	10x14	14.80	11.60	0.40	1.60	13.20	8.45	0.65	28	22x32
399A	10x16	16.80	13.60	0.30	1.60	15.20	9.50	0.50	40	22x36
400A	10x18	18.80	15.60	0.25	1.60	17.20	9.20	0.40	48	22x40
401A	10x20	20.80	17.60	0.17	1.60	19.20	9.30	0.30	64	22x44
402A	12x14	14.80	11.60	0.40	1.60	13.20	11.05	0.65	36	26x32
403A	12x16	16.80	13.60	0.30	1.60	15.20	11.50	0.50	48	26x36
404A	12x18	18.80	15.60	0.25	1.60	17.20	11.60	0.40	60	26x40
405A	12x20	20.80	17.60	0.17	1.60	19.20	11.10	0.30	76	26x44

Figure 3 TSOP land pattern dimensions

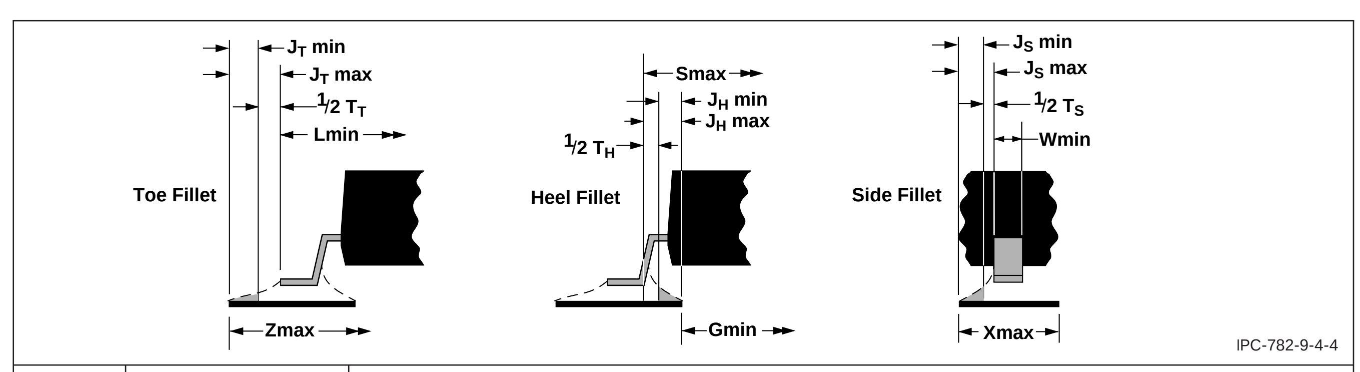
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



RLP No.	Tolerance Assumptions (mm)		Solder Joint								
			Toe (mm)			Heel (mm)			Side (mm)		
	F	P	C_L	$J_T$min	$J_T$max	C_S	$J_H$min	$J_H$max	C_W	$J_S$min	$J_S$max
390A	0.10	0.10	0.40	0.29	0.50	0.58	0.39	0.69	0.20	-0.02	0.10
391A	0.10	0.10	0.40	0.29	0.50	0.58	0.39	0.69	0.20	-0.02	0.10
392A	0.10	0.10	0.40	0.29	0.50	0.58	0.39	0.69	0.10	-0.01	0.10
393A	0.10	0.10	0.40	0.29	0.50	0.58	0.39	0.69	0.06	-0.03	0.06
394A	0.10	0.10	0.40	0.29	0.50	0.58	0.39	0.69	0.20	-0.02	0.10
395A	0.10	0.10	0.40	0.29	0.50	0.58	0.39	0.69	0.20	-0.02	0.10
396A	0.10	0.10	0.40	0.29	0.50	0.58	0.39	0.69	0.17	-0.01	0.10
397A	0.10	0.10	0.40	0.29	0.50	0.58	0.39	0.69	0.10	-0.03	0.06
398A	0.10	0.10	0.40	0.29	0.50	0.58	0.39	0.69	0.20	-0.02	0.10
399A	0.10	0.10	0.40	0.29	0.50	0.58	0.39	0.69	0.20	-0.02	0.10
400A	0.10	0.10	0.40	0.29	0.50	0.58	0.39	0.69	0.17	-0.01	0.10
401A	0.10	0.10	0.40	0.29	0.50	0.58	0.39	0.69	0.10	-0.03	0.06
402A	0.10	0.10	0.40	0.29	0.50	0.58	0.39	0.69	0.20	-0.02	0.10
403A	0.10	0.10	0.40	0.29	0.50	0.58	0.39	0.69	0.20	-0.02	0.10
404A	0.10	0.10	0.40	0.29	0.50	0.58	0.39	0.69	0.17	-0.01	0.10
405A	0.10	0.10	0.40	0.29	0.50	0.58	0.39	0.69	0.10	-0.03	0.06

Figure 4 Tolerance and solder joint analysis



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Surface Mount Design and Land Pattern Standard

Date	Section
8/93	9.5
Revision	Subject
	CFP

1.0 SCOPE

This subsection provides the component and land pattern dimensions for ceramic flat packs (CFP components) with gullwing leads on two sides. Basic construction of the CFP device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

2.0 APPLICABLE DOCUMENTS

See Section 9.0 and the following for documents applicable to this subsection.

JEDEC Publication 95 Registered and Standard Outlines for Solid State and Related Products:

Outline	*Issues*	*Title*
MO-003	C	Flatpack Family, 5.08 Width, 1.27 Pitch
MO-004	C	Flatpack Family, 7.62 Width, 1.27 Pitch
MO-018	—	Flatpack Family, 10.16 Width, 1.27 Pitch
MO-019	D	Flatpack Family, 10.16 Width, 1.27 Pitch
MO-020	C	Flatpack Family, 12.70 Width, 1.27 Pitch
MO-021	C	Flatpack Family, 15.24 Width, 1.27 Pitch
MO-022	D	Flatpack Family, 17.78 Width, 1.27 Pitch
MO-023	C	Flatpack Family, 22.86 Width, 1.27 Pitch

Application for copies should be addressed to:
Global Engineering Documents
1990 M Street N.W.
Washington, DC

3.0 COMPONENT DESCRIPTIONS

3.1 Basic Construction See Figure 1. Basic construction consists of a ceramic body and metallic leads. Leads are trimmed and formed into gullwing shape as shown in Figure 2.

3.1.1 Termination Materials Leads should be solder-coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the termination by hot dipping or by plating from solution. Plated solder terminations should be subjected to a post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.00075 mm [0.0003 in] thick.

3.1.2 Marking All parts shall be marked with a part number and an index area. The index area shall identify the location of pin 1.

3.1.3 Carrier trays are used for handling CFPs.

3.1.4 Resistance to Soldering Parts should be capable of withstanding ten cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260°C.

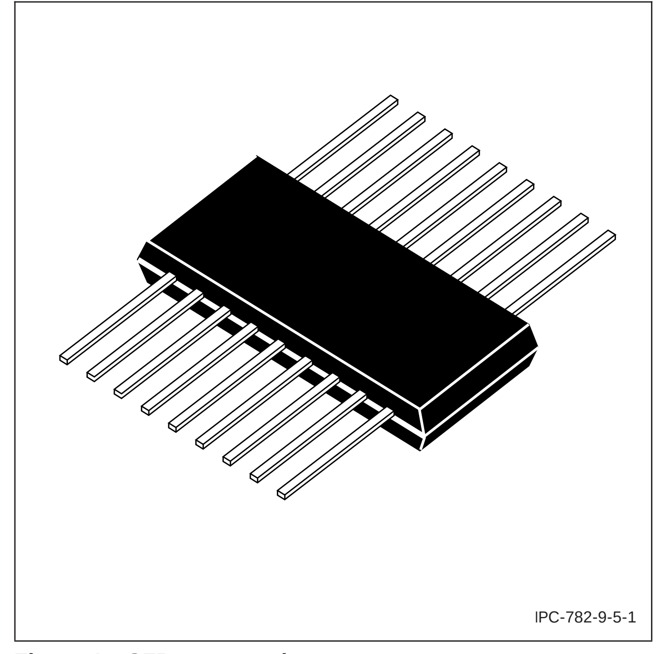
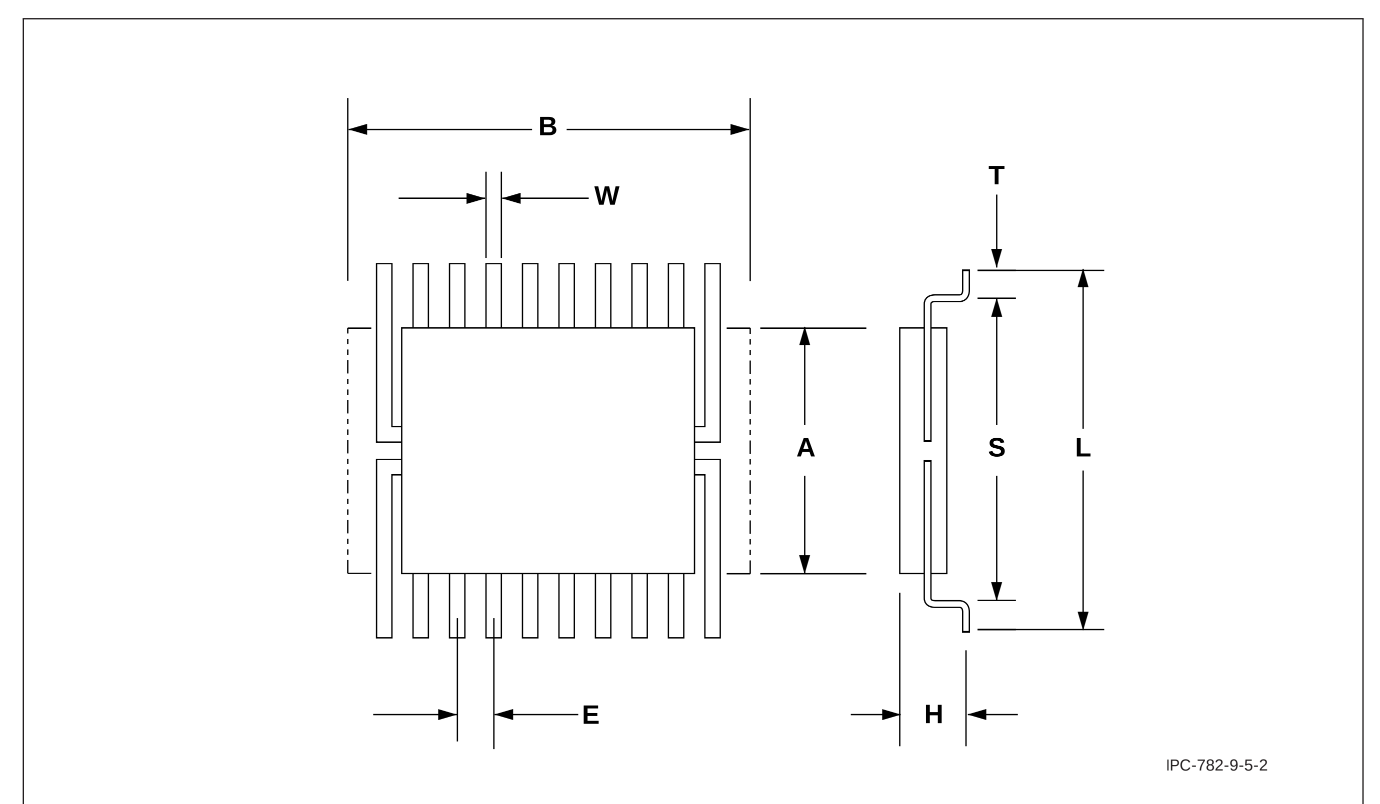


Figure 1 CFP construction

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for CFP components.



CFP Component Identifier	Pin Count	L (mm)		S (mm)		W (mm)		T (mm)		A (mm)		B (mm)	H (mm)	E
		min	max	min	max	min	max	min	max	min	max	max	max	basic
MO-003	10	9.00	9.60	6.46	7.26	0.25	0.35	0.90	1.27	2.54	5.08	7.36	2.50	1.27
MO-003	14	9.00	9.60	6.46	7.26	0.25	0.35	0.90	1.27	2.54	5.08	9.90	2.50	1.27
MO-004	10	11.00	11.60	8.46	9.26	0.38	0.48	0.90	1.27	5.08	7.62	7.36	2.50	1.27
MO-004	14	11.00	11.60	8.46	9.26	0.38	0.48	0.90	1.27	5.08	7.62	9.90	2.50	1.27
MO-004	16	11.00	11.60	8.46	9.26	0.38	0.48	0.90	1.27	5.08	7.62	11.17	2.50	1.27
MO-018	20	11.00	11.60	8.46	9.26	0.25	0.35	0.90	1.27	7.62	10.16	13.71	2.50	1.27
MO-019	24	15.00	15.60	12.46	13.26	0.38	0.48	0.90	1.27	7.62	10.16	16.25	2.50	1.27
MO-019	28	15.00	15.60	12.46	13.26	0.46	0.56	0.90	1.27	7.62	10.16	18.79	2.50	1.27
MO-020	36	17.00	17.60	14.46	15.26	0.38	0.48	0.90	1.27	10.16	12.70	23.87	3.00	1.27
MO-020	40	17.00	17.60	14.46	15.26	0.33	0.43	0.90	1.27	10.16	12.70	26.41	3.00	1.27
MO-021	16	20.00	20.60	17.46	18.26	0.38	0.48	0.90	1.27	12.70	15.24	11.17	2.50	1.27
MO-021	24	20.00	20.60	17.46	18.26	0.38	0.48	0.90	1.27	12.70	15.24	16.25	2.50	1.27
MO-021	36	20.00	20.60	17.46	18.26	0.38	0.48	0.90	1.27	12.70	15.24	23.87	3.00	1.27
MO-022	20	22.00	22.60	19.46	20.26	0.38	0.48	0.90	1.27	15.24	17.78	13.71	2.50	1.27
MO-022	42	22.00	22.60	19.46	20.26	0.46	0.56	0.90	1.27	15.24	17.78	27.68	3.00	1.27
MO-023	36	27.00	27.60	24.46	25.26	0.38	0.48	0.90	1.27	20.32	22.86	23.87	3.00	1.27
MO-023	50	27.00	27.60	24.46	25.26	0.38	0.48	0.90	1.27	20.32	22.86	32.76	3.00	1.27

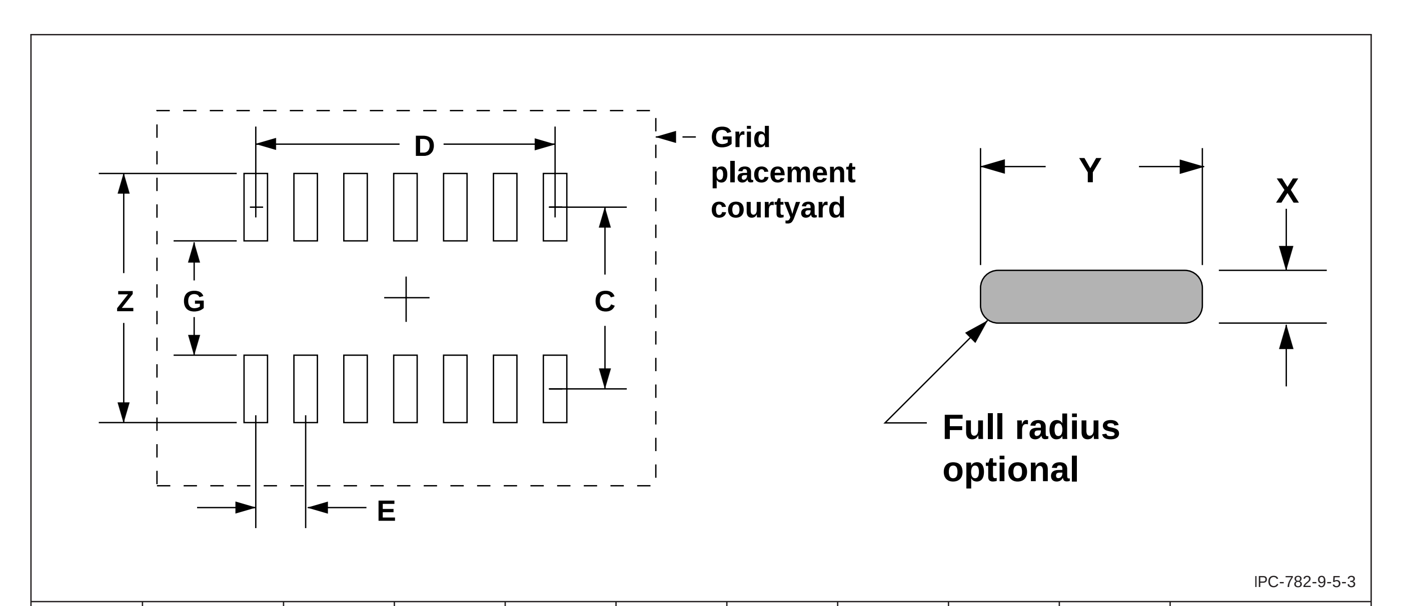
Figure 2 CFP component dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for CFP components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



RLP No.	Component Identifier	Pin Count	Z (mm)	G (mm)	X (mm)	Y (mm) ref	C (mm) ref	D (mm) ref	E (mm) basic	Placement Grid (No. Grid Elements)
420	MO-003	10	10.20	6.00	0.65	2.20	8.0	5.08	1.27	22x16
421	MO-003	14	10.20	6.00	0.65	2.20	8.0	7.62	1.27	22x22
422	MO-004	10	12.20	8.00	0.65	2.20	10.0	5.08	1.27	26x16
423	MO-004	14	12.20	8.00	0.65	2.20	10.0	7.62	1.27	26x22
424	MO-004	16	12.20	8.00	0.65	2.20	10.0	8.89	1.27	26x24
425	MO-018	20	12.20	8.00	0.65	2.20	10.0	11.43	1.27	26x28
426	MO-019	24	16.20	12.00	0.65	2.20	14.0	13.97	1.27	34x34
427	MO-019	28	16.20	12.00	0.65	2.20	14.0	16.51	1.27	34x38
428	MO-020	36	18.20	14.00	0.65	2.20	16.0	21.59	1.27	38x48
429	MO-020	40	18.20	14.00	0.65	2.20	16.0	24.13	1.27	38x54
430	MO-021	16	21.20	17.00	0.65	2.20	19.0	8.89	1.27	44x24
431	MO-021	24	21.20	17.00	0.65	2.20	19.0	13.97	1.27	44x34
432	MO-021	36	21.20	17.00	0.65	2.20	19.0	21.59	1.27	44x48
433	MO-022	20	23.20	19.00	0.65	2.20	21.0	11.43	1.27	48x28
434	MO-022	42	23.20	19.00	0.65	2.20	21.0	25.40	1.27	48x56
435	MO-023	36	28.20	24.00	0.65	2.20	26.0	21.59	1.27	58x48
436	MO-023	50	28.20	24.00	0.65	2.20	26.0	30.48	1.27	58x66

Figure 3 CFP land pattern dimensions

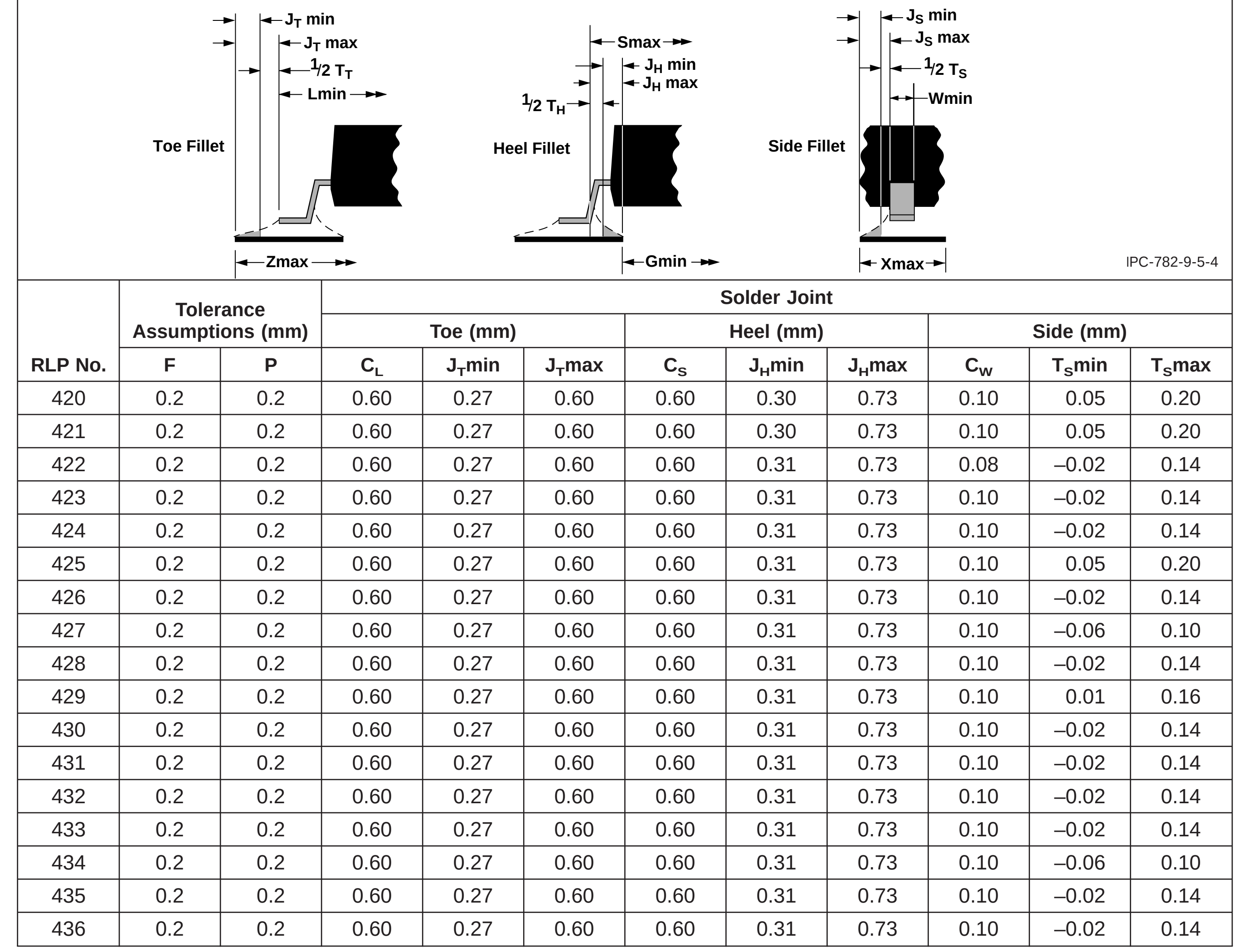
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



RLP No.	Tolerance Assumptions (mm)		Solder Joint								
			Toe (mm)			Heel (mm)			Side (mm)		
	F	P	C_L	$J_T$min	$J_T$max	C_S	$J_H$min	$J_H$max	C_W	$T_S$min	$T_S$max
420	0.2	0.2	0.60	0.27	0.60	0.60	0.30	0.73	0.10	0.05	0.20
421	0.2	0.2	0.60	0.27	0.60	0.60	0.30	0.73	0.10	0.05	0.20
422	0.2	0.2	0.60	0.27	0.60	0.60	0.31	0.73	0.08	–0.02	0.14
423	0.2	0.2	0.60	0.27	0.60	0.60	0.31	0.73	0.10	–0.02	0.14
424	0.2	0.2	0.60	0.27	0.60	0.60	0.31	0.73	0.10	–0.02	0.14
425	0.2	0.2	0.60	0.27	0.60	0.60	0.31	0.73	0.10	0.05	0.20
426	0.2	0.2	0.60	0.27	0.60	0.60	0.31	0.73	0.10	–0.02	0.14
427	0.2	0.2	0.60	0.27	0.60	0.60	0.31	0.73	0.10	–0.06	0.10
428	0.2	0.2	0.60	0.27	0.60	0.60	0.31	0.73	0.10	–0.02	0.14
429	0.2	0.2	0.60	0.27	0.60	0.60	0.31	0.73	0.10	0.01	0.16
430	0.2	0.2	0.60	0.27	0.60	0.60	0.31	0.73	0.10	–0.02	0.14
431	0.2	0.2	0.60	0.27	0.60	0.60	0.31	0.73	0.10	–0.02	0.14
432	0.2	0.2	0.60	0.27	0.60	0.60	0.31	0.73	0.10	–0.02	0.14
433	0.2	0.2	0.60	0.27	0.60	0.60	0.31	0.73	0.10	–0.02	0.14
434	0.2	0.2	0.60	0.27	0.60	0.60	0.31	0.73	0.10	–0.06	0.10
435	0.2	0.2	0.60	0.27	0.60	0.60	0.31	0.73	0.10	–0.02	0.14
436	0.2	0.2	0.60	0.27	0.60	0.60	0.31	0.73	0.10	–0.02	0.14

Figure 4 Tolerance and solder joint analysis



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Surface Mount Design and Land Pattern Standard

Date	Section
8/93	10.0
Revision	Subject
	Components with J Leads on Two Sides

1.0 INTRODUCTION This section covers land patterns for components with J leads on two sides. Each subsection contains information in accordance with the following format:

1.0 Scope
2.0 Applicable Documents
3.0 General Component Description (Figure 1)
4.0 Component Dimensions (Figure 2)
5.0 Land Pattern Dimensions (Figure 3)
6.0 Tolerance and Solder Joint Analysis (Figure 4)

The following is the table of contents for this section:

Table of Contents

2.0 APPLICABLE DOCUMENTS

The following documents, of the issue in effect on the revision date of this section, form a part of this specification to the extent specified herein.

2.1 Electronic Industries Association (EIA)[1]

JEDEC Publication 95 Registered and Standard Outlines for Solid State and Related Products:
MO-077, issue ''C,'' dated 8/91
MO-065, issue ''A,'' dated 5/87
MO-063, issue ''A,'' dated 4/2/87
MO-061, issue ''C,'' date 8/91

EIA-PDP-100 Registered and Standard Mechanical Outlines for Electronic Parts

EIA-481-A Taping of Surface Mount Components for Automatic Placement

EIA-481-3 32 mm, 44 mm, and 56 mm Embossed Carrier Taping of Surface Mount Components for Automated Handling

2.2 Electronic Industries Association of Japan (EIAJ)

EIAJ-ED-7406 General Rules for the Preparation of Outline Drawings of Integrated Circuits

2.3 International Electrotechnical Commission (IEC)[2]

IEC 97 Grid Elements

3.0 General Information

3.1 General Component Description This section provides the component and land pattern dimensions for small outline integrated circuits with ''J'' leads (SOJ components). Basic construction of the SOJ device is also covered. At the end of the subsections are listings of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

3.2 Packaging Components may be provided in tube or tape packaging. Tape is preferred for best handling and high volume applications. Bulk packaging is not acceptable because of lead coplanarity requirements required for placement and soldering. EIA-481 provides details on tape requirements.

1. Application for copies should be addressed to Global Engineering Documents, 1990 M St. N.W., Washington, DC 20036.
2. Application for copies should be addressed to IEC, 3 rue de Varembe, PO Box 131 - 1211 Geneva 20, Switzerland

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1.0 SCOPE

This subsection provides the component and land pattern dimensions for small outline integrated circuits with ''J'' leads (SOJ components). Basic construction of the SOJ device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

2.0 APPLICABLE DOCUMENTS

See Section 10.0 for documents applicable to the subsections.

3.0 COMPONENT DESCRIPTIONS

The two-sided J lead family is a small outline family identified by the dimension of the body size in inches. For example, the SOJ/300 has a body size of 0.300 inches or 7.63 mm, the SOJ/350 has a body size of 0.350 inches or 8.88 mm, the SOJ/400 has a body size of 0.400 inches or 10.12 mm, and the SOJ/450 has a body size of 0.450 inches or 11.38 mm. Package lead counts range from 14 to 28 pins.

The small-outline ''J'' (SOJ) package has leads on two sides, similar to a DIP. The lead configuration, like the letter J, extends out the side of the package and bends under the package forming a J bend. The point of contact of the lead to the land

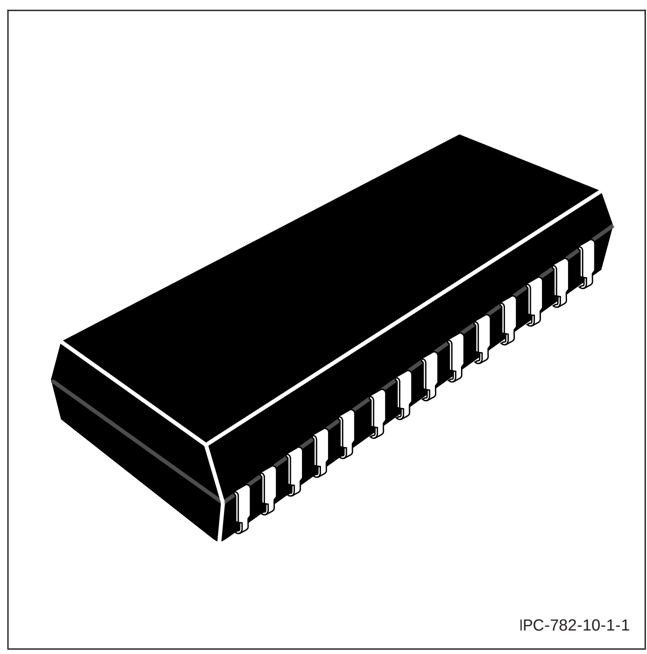


Figure 1 SOJ construction

pattern is at the apex of the J bend and is the basis for the span of the land pattern.

The leads must be coplanar within 0.1 mm. That is, when the component is placed on a flat surface, no lead may be more than 0.1 mm off the flat surface.

The SOJ package takes advantage of chips having parallel address or data line layouts. For example, memory IC's are often used in multiples, and buss lines connect to the same pin on each chip. Memory chips in SOJ packages can be placed close to one another because of the parallel pin layout and the use of ''J'' leads. With high capacity memory systems, the space savings can be significant.

3.1 Basic Construction See Figure 1. Basic construction consists of a plastic body, and metallic ''J'' leads.

3.1.1 Termination Materials Leads must be solder-coated with a tin/lead alloy. The solder should contain between 58 to 68% lead. Solder may be applied to theleads by hot dipping or by plating from solution. Plated solder terminations should be subjected to post-plating reflow operation to fuse the solder. The tin/lead finishshould be at least 0l.0075 mm [0.0003 in] thick.

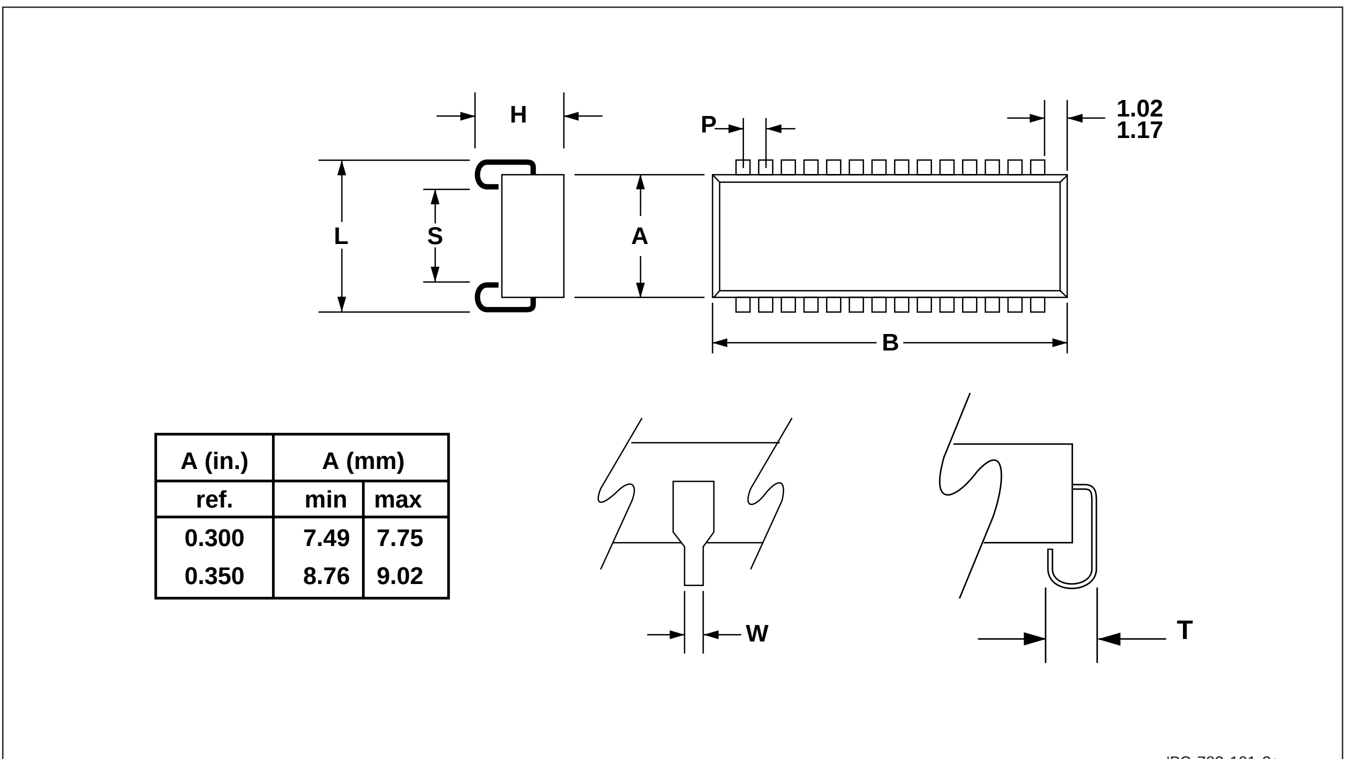
3.1.2 Marking The SOIC family of parts is generally marked with manufacturers part numbers, manufacturers name or symbol, and a pin 1 indicator. Some parts may have a pin 1 feature in the case shape instead of pin 1 marking. Additional markings may include date code/manufacturing lot and/or manufacturing location.

3.1.3 Carrier Package Format Components may be provided in tube or tape packaging. Tape is preferred for best handling and high volume applications. Bulk packaging is not acceptable because of lead coplanarity requirements required for placement and soldering. EIA-481 provides details on tape requirements.

3.1.4 Process Considerations J lead packages are normally processed using standard solder reflow processes. Parts should be capable of withstanding ten cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C.

4.0 COMPONENT DIMENSIONS

In this subsection, Figures 2a–2b provide the component dimensions for SOJ components. (Also see page 4.)



A (in.)	A (mm)	
ref.	min	max
0.300	7.49	7.75
0.350	8.76	9.02

Component Identifier (Pin Count)	L (mm)		S (mm)		W (mm)		T (mm)		B (mm)		H (mm)	P (mm)
	min	max	min	max	min	max	min	max	m in	max	max	basic
SOJ 14/300	8.38	8.76	4.38	5.06	0.38	0.51	1.60	2.00	9.65	9.96	3.75	1.27
SOJ 16/300	8.38	8.76	4.38	5.06	0.38	0.51	1.60	2.00	10.92	11.23	3.75	1.27
SOJ 18/300	8.38	8.76	4.38	5.06	0.38	0.51	1.60	2.00	12.19	12 .50	3.75	1.27
SOJ 20/300	8.38	8.76	4.38	5.06	0.38	0.51	1.60	2.00	13.46	13.77	3.75	1.27
SOJ 22/300	8.38	8.76	4.38	5.06	0.38	0.51	1.60	2.00	14.73	15.04	3.75	1.27
SOJ 24/300	8.38	8.76	4.38	5.06	0.38	0.51	1.60	2.00	16.00	16.31	3.75	1.27
SOJ 26/300	8.38	8.76	4.38	5.06	0.38	0.51	1.60	2.00	17.27	17.58	3.75	1.27
SOJ 28/300	8.38	8.76	4.38	5.06	0.38	0.51	1.60	2.00	18.54	18.85	3.75	1.27
SOJ 14/350	9.65	10.03	5.65	6.33	0.38	0.51	1.60	2.00	9.65	9.96	3.75	1.27
SOJ 16/350	9.65	10.03	5.65	6.33	0.38	0.51	1.60	2.00	10.92	11.23	3.75	1.27
SOJ 18/350	9.65	10.03	5.65	6.33	0.38	0.51	1.60	2.00	12.19	12.50	3.75	1.27
SOJ 20/350	9.65	10.03	5.65	6.33	0.38	0.51	1.60	2.00	13.46	13.77	3.75	1.27
SOJ 22/350	9.65	10.03	5.65	6.33	0.38	0.51	1.60	2.00	14.73	15.04	3.75	1.27
SOJ 24/350	9.65	10.03	5.65	6.33	0.38	0.51	1.60	2.00	16.00	16.31	3.75	1.27
SOJ 26/350	9.65	10.03	5.65	6.33	0.38	0.51	1.60	2.00	17.27	17.58	3.75	1.27
SOJ 28/350	9.65	10.03	5.65	6.33	0.38	0.51	1.60	2.00	18.54	18.85	3.75	1.27

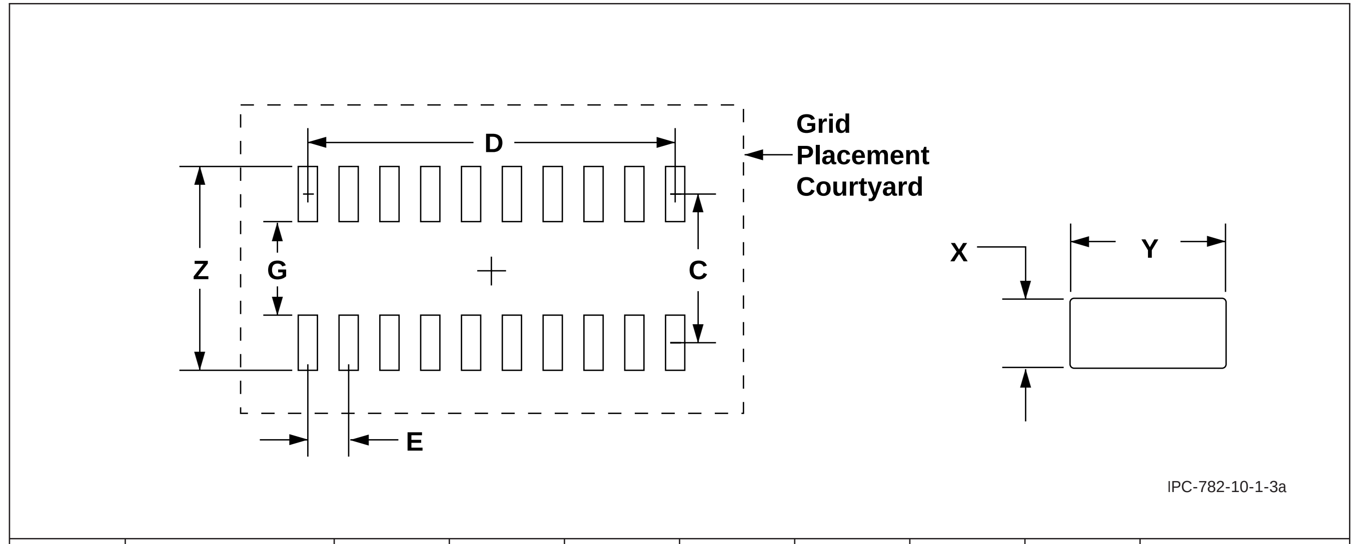
Figure 2a SOJ component dimensions

5.0 LAND PATTERN DIMENSIONS

In this subsection, Figures 3a–3b provide the land pattern dimensions for SOJ components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns. (Also see page 5.)

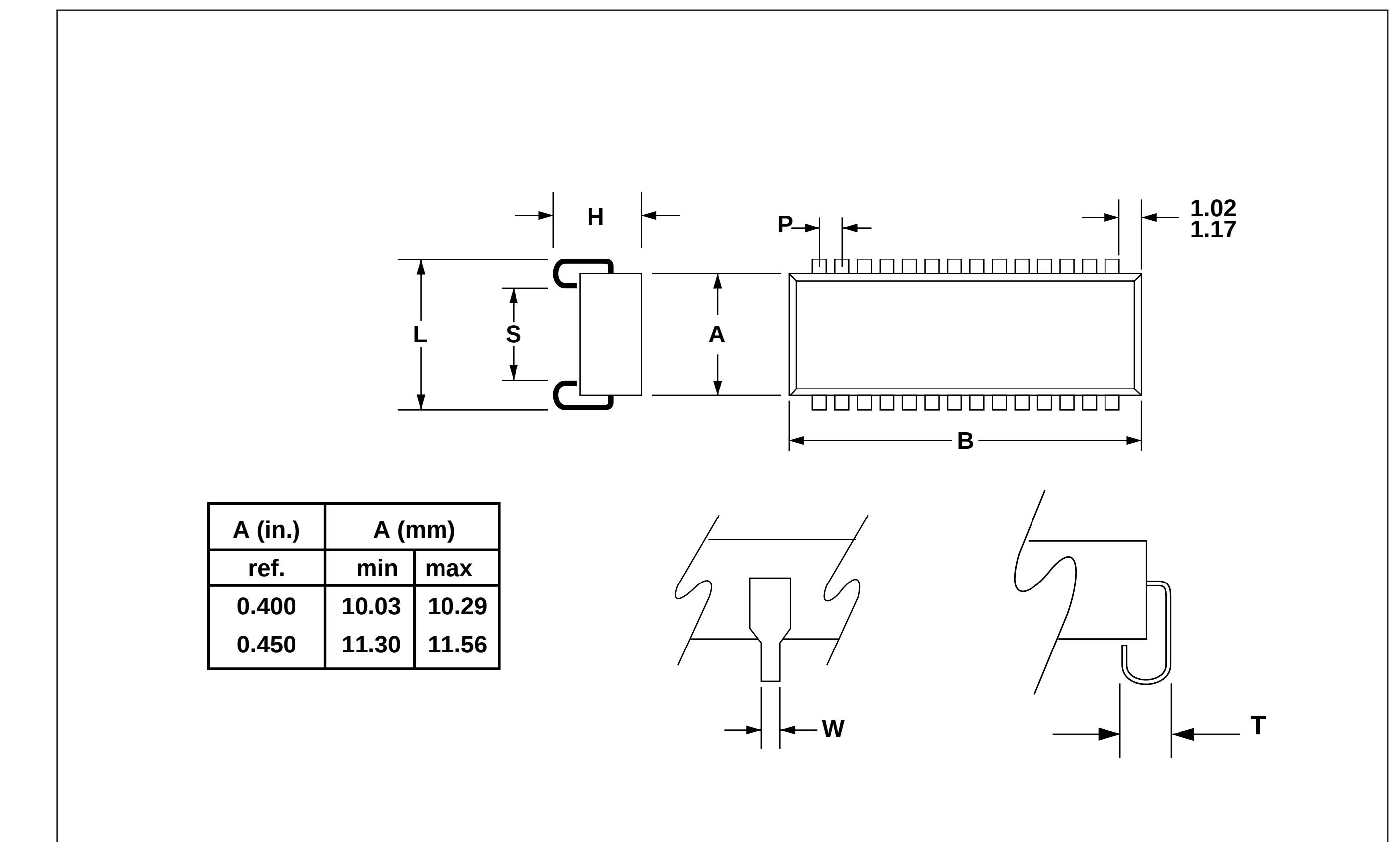
In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 6. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



RLP No.	Component Identifier (Pin Count)	Z (mm)	G (mm)	X (mm)	Y (mm) ref	C (mm) ref	D (mm) basic	E (mm) basic	Placement Grid (No. Grid Elements)
480A	SOJ 14/300	9.40	5.00	0.60	2.20	7.20	7.62	1.27	20x22
481A	SOJ 16/300	9.40	5.00	0.60	2.20	7.20	8.89	1.27	20x24
482A	SOJ 18/300	9.40	5.00	0.60	2.20	7.20	10.16	1.27	20x26
483A	SOJ 20/300	9.40	5.00	0.60	2.20	7.20	11.43	1.27	20x28
484A	SOJ 22/300	9.40	5.00	0.60	2.20	7.20	12.70	1.27	20x32
485A	SOJ 24/300	9.40	5.00	0.60	2.20	7.20	13.97	1.27	20x34
486A	SOJ 26/300	9.40	5.00	0.60	2.20	7.20	15.24	1.27	20x36
487A	SOJ 28/300	9.40	5.00	0.60	2.20	7.20	16.51	1.27	20x38
490A	SOJ 14/350	10.60	6.20	0.60	2.20	8.40	7.62	1.27	24x22
491A	SOJ 16/350	10.60	6.20	0.60	2.20	8.40	8.89	1.27	24x24
492A	SOJ 18/350	10.60	6.20	0.60	2.20	8.40	10.16	1.27	24x26
493A	SOJ 20/350	10.60	6.20	0.60	2.20	8.40	11.43	1.27	24x28
494A	SOJ 22/350	10.60	6.20	0.60	2.20	8.40	12.70	1.27	24x32
495A	SOJ 24/350	10.60	6.20	0.60	2.20	8.40	13.97	1.27	24x34
496A	SOJ 26/350	10.60	6.20	0.60	2.20	8.40	15.24	1.27	24x36
497A	SOJ 28/350	10. 60	6.20	0.60	2.20	8.40	16.51	1.27	24x38

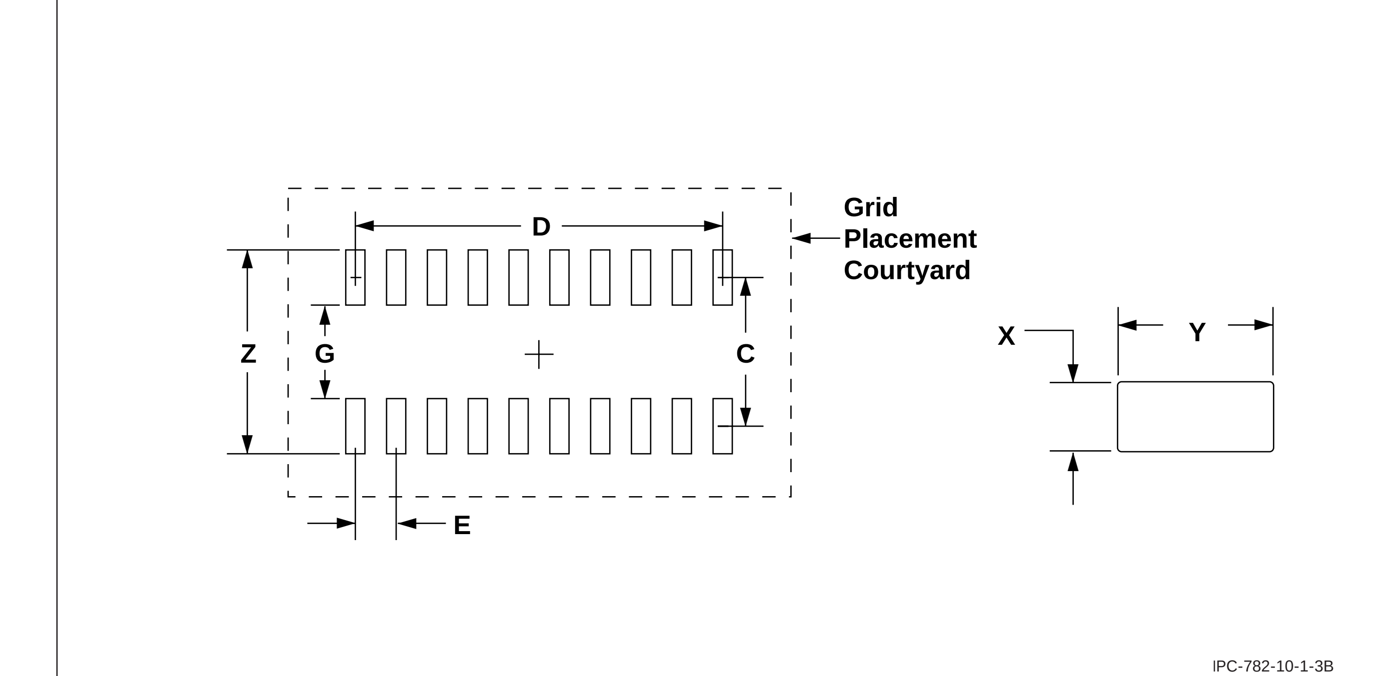
Figure 3a SOJ land pattern dimensions



A (in.)	A (mm)	
ref.	min	max
0.400	10.03	10.29
0.450	11.30	11.56

Component Identifier (Pin Count)	L (mm)		S (mm)		W (mm)		T (mm)		B (mm)		H (mm)	P (mm)
	min	max	min	max	min	max	min	max	min	max	max	basic
SOJ 14/400	10.92	11.30	6.92	7.60	0.38	0.51	1.60	2.00	9.65	9.96	3.75	1.27
SOJ 16/400	10.92	11.30	6.92	7.60	0.38	0.51	1.60	2.00	10.92	11.23	3.75	1.27
SOJ 18/400	10.92	11.30	6.92	7.60	0.38	0.51	1.60	2.00	12.19	12.50	3.75	1.27
SOJ 20/400	10.92	11.30	6.92	7.60	0.38	0.51	1.60	2.00	13.46	13.77	3.75	1.27
SOJ 22/400	10.92	11.30	6.92	7.60	0.38	0.51	1.60	2.00	14.73	15.04	3.75	1.27
SOJ 24/400	10.92	11.30	6.92	7.60	0.38	0.51	1.60	2.00	16.00	16.31	3.75	1.27
SOJ 26/400	10.92	11.30	6.92	7.60	0.38	0.51	1.60	2.00	17.27	17.58	3.75	1.27
SOJ 28/400	10.92	11.30	6.92	7.60	0.38	0.51	1.60	2.00	18.54	18.85	3.75	1.27
SOJ 14/450	12.19	12.57	8.19	8.87	0.38	0.51	1.60	2.00	9.65	9.96	3.75	1.27
SOJ 16/450	12.19	12.57	8.19	8.87	0.38	0.51	1.60	2.00	10.92	11.23	3.75	1.27
SOJ 18/450	12.19	12.57	8.19	8.87	0.38	0.51	1.60	2.00	12.19	12.50	3.75	1.27
SOJ 20/450	12.19	12.57	8.19	8.87	0.38	0.51	1.60	2.00	13.46	13.77	3.75	1.27
SOJ 22/450	12.19	12.57	8.19	8.87	0.38	0.51	1.60	2.00	14.73	15.04	3.75	1.27
SOJ 24/450	12.19	12.57	8.19	8.87	0.38	0.51	1.60	2.00	16.00	16.31	3.75	1.27
SOJ 26/450	12.19	12.57	8.19	8.87	0.38	0.51	1.60	2.00	17.27	17.58	3.75	1.27
SOJ 28/450	12.19	12.57	8.19	8.87	0.38	0.51	1.60	2.00	18.54	18.85	3.75	1.27

Figure 2b SOJ component dimensions



RLP No.	Component Identifier (Pin Count)	Z (mm)	G (mm)	X (mm)	Y (mm) ref	C (mm) ref	D (mm) basic	E (mm) basic	Placement Grid (No. Grid Elements)
500A	SOJ 14/400	11.80	7.40	0.60	2.20	9.60	7.62	1.27	26x22
501A	SOJ 16/400	11.80	7.40	0.60	2.20	9.60	8.89	1.27	26x24
502A	SOJ 18/400	11.80	7.40	0.60	2.20	9.60	10.16	1.27	26x26
503A	SOJ 20/400	11.80	7.40	0.60	2.20	9.60	11.43	1.27	26x28
504A	SOJ 22/400	11.80	7.40	0.60	2.20	9.60	12.70	1.27	26x32
505A	SOJ 24/400	11.80	7.40	0.60	2.20	9.60	13.97	1.27	26x34
506A	SOJ 26/400	11.80	7.40	0.60	2.20	9.60	15.24	1.27	26x36
507A	SOJ 28/400	11.80	7.40	0.60	2.20	9.60	16.51	1.27	26x38
510A	SOJ 14/450	13.20	8.80	0.60	2.20	11.00	7.62	1.27	28x22
511A	SOJ 16/450	13.20	8.80	0.60	2.20	11.00	8.89	1.27	28x24
512A	SOJ 18/450	13.20	8.80	0.60	2.20	11.00	10.16	1.27	28x26
513A	SOJ 20/450	13.20	8.80	0.60	2.20	11.00	11.43	1.27	28x28
514A	SOJ 22/450	13.20	8.80	0.60	2.20	11.00	12.70	1.27	28x32
515A	SOJ 24/450	13.20	8.80	0.60	2.20	11.00	13.97	1.27	28x34
516A	SOJ 26/450	13.20	8.80	0.60	2.20	11.00	15.24	1.27	28x36
517A	SOJ 28/450	13.20	8.80	0.60	2.20	11.00	16.51	1.27	28x38

Figure 3b SOJ land pattern dimensions

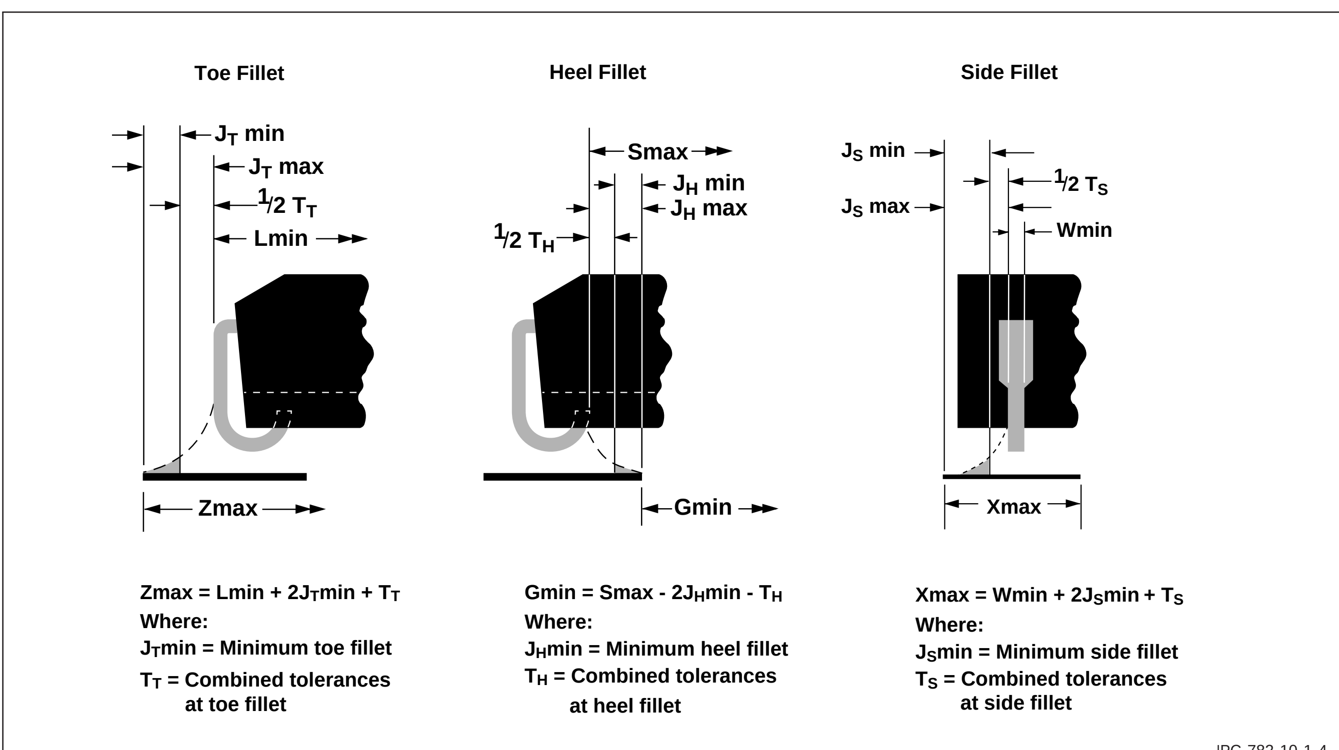
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



	Tolerance Assumptions (mm)		Solder Joint								
			Heel (mm)			Toe (mm)			Side (mm)		
RLP No.	F	P	C_S	$J_H$min	$J_H$max	C_L	$J_T$min	$J_T$max	C_W	$J_S$min	$J_S$max
480-487A	0.10	0.10	0.38	0.31	0.51	0.68	-0.32	0.03	0.13	-0.01	0.11
490-497A	0.10	0.10	0.38	0.27	0.48	0.68	-0.28	0.07	0.13	-0.01	0.11
500-507A	0.10	0.10	0.38	0.24	0.44	0.68	-0.27	0.10	0.13	-0.01	0.11
510-517A	0.10	0.10	0.38	0.30	0.51	0.68	-0.31	0.04	0.13	-0.01	0.11

Figure 4 Tolerance and solder joint analysis



IPC-SM-782

Surface Mount Design and Land Pattern Standard

Date	Section
8/93	11.0
Revision	Subject
	Components with Gullwing Leads on Four Sides

1.0 INTRODUCTION

This section covers land patterns for components with gull-wing leads on four sides. Each subsection contains information in accordance with the following format:

1.0 Scope
2.0 Applicable Documents
3.0 General Component Description (Figure 1)
4.0 Component Dimensions (Figure 2)
5.0 Land Pattern Dimensions (Figure 3)
6.0 Tolerance and Solder Joint Analysis (Figure 4)

The following is the table of contents for this section:

2.0 APPLICABLE DOCUMENTS

The following documents, of the issue in effect on the revision date of this section, form a part of this specification to the extent specified herein.

2.1 Electronic Industries Association (EIA)[1]

EIA-481-A Taping of Surface Mount Components for Automatic Placement

EIA-481-3 32 mm, 44 mm, and 56 mm Embossed Carrier Taping of Surface Mount Components for Automated Handling

JEDEC Publication 95 Registered and Standard Outlines for Solid State and Related Products:
MO 108, issue ''A,'' dated 10/90
MO 112, issue ''A,'' dated 8/90
MO 136, issue ''A,'' dated 8/92, now MS-026
MO 143, issue ''A,'' dated 3/93, now MS-029

2.2 Electronic Industries Association of Japan (EIAJ)

EIAJ-ED-7404 General Rules for the Preparation of Outline Drawings of Integrated Circuits

2.3 International Electrotechnical Commission (IEC)[2]

IEC 97 Grid Elements

3.0 General Information

3.1 General Component Description The four-sided gull wing family is characterized by gull wing leads on four sides of a square or rectangular package. The family includes both molded plastic and ceramic case styles. The acronyms PQFP, Plastic Quad Flat Pack and CQFP, Ceramic Quad Flat Pack, are also used to describe the family.

There are several lead pitches within the family from 1.0 mm to 0.30 mm. High lead-count packages are available in this family that accommodate complex, high lead-count chips.

3.2 Marking The PFQP and CQFP families of parts are generally marked with manufacturers part numbers, manufacturers name or symbol, and a pin 1 indicator. Some parts may have a pin 1 feature in the case shape instead of pin 1 marking. Additional markings may include date code/manufacturing lot and/or manufacturing location.

3.3 Carrier Package Format Components may be provided in tube but packaging tray carriers are preferred for best handling and high volume applications. Bulk packaging is not acceptable because of lead coplanarity required for placement and soldering.

3.3 Process Considerations PQFP and CQFP packages are normally processed by solder reflow operations.

High lead-count fine pitch parts may require special processing outside the normal pick/place and reflow manufacturing operations.

Separate pick/place, excise, and reflow processes are sometimes used as an alternate to normal SMT processes.

1. Application for copies should be addressed to Global Engineering Documents, 1990 M St. N.W., Washington, DC 20036.
2. Application for copies should be addressed to IEC, 3 rue de Varembe, PO Box 131 - 1211 Geneva 20, Switzerland

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IPC-SM-782

Surface Mount Design and Land Pattern Standard

Date	Section
5/96	11.1
Revision	Subject
A	PQFP

1.0 SCOPE

This subsection provides the component and land pattern dimensions for PQFP (Plastic Quad Flat Pack) components. Basic construction of the PQFP device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

2.0 APPLICABLE DOCUMENTS

See Section 11.0 and the following for documents applicable to the subsections.

Electronic Industries Association (EIA)

JEDEC Publication 95 Registered and Standard Outlines for Solid State and Related Products, ''Low Profile Plastic Quad Flat Pack Family 0.025 Lead Spacing (Gullwing), Outline MO-086, issue ''B,'' dated 6/90

Application for copies should be addressed to:
Global Engineering Documents
1990 M Street N.W.
Washington, DC

3.0 COMPONENT DESCRIPTIONS

Flatpacks are widely used in a variety of applications for commercial, industrial, or military electronics.

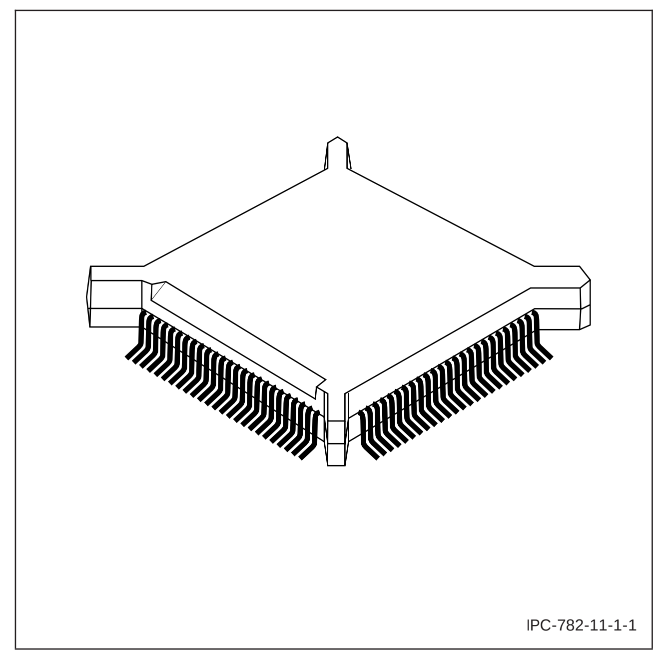


Figure 1 PQFP construction

3.1 Basic Construction See Figure 1. PQFPs have leads on a 0.635 mm pitch.

3.1.1 Termination Materials Leads must be solder-coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the leads by hot dipping or by plating from solution. Plated solder terminations should be subjected to post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

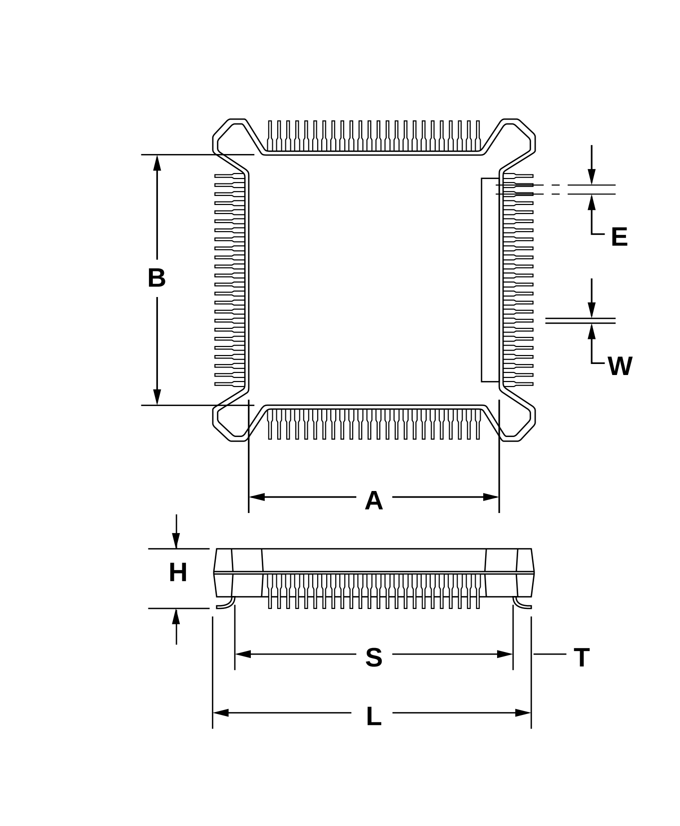
3.1.2 Marking All parts shall be marked with a part number and an index area. The index area shall identify the location of pin 1.

3.1.3 Carrier Package Format The carrier package format for PFQPs is the tube format; however, packaging trays provide the best handling capability.

3.1.4 Process Considerations PQFPs are usually processed using standard solder reflow processes. Parts should be capable of withstanding ten cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C.

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for PQFP components.



PQFP Component Identifier (Pin Count)	L (mm)		S (mm)		W (mm)		T (mm)		A (mm)	B (mm)	E (mm)	H (mm)
	min	max	min	max	min	max	min	max	max	max	basic	max
PQFP 84	19.55	20.05	17.55	18.16	0.20	0.30	0.75	1.00	16.80	16.80	0.635	4.57
PQFP 100	22.10	22.60	20.10	20.71	0.20	0.30	0.75	1.00	19.35	19.35	0.635	4.57
PQFP 132	27.20	27.70	25.25	25.81	0.20	0.30	0.75	1.00	24.40	24.40	0.635	4.57
PQFP 164	32.25	32.75	30.25	30.86	0.20	0.30	0.75	1.00	29.40	29.40	0.635	4.75
PQFP 196	37.35	37.85	35.35	35.96	0.20	0.30	0.75	1.00	34.40	34.40	0.635	4.57
PQFP 244	41.65	42.15	39.65	40.26	0.20	0.30	0.75	1.00	45.40	45.40	0.635	4.57

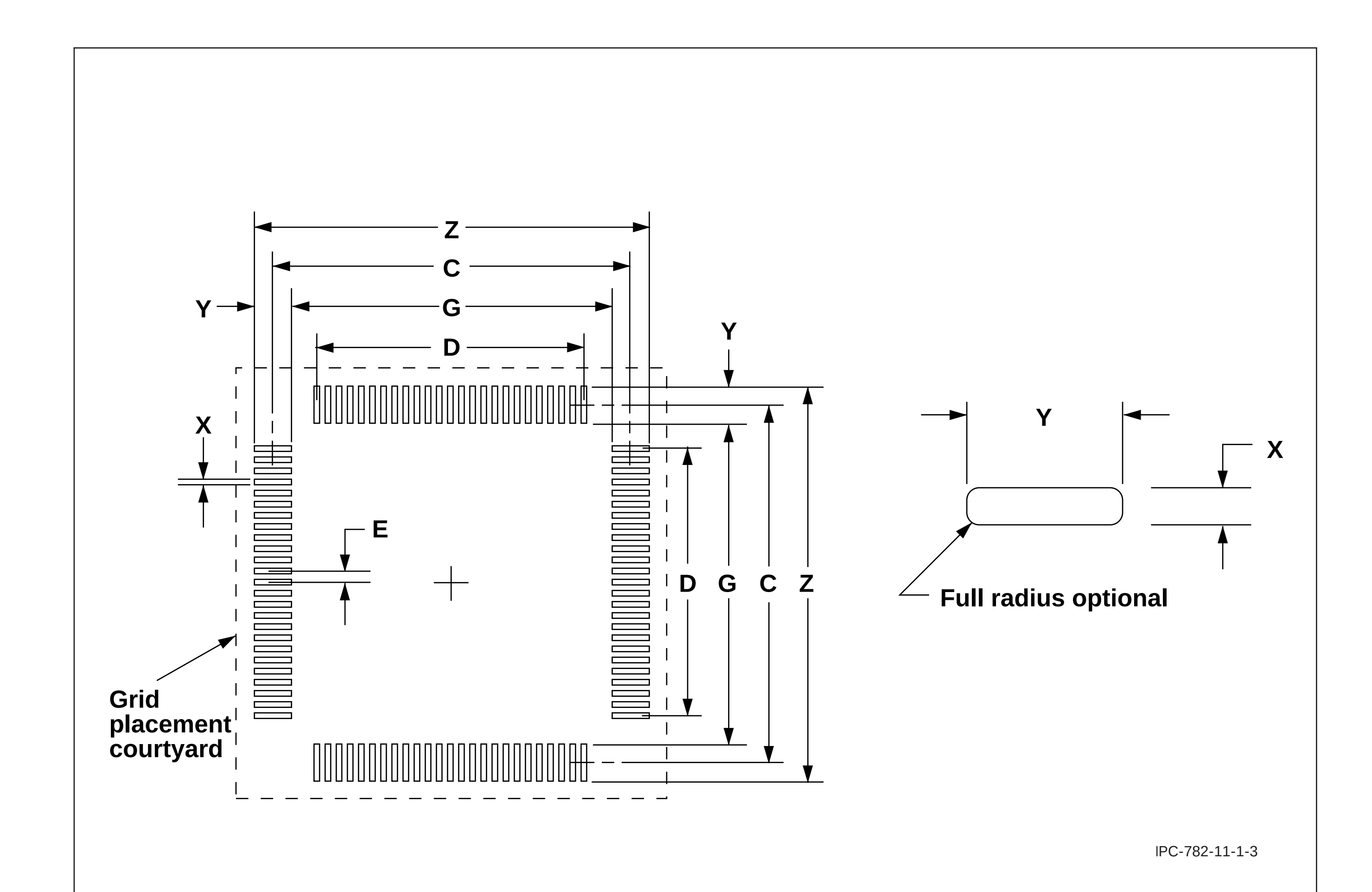
Figure 2 PQFP dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for PQFP components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



RLP No.	Component Identifier (Pin Count)	Z (mm)	G (mm)	X (mm)	Y (mm) ref	C (mm) ref	D (mm) ref	E (mm) basic	Placement Grid (No. of Grid Elements)
530A	PQFP 84	20.60	17.00	0.35	1.80	18.80	12.70	0.63	44X44
531A	PQFP 100	23.20	19.60	0.35	1.80	21.40	15.24	0.63	50X50
532A	PQFP 132	28.20	24.60	0.35	1.80	26.40	20.32	0.63	58X58
533A	PQFP 164	33.40	29.80	0.35	1.80	31.60	25.40	0.63	68X68
534A	PQFP 196	38.40	34.80	0.35	1.80	36.60	30.48	0.63	80X80
535A	PQFP 244	42.80	39.20	0.35	1.80	41.00	38.10	0.63	88X88

Figure 3

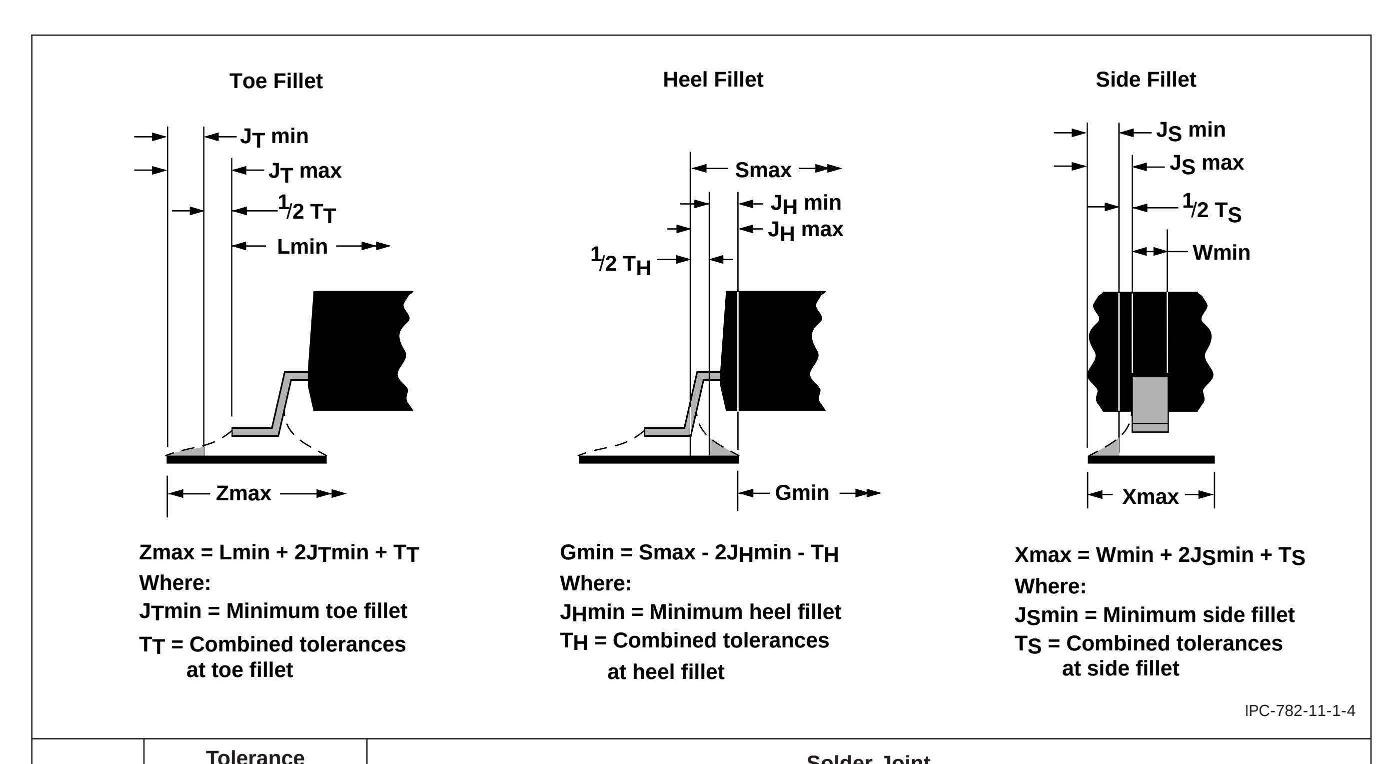
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



RLP No.	Tolerance Asssumptions (mm)		Solder Joint								
			Toe (mm)			Heel (mm)			Side (mm)		
	F	P	C_L	$J_T$min	$J_T$max	C_S	$J_H$min	$J_H$max	C_W	$J_S$min	$J_S$max
530A	0.10	0.10	0.50	0.27	0.53	0.61	0.27	0.58	0.10	-0.01	0.08
531A	0.10	0.10	0.50	0.29	0.55	0.61	0.24	0.56	0.10	-0.01	0.08
532A	0.10	0.10	0.50	0.24	0.50	0.61	0.29	0.61	0.10	-0.01	0.08
533A	0.10	0.10	0.50	0.32	0.58	0.61	0.22	0.53	0.10	-0.01	0.08
534A	0.10	0.10	0.50	0.27	0.53	0.61	0.27	0.58	0.10	-0.01	0.08
535A	0.10	0.10	0.50	0.32	0.57	0.61	0.22	0.53	0.10	-0.01	0.08

Figure 4 Tolerance and solder joint analysis

1.0 SCOPE

This subsection provides the component and land pattern dimensions for square SQFP (Shrink Quad Flat Pack) and QFP (metric plastic quad flat pack) components. Basic construction of the SQFP device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

2.0 APPLICABLE DOCUMENTS

See Section 11.0 and the following for documents applicable to this subsection.

2.1 Electronic Industries Association (EIA)

JEDEC Publication 95 Registered and Standard Outlines for Solid State and Related Products, ''Metric Quad Flat Pack Family 3.2 mm Footprint,'' Outline MO-108, issue ''A,'' dated 10/90

Application for copies should be addressed to:
Global Engineering Documents
1990 M Street N.W.
Washington, DC

2.2 Electronic Industries Association of Japan (EIAJ)

EIAJ-ED-7404-1 General Rules for the Preparation of Outline Drawings of Integrated Circuits Fine Pitch Quad Flat Packages (dated January 26, 1989)

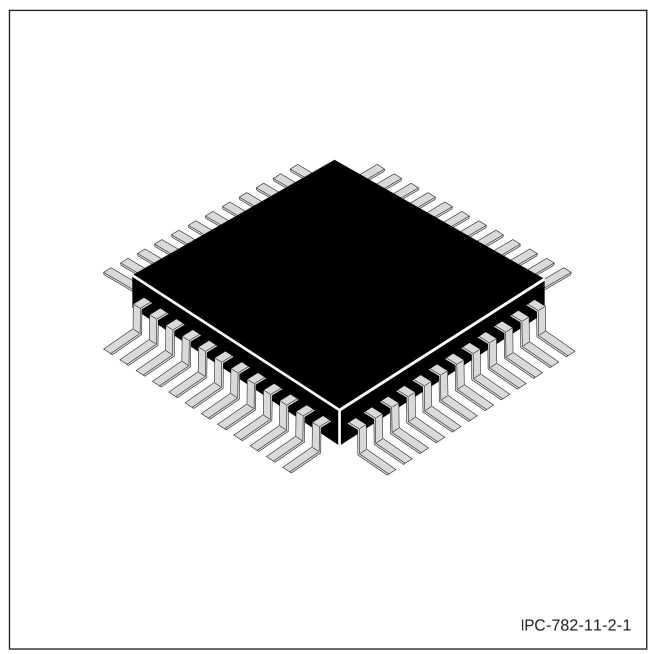


Figure 1 SQFP & QFP (Square)

3.0 COMPONENT DESCRIPTIONS

Flatpacks are widely used in a variety of applications for commercial, industrial, or military electronics.

3.1 Basic Construction

See Figure 1.

The shrink quad flat pack has been developed for applications requiring low height and high density. The SQFP, along with the TSOP components, are frequently used in memory card applications. The square SQFP family comes in 13 standard sizes, each of which sizes can come in either a 0.5, 0.4, or 0.3 mm pitch. There are therefore 39 configurations for square SQFPs.

Two different pin counts are allowed for each package and the component will still meet the standard (e.g., a 5x5 package with a 0.3 mm pitch can have either 56 or 48 pins, and still meet EIAJ-7404-1).

QFPs are also square and come in larger pitches. Wherever applicable, the body sizes of the components identified in Figures 2 and 3 show the relationships and pin numbers for SQFPs and QFPs that have the same body size.

3.1.1 Termination Materials Leads must be solder-coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the leads by hot dipping or by plating from solution. Plated solder terminations should be subjected to post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

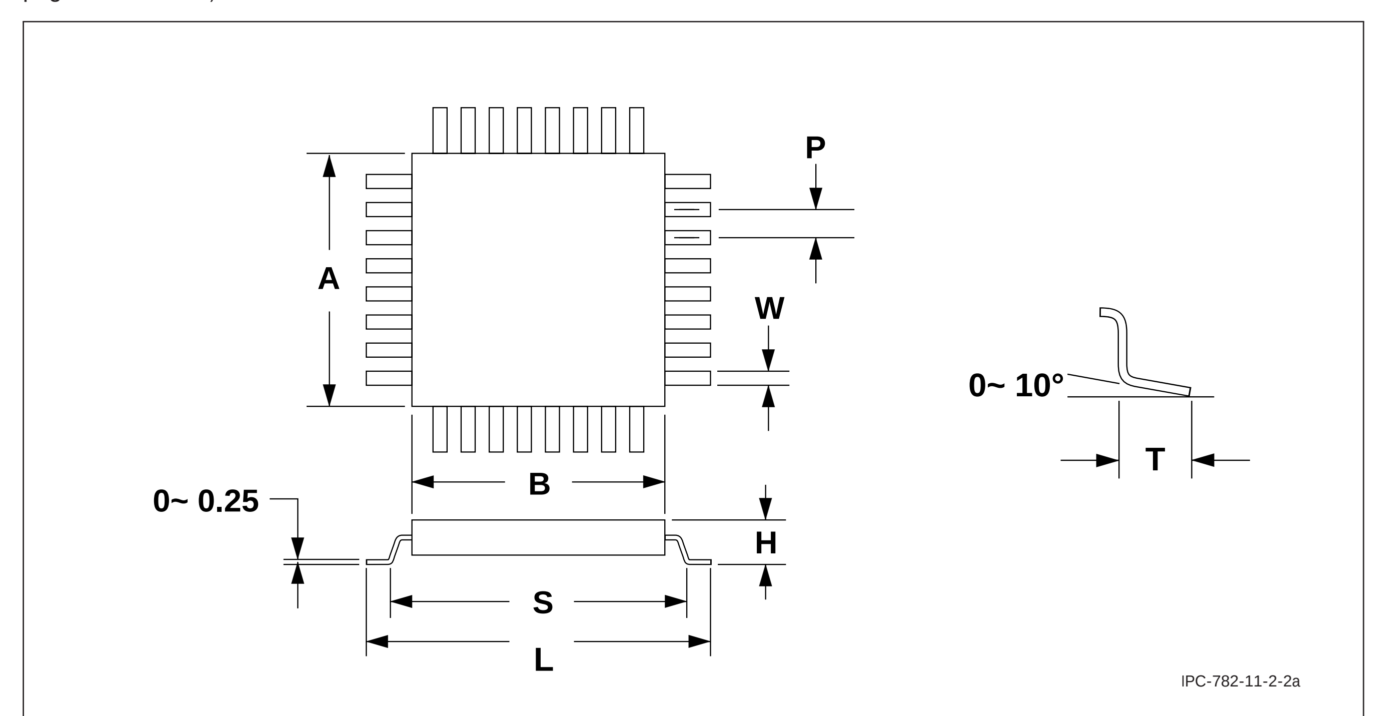
3.1.2 Marking All parts shall be marked with a part number and an index area. The index area shall identify the location of pin 1.

3.1.3 Carrier Package Format The carrier package format for flatpacks may be tube format; but, in most instances, flatpacks are delivered in a carrier tray.

3.1.4 Process Considerations SQFPs and QFPs are usually processed using standard solder reflow processes. Parts should be capable of withstanding ten cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure and 215°C.

4.0 COMPONENT DIMENSIONS

In this subsection, Figures 2a–2d provide the component dimensions for SQFP (Square) components. (Also see pages 4, 6 and 8.)



Component Identifier	L (mm)		S (mm)		W (mm)		T (mm)		A (mm)	B (mm)	P (mm)	H (mm)
	min	max	min	max	min	max	min	max	ref	ref	basic	max
SQFP 5X5-24	6.80	7.20	5.20	5.89	0.10	0.30	0.40	0.80	5.00	5.00	0.50	1.70
SQFP 5X5-32	6.80	7.20	5.20	5.89	0.10	0.30	0.40	0.80	5.00	5.00	0.50	1.70
SQFP 5X5-32-F	6.80	7.20	5.20	5.89	0.05	0.22	0.40	0.80	5.00	5.00	0.40	1.70
SQFP 5X5-40	6.80	7.20	5.20	5.89	0.05	0.22	0.40	0.80	5.00	5.00	0.40	1.70
SQFP 5X5-48	6.80	7.20	5.20	5.89	0.05	0.15	0.40	0.80	5.00	5.00	0.30	1.70
SQFP 5X5-56	6.80	7.20	5.20	5.89	0.05	0.15	0.40	0.80	5.00	5.00	0.30	1.70
SQFP 6X6-32	7.80	8.20	6.20	6.89	0.10	0.30	0.40	0.80	6.00	6.00	0.50	1.70
SQFP 6X6-40	7.80	8.20	6.20	6.89	0.10	0.30	0.40	0.80	6.00	6.00	0.50	1.70
SQFP 6X6-40-F	7.80	8.20	6.20	6.89	0.05	0.22	0.40	0.80	6.00	6.00	0.40	1.70
SQFP 6X6-48	7.80	8.20	6.20	6.89	0.05	0.22	0.40	0.80	6.00	6.00	0.40	1.70
SQFP 6X6-56	7.80	8.20	6.20	6.89	0.05	0.15	0.40	0.80	6.00	6.00	0.30	1.70
SQFP 6X6-64	7.80	8.20	6.20	6.89	0.05	0.15	0.40	0.80	6.00	6.00	0.30	1.70
SQFP 7X7-40	8.80	9.20	7.20	7.89	0.10	0.30	0.40	0.80	7.00	7.00	0.50	1.70
SQFP 7X7-48	8.80	9.20	7.20	7.89	0.10	0.30	0.40	0.80	7.00	7.00	0.50	1.70
SQFP 7X7-56	8.80	9.20	7.20	7.89	0.05	0.22	0.40	0.80	7.00	7.00	0.40	1.70
SQFP 7X7-64	8.80	9.20	7.20	7.89	0.05	0.22	0.40	0.80	7.00	7.00	0.40	1.70
SQFP 7X7-72	8.80	9.20	7.20	7.89	0.05	0.15	0.40	0.80	7.00	7.00	0.30	1.70
SQFP 7X7-80	8.80	9.20	7.20	7.89	0.05	0.15	0.40	0.80	7.00	7.00	0.30	1.70

Figure 2a SQFP (Square) component dimensions

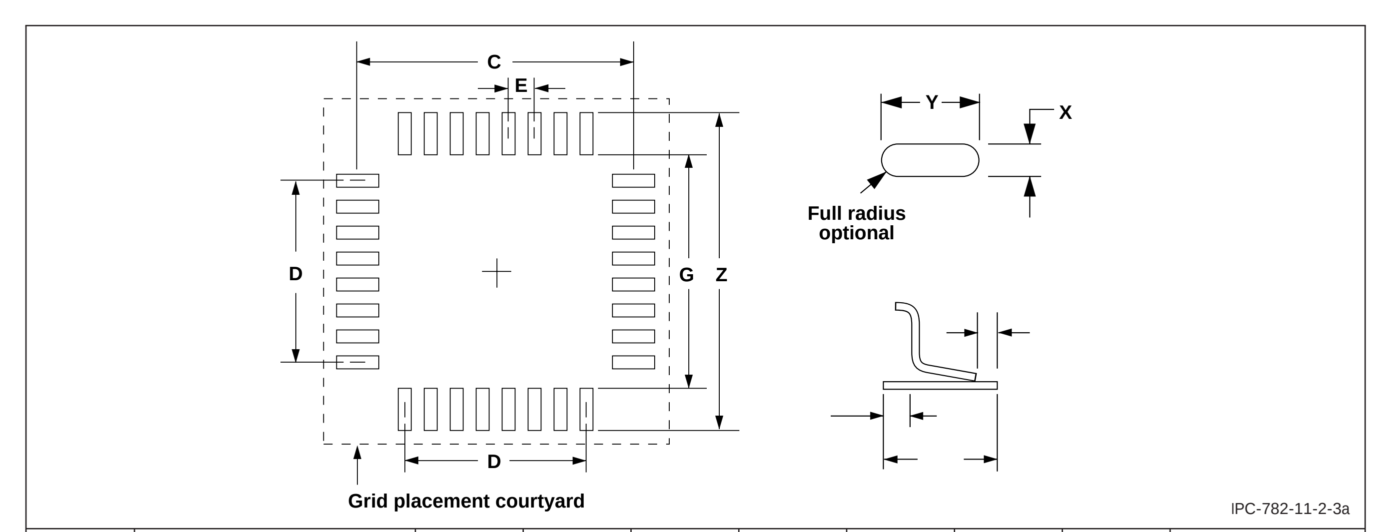
5.0 LAND PATTERN DIMENSIONS

In this subsection, Figures 3a–3d provide the land pattern dimensions for SQFP (Square) components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns. (Also see pages 5, 7, and 9.)

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 10.

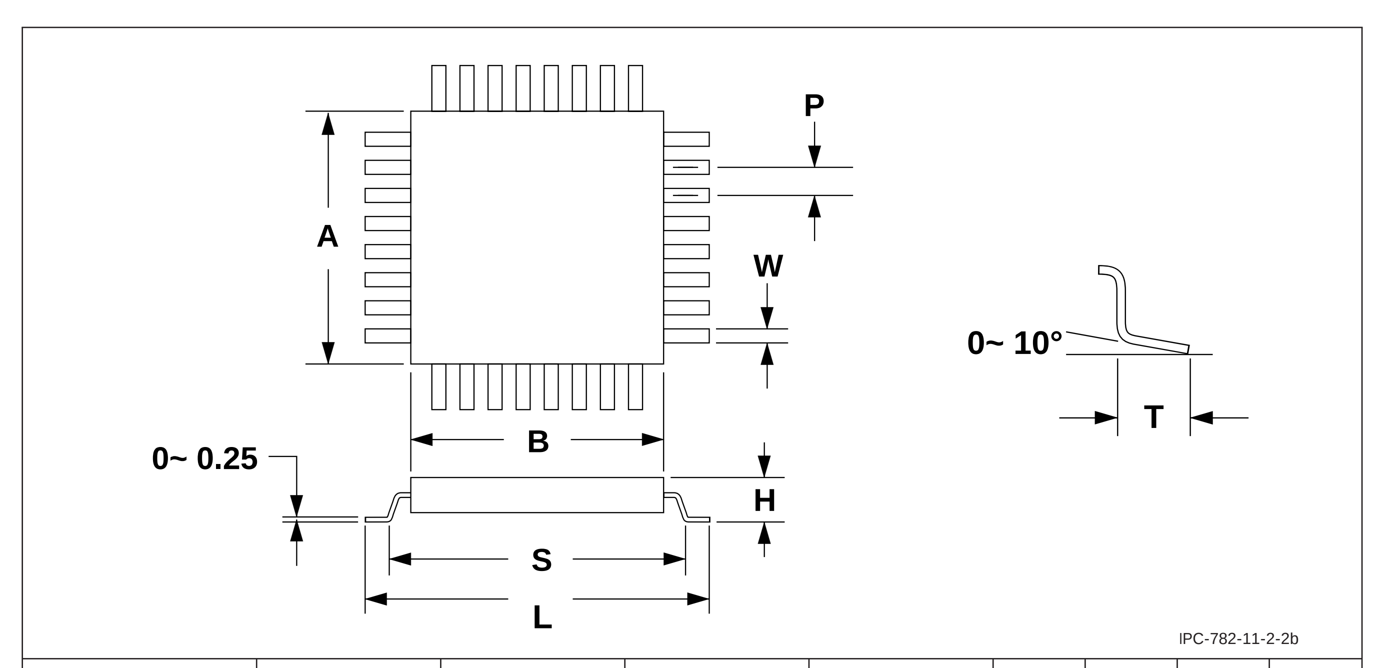
The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



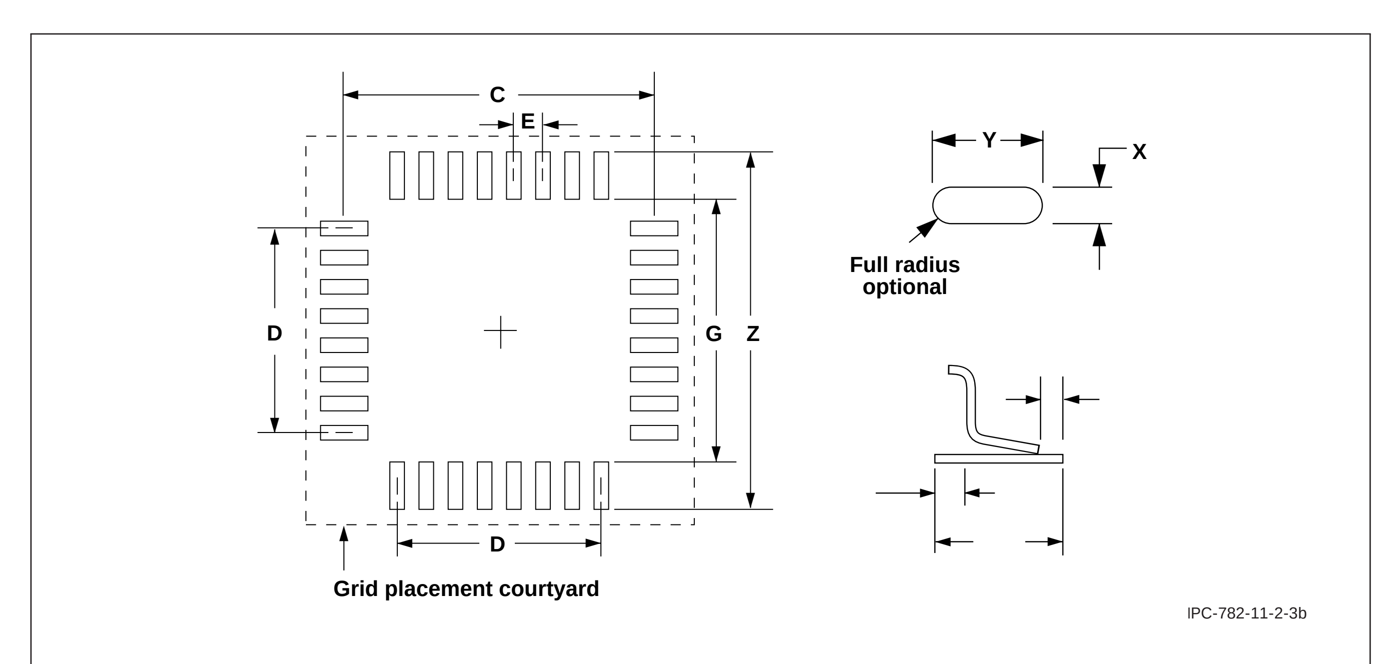
RLP No.	Component Identifier	Z (mm)	G (mm)	X (mm)	Y (mm) ref	C (mm) ref	D (mm) ref	E (mm) ref	Placement Grid (No. of Grid Elements)
550A	SQFP 5x5-24	7.80	4.60	0.30	1.60	6.20	2.50	0.50	18x18
551A	SQFP 5x5-32	7.80	4.60	0.30	1.60	6.20	3.50	0.50	18x18
552A	SQFP 5x5-32-F	7.80	4.60	0.25	1.60	6.20	2.80	0.40	18x18
553A	SQFP 5x5-40	7.80	4.60	0.25	1.60	6.20	3.60	0.40	18x18
554A	SQFP 5x5-48	7.80	4.60	0.17	1.60	6.20	3.30	0.30	18x18
555A	SQFP 5x5-56	7.80	4.60	0.17	1.60	6.20	3.90	0.30	18x18
556A	SQFP 6x6-32	8.80	5.60	0.30	1.60	7.20	3.50	0.50	20x20
557A	SQFP 6x6-40	8.80	5.60	0.30	1.60	7.20	4.50	0.50	20x20
558A	SQFP 6x6-40-F	8.80	5.60	0.25	1.60	7.20	3.60	0.40	20x20
559A	SQFP 6x6-48	8.80	5.60	0.25	1.60	7.20	4.40	0.40	20x20
560A	SQFP 6x6-56	8.80	5.60	0.17	1.60	7.20	3.90	0.30	20x20
561A	SQFP 6x6-64	8.80	5.60	0.17	1.60	7.20	4.50	0.30	20x20
562A	SQFP 7x7-40	9.80	6.60	0.30	1.60	8.20	4.50	0.50	22x22
563A	SQFP 7x7-48	9.80	6.60	0.30	1.60	8.20	5.50	0.50	22x22
564A	SQFP 7x7-56	9.80	6.60	0.25	1.60	8.20	5.20	0.40	22x22
565A	SQFP 7x7-64	9.80	6.60	0.25	1.60	8.20	6.00	0.40	22x22
566A	SQFP 7x7-72	9.80	6.60	0.17	1.60	8.20	5.10	0.30	22x22
567A	SQFP 7x7-80	9.80	6.60	0.17	1.60	8.20	5.70	0.30	22x22

Figure 3a SQFP (Square) land pattern dimensions



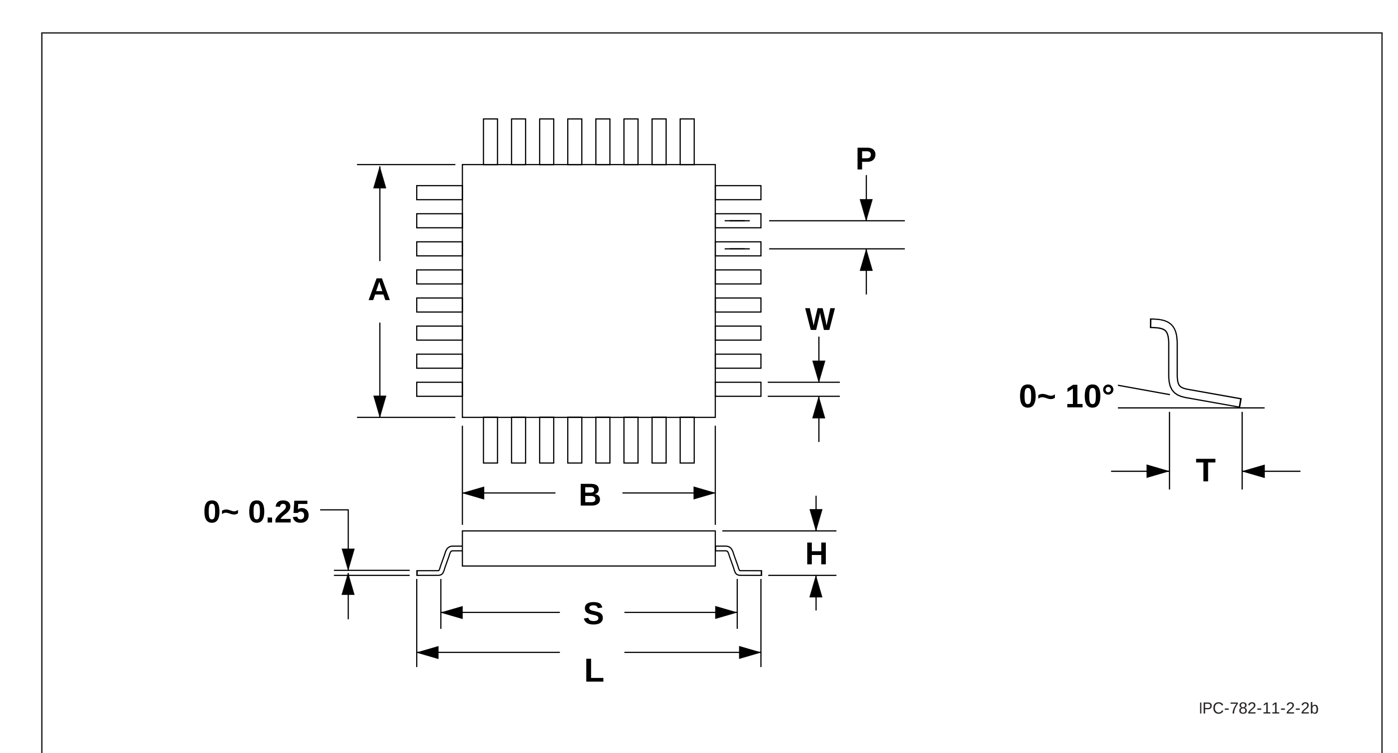
Component Identifier	L (mm)		S (mm)		W (mm)		T (mm)		A (mm)	B (mm)	P (mm)	H (mm)
	min	max	min	max	min	max	min	max	ref	ref	basic	max
QFP 10x10-44	12.95	13.45	11.05	11.71	0.30	0.45	0.65	0.95	10.00	10.00	0.80	2.45
QFP 10x10-52	12.95	13.45	11.05	11.71	0.22	0.38	0.65	0.95	10.00	10.00	0.65	2.45
SQFP 10x10-64	11.80	12.20	10.20	10.89	0.10	0.30	0.40	0.80	10.00	10.00	0.50	2.20
SQFP 10x10-72	11.80	12.20	10.20	10.89	0.10	0.30	0.40	0.80	10.00	10.00	0.50	2.20
SQFP 10x10-80	11.80	12.20	10.20	10.89	0.05	0.22	0.40	0.80	10.00	10.00	0.40	2.20
SQFP 10x10-88	11.80	12.20	10.20	10.89	0.05	0.22	0.40	0.80	10.00	10.00	0.40	2.20
SQFP 10x10-112	11.80	12.20	10.20	10.89	0.05	0.15	0.40	0.80	10.00	10.00	0.30	2.20
SQFP 10x10-120	11.80	12.20	10.20	10.89	0.05	0.15	0.40	0.80	10.00	10.00	0.30	2.20
QFP 12x12-48	15.00	15.50	13.05	13.71	0.30	0.45	0.65	0.95	12.00	12.00	0.80	2.45
QFP 12x12-64	15.00	15.50	13.05	13.71	0.22	0.38	0.65	0.95	12.00	12.00	0.65	2.45
SQFP 12x12-80	13.80	14.20	12.20	12.89	0.10	0.30	0.40	0.80	12.00	12.00	0.50	2.20
SQFP 12x12-88	13.80	14.20	12.20	12.89	0.10	0.30	0.40	0.80	12.00	12.00	0.50	2.20
SQFP 12x12-100	13.80	14.20	12.20	12.89	0.05	0.22	0.40	0.80	12.00	12.00	0.40	2.20
SQFP 12x12-108	13.80	14.20	12.20	12.89	0.05	0.22	0.40	0.80	12.00	12.00	0.40	2.20
SQFP 12x12-136	13.80	14.20	12.20	12.89	0.05	0.15	0.40	0.80	12.00	12.00	0.30	2.20
SQFP 12x12-144	13.80	14.20	12.20	12.89	0.05	0.15	0.40	0.80	12.00	12.00	0.30	2.20
QFP 14x14-64	16.95	17.45	15.05	15.71	0.30	0.45	0.65	0.95	14.00	14.00	0.80	2.45
QFP 14x14-80	16.95	17.45	15.05	15.71	0.22	0.38	0.65	0.95	14.00	14.00	0.65	2.45
SQFP 14x14-100	15.80	16.20	14.20	14.89	0.10	0.30	0.40	0.80	14.00	14.00	0.50	2.20
SQFP 14x14-108	15.80	16.20	14.20	14.89	0.10	0.30	0.40	0.80	14.00	14.00	0.50	2.20
SQFP 14x14-120	15.80	16.20	14.20	14.89	0.05	0.22	0.40	0.80	14.00	14.00	0.40	2.20
SQFP 14x14-128	15.80	16.20	14.20	14.89	0.05	0.22	0.40	0.80	14.00	14.00	0.40	2.20
SQFP 14x14-168	15.80	16.20	14.20	14.89	0.05	0.15	0.40	0.80	14.00	14.00	0.30	2.20
SQFP 14x14-176	15.80	16.20	14.20	14.89	0.05	0.15	0.40	0.80	14.00	14.00	0.30	2.20

Figure 2b SQFP/QFP (square) component dimensions



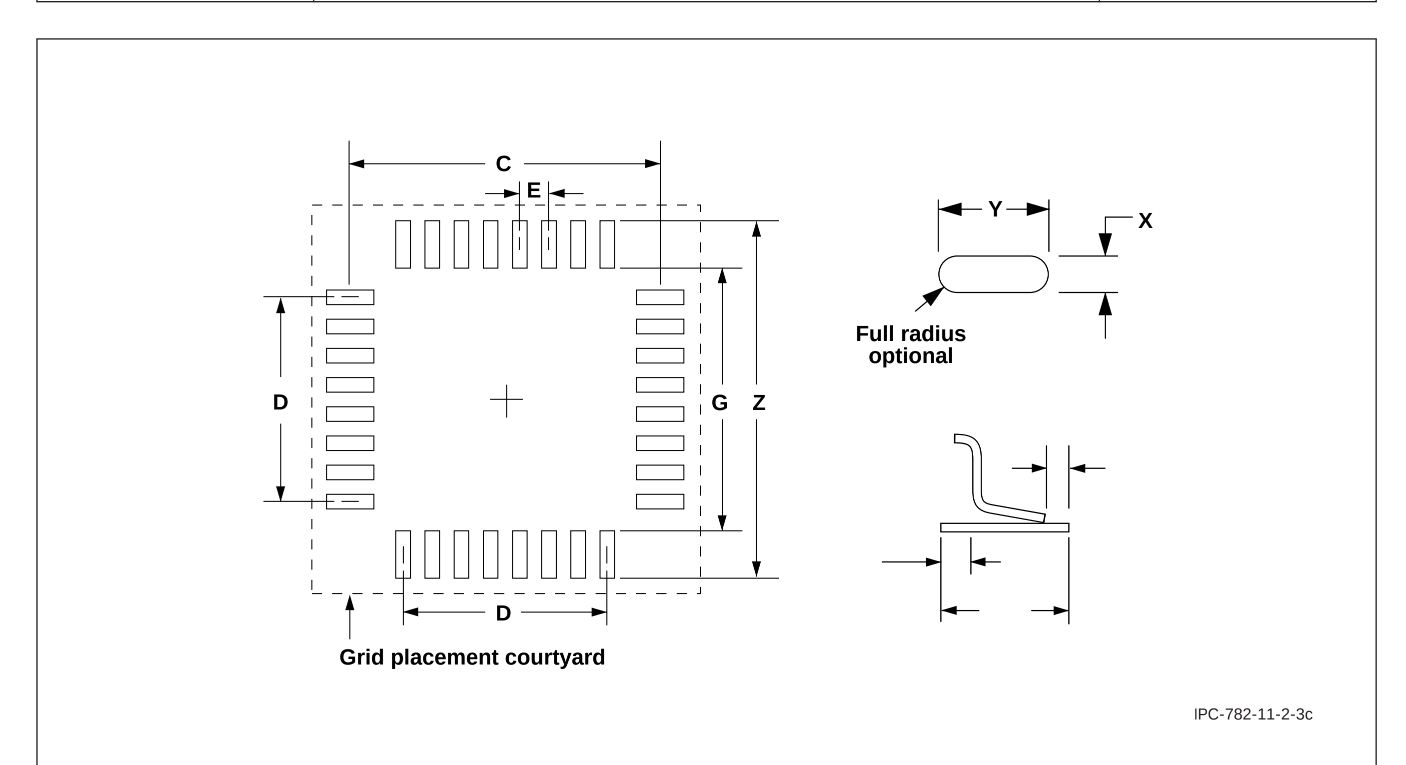
RLP No.	Component Identifier	Z (mm)	G (mm)	X (mm)	Y (mm) ref	C (mm) basic	D (mm) ref	E (mm) ref	Placement Grid (No. of Grid Elements)
570A	QFP 10x10-44	13.80	10.20	0.50	1.80	12.00	8.00	0.80	30x30
571A	QFP 10x10-52	13.80	10.20	0.40	1.80	12.00	7.80	0.65	30x30
572A	SQFP 10x10-64	12.80	9.60	0.30	1.60	11.20	7.50	0.50	28x28
573A	SQFP 10x10-72	12.80	9.60	0.30	1.60	11.20	8.50	0.50	28x28
574A	SQFP 10x10-80	12.80	9.60	0.25	1.60	11.20	7.60	0.40	28x28
575A	SQFP 10x10-88	12.80	9.60	0.25	1.60	11.20	8.40	0.40	28x28
576A	SQFP 10x10-112	12.80	9.60	0.17	1.60	11.20	8.10	0.30	28x28
577A	SQFP 10x10-120	12.80	9.60	0.17	1.60	11.20	8.70	0.30	28x28
580A	QFP 12x12-48	16.00	12.40	0.50	1.80	14.20	8.80	0.80	34x34
581A	QFP 12x12-64	16.00	12.40	0.40	1.80	14.20	9.75	0.65	34x34
582A	SQFP 12x12-80	14.80	11.60	0.30	1.60	13.20	9.50	0.50	32x32
583A	SQFP 12x12-88	14.80	11.60	0.30	1.60	13.20	10.50	0.50	32x32
584A	SQFP 12x12-100	14.80	11.60	0.25	1.60	13.20	9.60	0.40	32x32
585A	SQFP 12x12-108	14.80	11.60	0.25	1.60	13.20	10.40	0.40	32x32
586A	SQFP 12x12-136	14.80	11.60	0.17	1.60	13.20	9.90	0.30	32x32
587A	SQFP 12x12-144	14.80	11.60	0.17	1.60	13.20	10.50	0.30	32x32
590A	QFP 14x14-64	17.80	14.20	0.50	1.80	16.00	12.00	0.80	38x38
591A	QFP 14x14-80	17.80	14.20	0.40	1.80	16.00	12.35	0.65	38x38
592A	SQFP 14x14-100	16.80	13.60	0.30	1.60	15.20	12.00	0.50	36x36
593A	SQFP 14x14-108	16.80	13.60	0.30	1.60	15.20	13.00	0.50	36x36
594A	SQFP 14x14-120	16.80	13.60	0.25	1.60	15.20	11.60	0.40	36x36
595A	SQFP 14x14-128	16.80	13.60	0.25	1.60	15.20	12.40	0.40	36x36
596A	SQFP 14x14-168	16.80	13.60	0.17	1.60	15.20	12.30	0.30	36x36
597A	SQFP 14x14-176	16.80	13.60	0.17	1.60	15.20	12.90	0.30	36x36

Figure 3b SQFP/QFP (square) land pattern dimensions



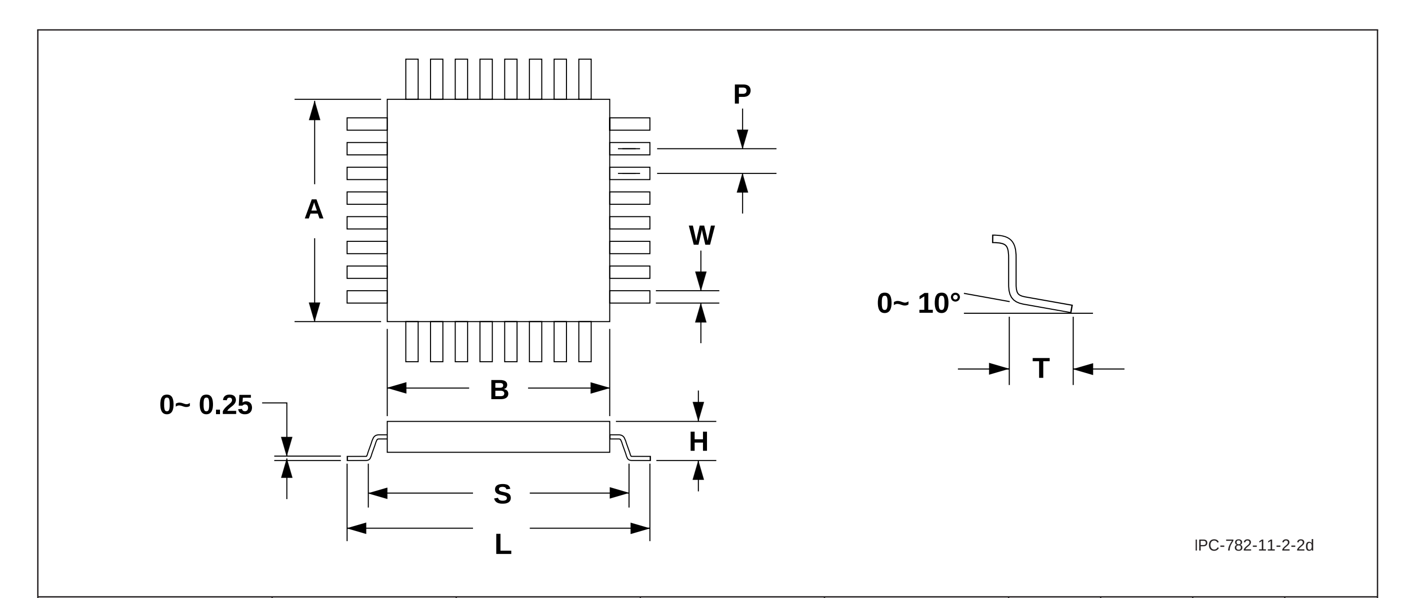
Component Identifier	L (mm)		S (mm)		W (mm)		T (mm)		A (mm)	B (mm)	P (mm)	H (mm)
	min	max	min	max	min	max	min	max	ref	ref	basic	max
SQFP 20x20-144	21.80	22.20	20.20	20.89	0.10	0.30	0.40	0.80	20.00	20.00	0.50	2.70
SQFP 20x20-152	21.80	22.20	20.20	20.89	0.10	0.30	0.40	0.80	20.00	20.00	0.50	2.70
SQFP 20x20-184	21.80	22.20	20.20	20.89	0.05	0.22	0.40	0.80	20.00	20.00	0.40	2.70
SQFP 20x20-192	21.80	22.20	20.20	20.89	0.05	0.22	0.40	0.80	20.00	20.00	0.40	2.70
SQFP 20x20-248	21.80	22.20	20.20	20.89	0.05	0.15	0.40	0.80	20.00	20.00	0.30	2.70
SQFP 20x20-256	21.80	22.20	20.20	20.89	0.05	0.15	0.40	0.80	20.00	20.00	0.30	2.70
SQFP 24x24-176	25.80	26.20	24.20	24.89	0.10	0.30	0.40	0.80	24.00	24.00	0.50	3.20
SQFP 24x24-184	25.80	26.20	24.20	24.89	0.10	0.30	0.40	0.80	24.00	24.00	0.50	3.20
SQFP 24x24-224	25.80	26.20	24.20	24.89	0.05	0.22	0.40	0.80	24.00	24.00	0.40	3.20
SQFP 24x24-232	25.80	26.20	24.20	24.89	0.05	0.22	0.40	0.80	24.00	24.00	0.40	3.20
SQFP 24x24-296	25.80	26.20	24.20	24.89	0.05	0.15	0.40	0.80	24.00	24.00	0.30	3.20
SQFP 24x24-304	25.80	26.20	24.20	24.89	0.05	0.15	0.40	0.80	24.00	24.00	0.30	3.20
QFP 28x28-120	30.95	31.45	29.05	29.71	0.30	0.45	0.65	0.95	28.00	28.00	0.80	3.75
QFP 28x28-128	30.95	31.45	29.05	29.71	0.30	0.45	0.65	0.95	28.00	28.00	0.80	3.75
QFP 28x28-144	30.95	31.45	29.05	29.71	0.22	0.38	0.65	0.95	28.00	28.00	0.65	3.75
QFP 28x28-160	30.95	31.45	29.05	29.71	0.22	0.38	0.65	0.95	28.00	28.00	0.65	3.75
SQFP 28x28-208	29.80	30.60	28.20	28.89	0.10	0.30	0.40	0.80	28.00	28.00	0.50	3.75
SQFP 28x28-216	29.80	30.60	28.20	28.89	0.10	0.30	0.40	0.80	28.00	28.00	0.50	3.75
SQFP 28x28-264	29.80	30.60	28.20	28.89	0.05	0.22	0.40	0.80	28.00	28.00	0.40	3.75
SQFP 28x28-272	29.80	30.60	28.20	28.89	0.05	0.22	0.40	0.80	28.00	28.00	0.40	3.75
SQFP 28x28-352	29.80	30.60	28.20	28.89	0.05	0.15	0.40	0.80	28.00	28.00	0.30	3.75
SQFP 28x28-360	29.80	30.60	28.20	28.89	0.05	0.15	0.40	0.80	28.00	28.00	0.30	3.75

Figure 2c SQFP/QFP (square) component dimensions



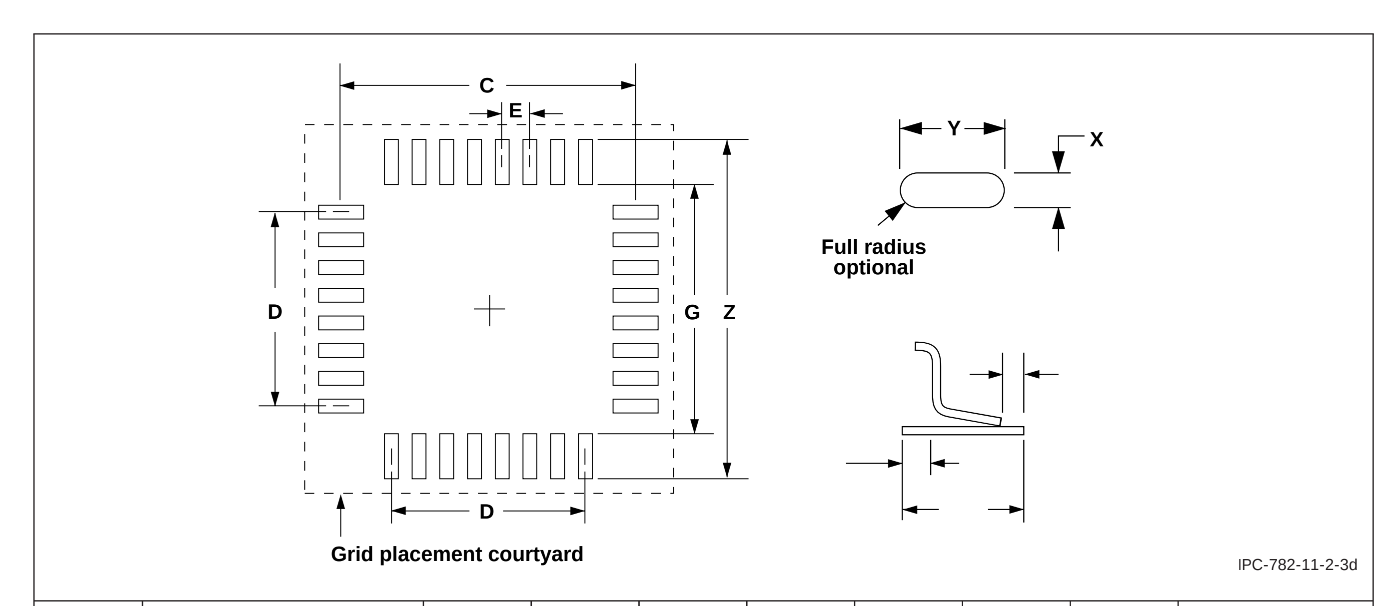
RLP No.	Component Identifier	Z (mm)	G (mm)	X (mm)	Y (mm) ref	C (mm) ref	D (mm) ref	E (mm) ref	Placement Grid (No. of Grid Elements)
600A	SQFP 20x20-144	22.80	19.60	0.30	1.60	21.20	17.50	0.50	48x48
601A	SQFP 20x20-152	22.80	19.60	0.30	1.60	21.20	18.50	0.50	48x48
602A	SQFP 20x20-184	22.80	19.60	025	1.60	21.20	18.00	0.40	48x48
603A	SQFP 20x20-192	22.80	19.60	0.25	1.60	21.20	18.80	0.40	48x48
604A	SQFP 20x20-248	22.80	19.60	0.17	1.60	21.20	18.30	0.30	48x48
605A	SQFP 20x20-256	22.80	19.60	0.17	1.60	21.20	18.90	0.30	48x48
609A	SQFP 24x24-176	26.80	23.60	0.30	1.60	25.20	21.50	0.50	56x56
610A	SQFP 24x24-184	26.80	23.60	0.30	1.60	25.20	22.50	0.50	56x56
611A	SQFP 24x24-224	26.80	23.60	0.25	1.60	25.20	22.00	0.40	56x56
612A	SQFP 24x24-232	26.80	23.60	0.25	1.60	25.20	22.80	0.40	56x56
613A	SQFP 24x24-296	26.80	23.60	0.17	1.60	25.20	21.90	0.30	56x56
614A	SQFP 24x24-304	26.80	23.60	0.17	1.60	25.20	22.50	0.30	56x56
618A	QFP 28x28-120	31.80	28.20	0.50	1.80	30.00	23.20	0.80	66x66
619A	QFP 28x28-128	31.80	28.20	0.50	1.80	30.00	24.80	0.80	66x66
620A	QFP 28x28-144	31.80	28.20	0.40	1.80	30.00	22.75	0.65	66x66
621A	QFP 28x28-160	31.80	28.20	0.40	1.80	30.00	25.35	0.65	66x66
622A	SQFP 28x28-208	30.80	27.60	0.30	1.60	29.20	25.50	0.50	64x64
623A	SQFP 28x28-216	30.80	27.60	0.30	1.60	29.20	26.50	0.50	64x64
624A	SQFP 28x28-264	30.80	27.60	0.25	1.60	29.20	26.00	0.40	64x64
625A	SQFP 28x28-272	30.80	27.60	0.25	1.60	29.20	26.80	0.40	64x64
626A	SQFP 28x28-352	30.80	27.60	0.17	1.60	29.20	26.10	0.30	64x64
627A	SQFP 28x28-360	30.80	27.60	0.17	1.60	29.20	26.70	0.30	64x64

Figure 3c SQFP/QFP (square) land pattern dimensions



Component Identifier	L (mm)		S (mm)		W (mm)		T (mm)		A (mm)	B (mm)	P (mm)	H (mm)
	min	max	min	max	min	max	min	max	ref	ref	basic	max
QFP 32x32-184	34.95	35.45	33.05	33.71	0.22	0.38	0.65	0.95	32.00	32.00	0.65	4.20
SQFP 32x32-240	33.80	34.20	32.20	32.89	0.10	0.30	0.40	0.80	32.00	32.00	0.50	4.20
SQFP 32x32-248	33.80	34.20	32.20	32.89	0.10	0.30	0.40	0.80	32.00	32.00	0.50	4.20
SQFP 32x32-304	33.80	34.20	32.20	32.89	0.05	0.22	0.40	0.80	32.00	32.00	0.40	4.20
SQFP 32x32-312	33.80	34.20	32.20	32.89	0.05	0.22	0.40	0.80	32.00	32.00	0.40	4.20
SQFP 32x32-400	33.80	34.20	32.20	32.89	0.05	0.15	0.40	0.80	32.00	32.00	0.30	4.20
SQFP 32x32-408	33.80	34.20	32.20	32.89	0.05	0.15	0.40	0.80	32.00	32.00	0.30	4.20
SQFP 36x36-272	37.80	38.20	36.20	36.89	0.10	0.30	0.40	0.80	36.00	36.00	0.50	4.20
SQFP 36x36-280	37.80	38.20	36.20	36.89	0.10	0.30	0.40	0.80	36.00	36.00	0.50	4.20
SQFP 36x36-344	37.80	38.20	36.20	36.89	0.05	0.22	0.40	0.80	36.00	36.00	0.40	4.20
SQFP 36x36-352	37.80	38.20	36.20	36.89	0.05	0.22	0.40	0.80	36.00	36.00	0.40	4.20
SQFP 36x36-456	37.80	38.20	36.20	36.89	0.05	0.15	0.40	0.80	36.00	36.00	0.30	4.20
SQFP 36x36-464	37.80	38.20	36.20	36.89	0.05	0.15	0.40	0.80	36.00	36.00	0.30	4.20
QFP 40x40-232	42.95	43.45	41.05	41.71	0.22	0.38	0.65	0.95	40.00	40.00	0.65	4.20
SQFP 40x40-304	41.80	42.20	40.20	40.89	0.10	0.30	0.40	0.80	40.00	40.00	0.50	4.20
SQFP 40x40-312	41.80	42.20	40.20	40.89	0.10	0.30	0.40	0.80	40.00	40.00	0.50	4.20
SQFP 40x40-384	41.80	42.20	40.20	40.89	0.05	0.22	0.40	0.80	40.00	40.00	0.40	4.20
SQFP 40x40-392	41.80	42.20	40.20	40.89	0.05	0.22	0.40	0.80	40.00	40.00	0.40	4.20
SQFP 40x40-512	41.80	42.20	40.20	40.89	0.05	0.15	0.40	0.80	40.00	40.00	0.30	4.20
SQFP 40x40-520	41.80	42.20	40.20	40.89	0.05	0.15	0.40	0.80	40.00	40.00	0.30	4.20
SQFP 44x44-336	45.80	46.20	44.20	44.89	0.10	0.30	0.40	0.80	44.00	44.00	0.50	4.20
SQFP 44x44-344	45.80	46.20	44.20	44.89	0.10	0.30	0.40	0.80	44.00	44.00	0.50	4.20
SQFP 44x44-424	45.80	46.20	44.20	44.89	0.05	0.22	0.40	0.80	44.00	44.00	0.40	4.20
SQFP 44x44-432	45.80	46.20	44.20	44.89	0.05	0.22	0.40	0.80	44.00	44.00	0.40	4.20
SQFP 44x44-568	45.80	46.20	44.20	44.89	0.05	0.15	0.40	0.80	44.00	44.00	0.30	4.20
SQFP 44x44- 576	45.80	46.20	44.20	44.89	0.05	0.15	0.40	0.80	44.00	44.00	0.30	4.20

Figure 2d SQFP/QFP (square) component dimensions



RLP No.	Component Identifier	Z (mm)	G (mm)	X (mm)	Y (mm) ref	C (mm) ref	D (mm) ref	E (mm) ref	Placement Grid (No. of Grid Elements)
630A	QFP 32x32-184	35.80	32.20	0.40	1.80	34.00	29.25	0.65	74x74
631A	SQFP 32x32-240	34.80	31.60	0.30	1.60	33.20	29.50	0.50	72x72
632A	SQFP 32x32-248	34.80	31.60	0.30	1.60	33.20	30.50	0.50	72x72
633A	SQFP 32x32-304	34.80	31.60	0.25	1.60	33.20	30.00	0.40	72x72
634A	SQFP 32x32-312	34.80	31.60	0.25	1.60	33.20	30.80	0.40	72x72
635A	SQFP 32x32-400	34.80	31.60	0.17	1.60	33.20	29.70	0.30	72x72
636A	SQFP 32x32-408	34.80	35.60	0.17	1.60	33.20	30.30	0.30	72x72
640A	SQFP 36x36-272	38.80	35.60	0.30	1.60	37.20	33.50	0.50	80x80
641A	SQFP 36x36-280	38.80	35.60	0.30	1.60	37.20	34.50	0.50	80x80
642A	SQFP 36x36-344	38.80	35.60	0.25	1.60	37.20	34.00	0.40	80x80
643A	SQFP 36x36-352	38.80	35.60	0.25	1.60	37.20	34.80	0.40	80x80
644A	SQFP 36x36-456	38.80	35.60	0.17	1.60	37.20	33.90	0.30	80x80
645A	SQFP 36x36-464	38.80	35.60	0.17	1.60	37.20	34.50	0.30	80x80
650A	QFP 40x40-232	43.80	40.20	0.40	1.80	42.00	37.05	0.65	90x90
651A	SQFP 40x40-304	42.80	39.60	0.30	1.60	41.20	37.50	0.50	88x88
652A	SQFP 40x40-312	42.80	39.60	0.30	1.60	41.20	38.50	0.50	88x88
653A	SQFP 40x40-384	42.80	39.60	0.25	1.60	41.20	38.00	0.40	88x88
654A	SQFP 40x40-392	42.80	39.60	0.25	1.60	41.20	38.80	0.40	88x88
655A	SQFP 40x40-512	42.80	39.60	0.17	1.60	41.20	38.10	0.30	88x88
656A	SQFP 40x40-520	42.80	39.60	0.17	1.60	41.20	38.70	0.30	88x88
660A	SQFP 44x44-336	46.80	43.60	0.30	1.60	45.20	41.50	0.50	96x96
661A	SQFP 44x44-344	46.80	43.60	0.30	1.60	45.20	42.50	0.50	96x96
662A	SQFP 44x44-424	46.80	43.60	0.25	1.60	45.20	42.00	0.40	96x96
663A	SQFP 44x44-432	46.80	43.60	0.25	1.60	45.20	42.80	0.40	96x96
664A	SQFP 44x44-568	46.80	43.60	0.17	1.60	45.20	42.30	0.30	96x96
665A	SQFP 44x44-576	46.80	43.60	0.17	1.60	45.20	42.90	0.30	96x96

Figure 3d SQFP/QFP (square) land pattern dimensions

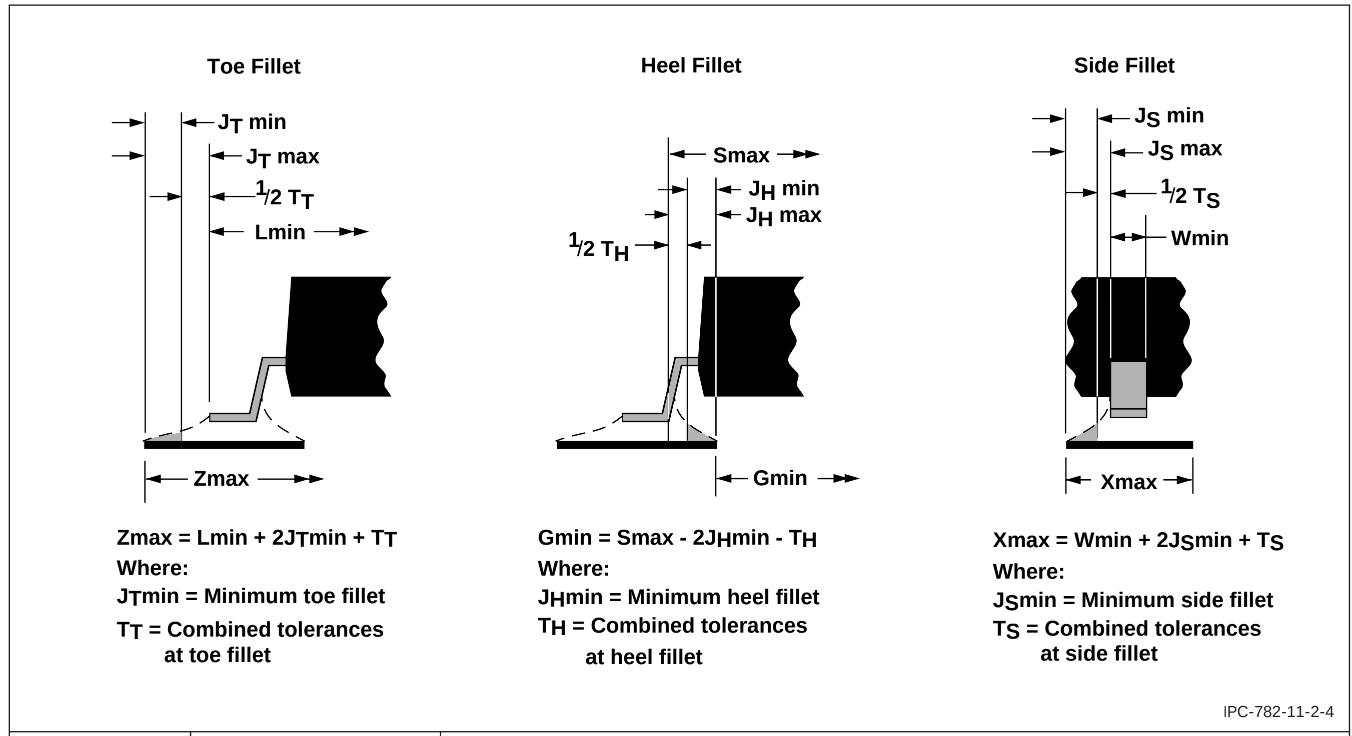
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



Component Pitch (mm)	Tolerance Assumptions (mm)		Solder Joint								
			Toe (mm)			Heel (mm)			Side (mm)		
Basic	F	P	C_L	J_T min	$J_T$max	C_S	$J_H$min	$J_H$max	C_w	$J_S$min	$J_S$max
0.80	0.10	0.10	0.50	0.17	0.43	0.66	0.42	0.75	0.15	0.00	0.10
0.65	0.10	0.10	0.50	0.17	0.43	0.66	0.42	0.75	0.16	–0.02	0.09
0.50	0.10	0.10	0.50	0.29	0.50	0.69	0.29	0.65	0.20	–0.02	0.10
0.40	0.10	0.10	0.50	0.29	0.50	0.69	0.29	0.65	0.17	–0.01	0.10
0.30	0.10	0.10	0.50	0.29	0.50	0.69	0.29	0.65	0.10	–0.03	0.06

Figure 4 Tolerance and solder joint analysis



IPC-SM-782

Surface Mount Design and Land Pattern Standard

Date	Section
5/96	11.3
Revision	Subject
A	SQFP/QFP (Rectangular)

1.0 SCOPE

This subsection provides the component and land pattern dimensions for rectangular SQFP (Shrink Quad Flat Pack) and the QFP (metric plastic quad flat pack) components. Basic construction of the SQFP device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

2.0 APPLICABLE DOCUMENTS

See Section 11.0 for documents applicable to the subsections.

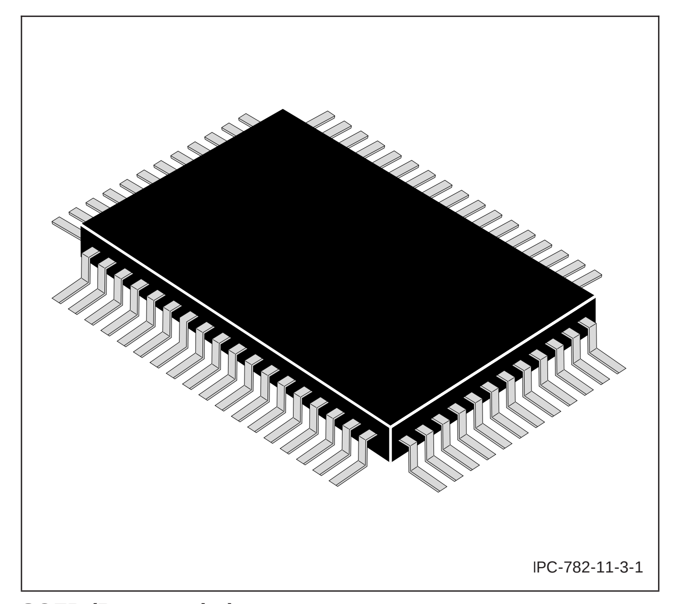
2.1 Electronic Industries Association (EIA)

JEDEC Publication 95 Registered and Standard Outlines for Solid State and Related Products, ''Metric Quad Flat Pack Family 3.2 mm Footprint,'' Outline MO-108, issue ''A,'' dated 10/90

Application for copies should be addressed to:
Global Engineering Documents
1990 M Street N.W.
Washington, DC

2.2 Electronic Industries Association of Japan (EIAJ)

EIAJ-ED-7404-1 General Rules for the Preparation of Outline Drawings of Integrated Circuits Fine Pitch Quad Flat Packages (dated January 26, 1989)



SQFP (Rectangular)

3.0 COMPONENT DESCRIPTIONS

Flatpacks are widely used in a variety of applications for commercial, industrial, or military electronics.

3.1 Basic Construction

See Figure 1.

The shrink quad flat pack has been developed for applications requiring low height and high density. The SQFP, along with the TSOP components, are frequently used in memory card applications. The square SQFP family comes in 13 standard sizes, each of which sizes can come in either a 0.5, 0.4, or 0.3 mm pitch. There are therefore 39 configurations for square SQFPs.

Two different pin counts are allowed for each package and the component will still meet the standard (e.g., a 5x5 package with a 0.3 mm pitch can have either 56 or 48 pins, and still meet EIAJ-7404-1).

QFPs are also square and come in larger pitches. Wherever applicable, the body sizes of the components identified in Figures 2 and 3 show the relationships and pin numbers for SQFPs and QFPs that have the same body size.

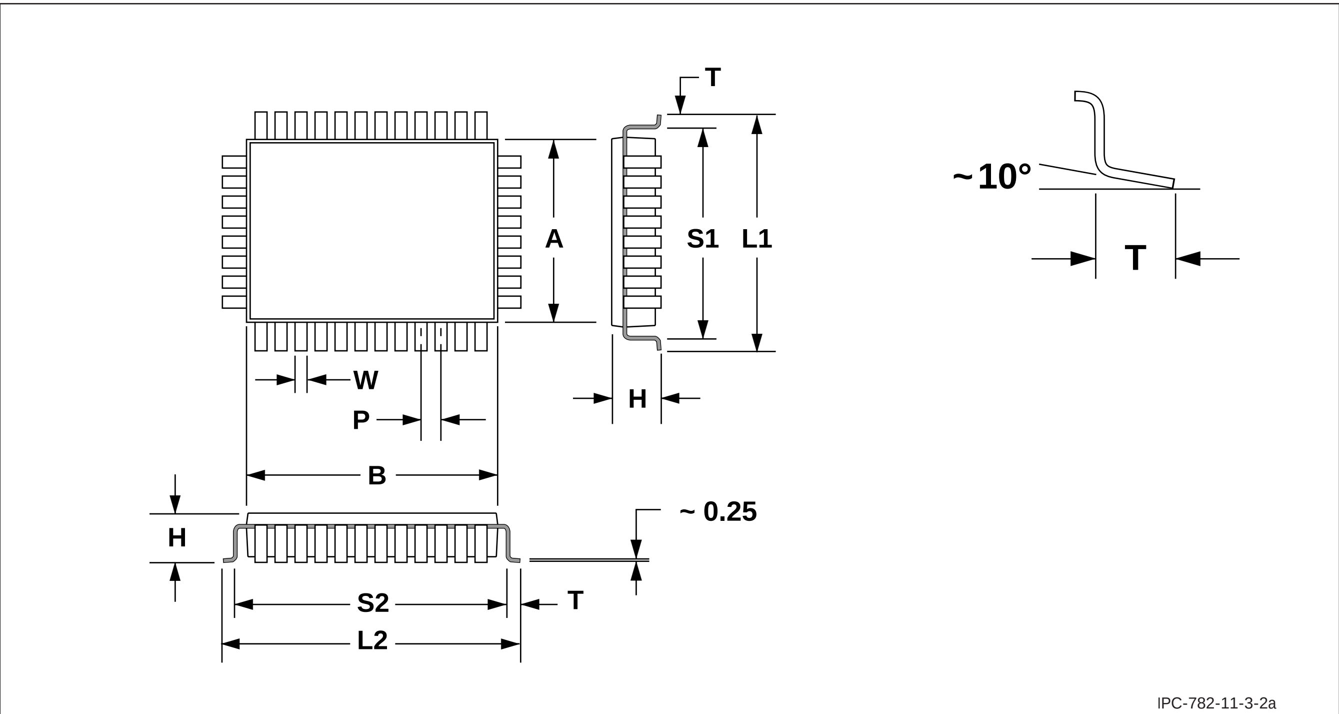
3.1.1 Termination Materials Leads must be solder-coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the leads by hot dipping or by plating from solution. Plated solder terminations should be subjected to post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

3.1.2 Marking All parts shall be marked with a part number and an index area. The index area shall identify the location of pin 1.

3.1.3 Carrier Package Format The carrier package format for flat packs may be tube format; but, in most instances, flat packs are delivered in a carrier tray.

3.1.4 Process Considerations SQFPs and QFPs are usually processed using standard solder reflow processes. Parts should be capable of withstanding ten cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C.

4.0 Component Dimensions In this subsection, Figures 2a-2b provide the component dimensions for SOJ components. (Also see page 4.)



Component Identifier	L1 (mm)		S1 (mm)		L2 (mm)		S2 (mm)		W (mm)		T (mm)		P (mm)	H (mm)	A (mm)	B (mm)	Pin count, short side	Pin count, long side
	min	max	min	max	min	max	min	max	min	max	min	max	basic	max	ref	ref		
SQFP 5X7-32	6.80	7.20	5.20	5.89	8.80	9.20	7.20	7.89	0.10	0.30	0.40	0.80	0.50	1.70	5.00	7.00	6	10
SQFP 5X7-40	6.80	7.20	5.20	5.89	8.80	9.20	7.20	7.89	0.10	0.30	0.40	0.80	0.50	1.70	5.00	7.00	8	12
SQFP 5X7-44	6.80	7.20	5.20	5.89	8.80	9.20	7.20	7.89	0.05	0.22	0.40	0.80	0.40	1.70	5.00	7.00	8	14
SQFP 5X7-52	6.80	7.20	5.20	5.89	8.80	9.20	7.20	7.89	0.05	0.22	0.40	0.80	0.40	1.70	5.00	7.00	10	16
SQFP 5X7-60	6.80	7.20	5.20	5.89	8.80	9.20	7.20	7.89	0.05	0.15	0.40	0.80	0.30	1.70	5.00	7.00	12	18
SQFP 5X7-68	6.80	7.20	5.20	5.89	8.80	9.20	7.20	7.89	0.05	0.15	0.40	0.80	0.30	1.70	7.00	10.00	14	20
SQFP 7X10-52	8.80	9.20	7.20	7.89	11.80	12.20	10.20	10.89	0.10	0.30	0.40	0.80	0.50	2.20	7.00	10.00	10	16
SQFP 7X10-60	8.80	9.20	7.20	7.89	11.80	12.20	10.20	10.89	0.10	0.30	0.40	0.80	0.50	2.20	7.00	10.00	12	18
SQFP 7X10-68	8.80	9.20	7.20	7.89	11.80	12.20	10.20	10.89	0.05	0.22	0.40	0.80	0.40	2.20	7.00	10.00	14	20
SQFP 7X10-76	8.80	9.20	7.20	7.89	11.80	12.20	10.20	10.89	0.05	0.22	0.40	0.80	0.40	2.20	7.00	10.00	16	22
SQFP 7X10-92	8.80	9.20	7.20	7.89	11.80	12.20	10.20	10.89	0.05	0.15	0.40	0.80	0.30	2.20	7.00	10.00	18	28
SQFP 7X10-100	8.80	9.20	7.20	7.89	11.80	12.20	10.20	10.89	0.05	0.15	0.40	0.80	0.30	2.20	7.00	10.00	20	30
SQFP 10X14-80	11.80	12.20	10.20	10.89	15.80	16.20	14.20	14.89	0.10	0.30	0.40	0.80	0.50	2.20	10.00	14.00	16	24
SQFP 10X14-88	11.80	12.20	10.20	10.89	15.80	16.20	14.20	14.89	0.10	0.30	0.40	0.80	0.50	2.20	10.00	14.00	18	26
SQFP 10X14-100	11.80	12.20	10.20	10.89	15.80	16.20	14.20	14.89	0.05	0.22	0.40	0.80	0.40	2.20	10.00	14.00	20	30
SQFP 10X14-108	11.80	12.20	10.20	10.89	15.80	16.20	14.20	14.89	0.05	0.22	0.40	0.80	0.40	2.20	10.00	14.00	22	32
SQFP 10X14-140	11.80	12.20	10.20	10.89	15.80	16.20	14.20	14.89	0.05	0.15	0.40	0.80	0.30	2.20	10.00	14.00	28	42
SQFP 10X14-148	11.80	12.20	10.20	10.89	15.80	16.20	14.20	14.89	0.05	0.15	0.40	0.80	0.30	2.20	10.00	14.00	30	44

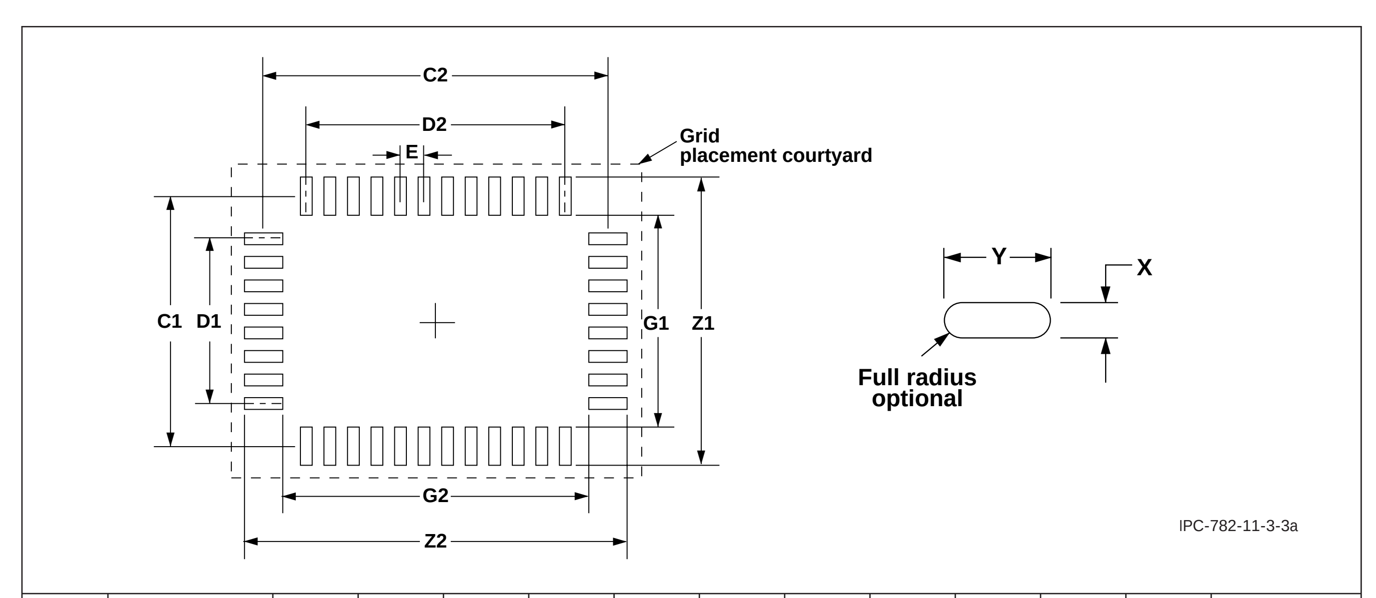
Figure 2a SQFP (Rectangular) component dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for SQFP (Rectangular) components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

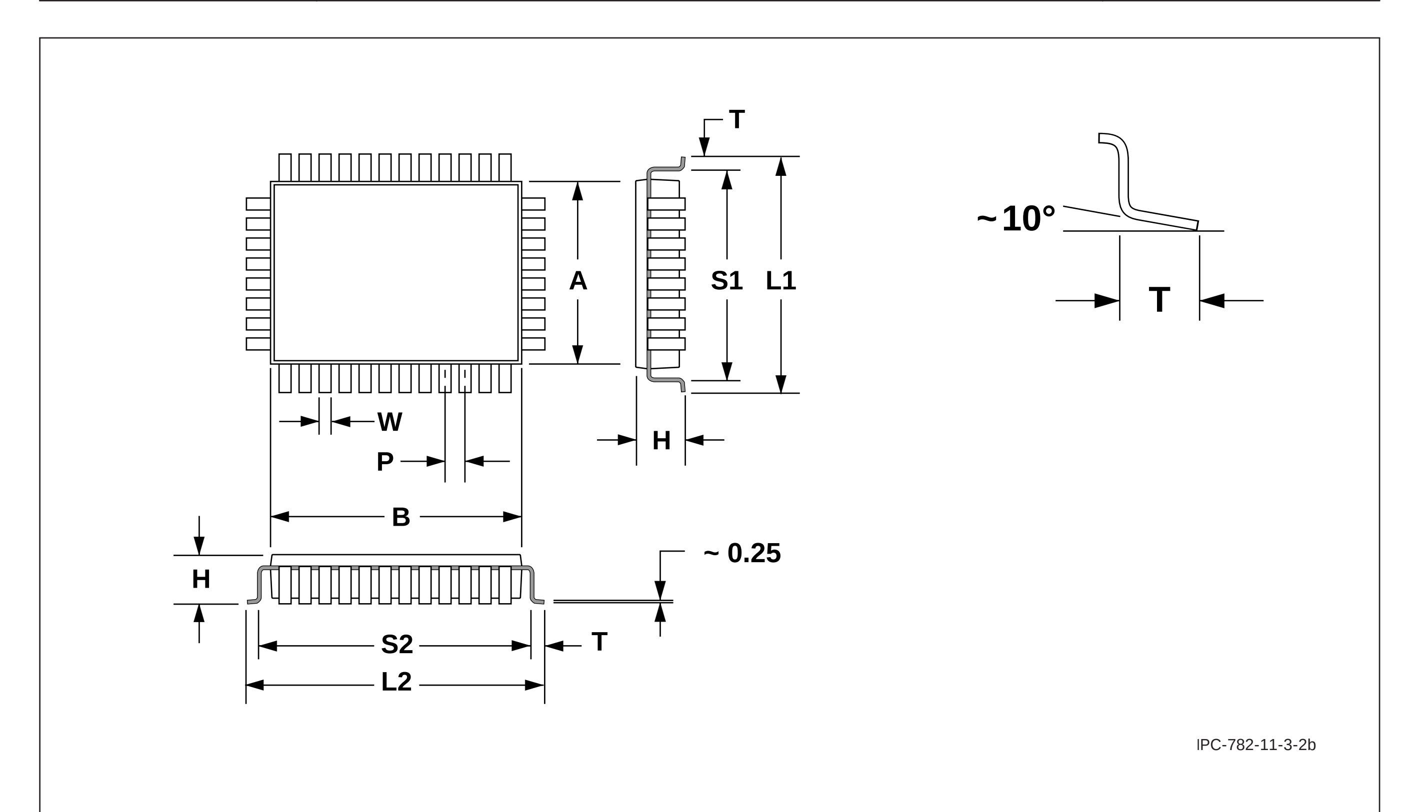
In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 6. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



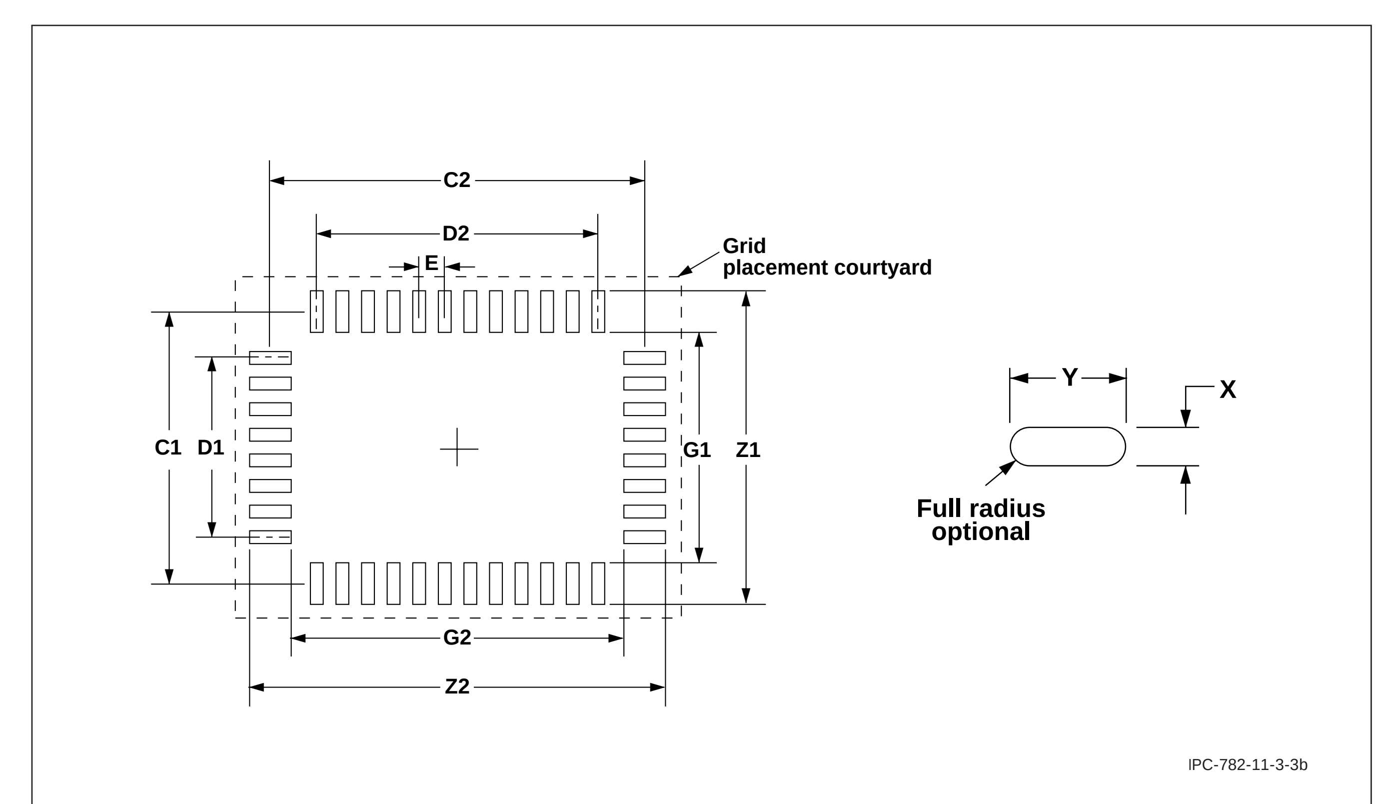
RLP No.	Component Identifier	Z1 (mm)	G1 (mm)	Z2 (mm)	G2 (mm)	X (mm)	Y (mm) ref	C1 (mm) ref	D1 (mm) ref	C2 (mm) ref	D2 (mm) ref	E (mm) ref	Placement Grid (No. of Grid Elements)
680A	SQFP 5x7-32	7.80	4.60	9.80	6.60	0.30	1.60	6.20	2.50	8.20	4.50	0.50	18x22
681A	SQFP 5x7-40	7.80	4.60	9.80	6.60	0.30	1.60	6.20	3.50	8.20	5.50	0.50	18x22
682A	SQFP 5x7-44	7.80	4.60	9.80	6.60	0.25	1.60	6.20	2.80	8.20	5.20	0.40	18x22
683A	SQFP 5x7-52	7.80	4.60	9.80	6.60	0.25	1.60	6.20	3.60	8.20	6.00	0.40	18x22
684A	SQFP 5x7-60	7.80	4.60	9.80	6.60	0.17	1.60	6.20	3.30	8.20	5.10	0.30	18x22
685A	SQFP 5x7-68	7.80	4.60	9.80	6.60	0.17	1.60	6.20	3.90	8.20	5.70	0.30	18x22
690A	SQFP 7x10-52	9.80	6.60	12.80	9.60	0.30	1.60	8.20	4.50	11.20	7.50	0.50	22x28
691A	SQFP 7x10-60	9.80	6.60	12.80	9.60	0.30	1.60	8.20	5.50	11.20	8.50	0.50	22x28
692A	SQFP 7x10-68	9.80	6.60	12.80	9.60	0.25	1.60	8.20	5.20	11.20	7.60	0.40	22x28
693A	SQFP 7x10-76	9.80	6.60	12.80	9.60	0.25	1.60	8.20	6.00	11.20	8.40	0.40	22x28
694A	SQFP 7x10-92	9.80	6.60	12.80	9.60	0.17	1.60	8.20	5.10	11.20	8.10	0.30	22x28
695A	SQFP 7x10-100	9.80	6.60	12.80	9.60	0.17	1.60	8.20	5.70	11.20	8.70	0.30	22x28
700A	SQFP 10x14-80	12.80	9.60	16.80	13.60	0.30	1.60	11.20	7.50	15.20	11.50	0.50	28x36
701A	SQFP 10x14-88	12.80	9.60	16.80	13.60	0.30	1.60	11.20	8.50	15.20	12.50	0.50	28x36
702A	SQFP 10x14-100	12.80	9.60	16.80	13.60	0.25	1.60	11.20	7.60	15.20	11.60	0.40	28x36
703A	SQFP 10x14-108	12.80	9.60	16.80	13.60	0.25	1.60	11.20	8.40	15.20	12.40	0.40	28x36
704A	SQFP 10x14- 140	12.80	9.60	16.80	13.60	0.17	1.60	11.20	8.10	15.20	12.30	0.30	28x36
705A	SQFP 10x14-148	12.80	9.60	16.80	13.60	0.17	1.60	11.20	8.70	15.20	12.90	0.30	28x36

Figure 3a SQFP (Rectangular) land pattern dimensions



Component Identifier	L (mm)		S1 (mm)		L2 (mm)		S2 (mm)		W (mm)		T (mm)		P (mm)	H (mm)	A (mm)	B (mm)	Pin Count, Short Side	Pin Count, Long Side
	min	max	min	max	min	max	min	max	min	max	min	max	basic	max	ref	ref		
QFP-14x20-80	16.95	17.45	14.85	15.55	22.95	23.45	20.85	21.55	0.30	0.45	0.70	1.05	0.80	2.45	14.00	20.00	16	24
QFP-14x20-100	16.95	17.45	14.85	15.55	22.95	23.45	20.85	21.55	0.22	0.38	0.70	1.05	0.65	2.45	14.00	20.00	20	30
SQFP-14x20-120	15.80	16.20	14.20	14.89	21.80	22.20	20.20	20.89	0.10	0.30	0.40	0.80	0.50	2.20	14.00	20.00	24	36
SQFP-14x20-128	15.80	16.20	14.20	14.89	21.80	22.20	20.20	20.89	0.10	0.30	0.40	0.80	0.50	2.20	14.00	20.00	26	38
SQFP-14x20-152	15.80	16.20	14.20	14.89	21.80	22.20	20.20	20.89	0.05	0.22	0.40	0.80	0.40	2.20	14.00	20.00	30	46
SQFP-14x20-160	15.80	16.20	14.20	14.89	21.80	22.20	20.20	20.89	0.05	0.22	0.40	0.80	0.40	2.20	14.00	20.00	32	48
SQFP-14x20-208	15.80	16.20	14.20	14.89	21.80	22.20	20.20	20.89	0.05	0.15	0.40	0.80	0.30	2.20	14.00	20.00	42	62
SQFP-14x20-216	15.80	16.20	14.20	14.89	21.80	22.20	20.20	20.89	0.05	0.15	0.40	0.80	0.30	2.20	14.00	20.00	44	64
SQFP-20x28-176	21.80	22.20	20.20	20.89	29.80	30.20	28.20	28.89	0.10	0.30	0.40	0.80	0.50	3.75	20.00	28.00	36	52
SQFP-20x28-184	21.80	22.20	20.20	20.89	29.80	30.20	28.20	28.89	0.10	0.30	0.40	0.80	0.50	3.75	20.00	28.00	38	54
SQFP-20x28-224	21.80	22.20	20.20	20.89	29.80	30.20	28.20	28.89	0.05	0.22	0.40	0.80	0.40	3.75	20.00	28.00	46	66
SQFP-20x28-232	21.80	22.20	20.20	20.89	29.80	30.20	28.20	28.89	0.05	0.22	0.40	0.80	0.40	3.75	20.00	28.00	48	68
SQFP-20x28-300	21.80	22.20	20.20	20.89	29.80	30.20	28.20	28.89	0.05	0.15	0.40	0.80	0.30	3.75	20.00	28.00	62	88
SQFP-20x28-308	21.80	22.20	20.20	20.89	29.80	30.20	28.20	28.89	0.05	0.15	0.40	0.80	0.30	3.75	20.00	28.00	64	90
SQFP-28x40-256	29.80	30.20	28.20	28.89	41.80	42.20	40.20	40.89	0.10	0.30	0.40	0.80	0.50	4.20	28.00	28.00	52	76
SQFP-28x40-264	29.80	30.20	28.20	28.89	41.80	42.20	40.20	40.89	0.10	0.30	0.40	0.80	0.50	4.20	28.00	40.00	54	78
SQFP-28x40-324	29.80	30.20	28.20	28.89	41.80	42.20	40.20	40.89	0.05	0.22	0.40	0.80	0.40	4.20	28.00	40.00	66	96
SQFP-28x40-332	29.80	30.20	28.20	28.89	41.80	42.20	40.20	40.89	0.05	0.22	0.40	0.80	0.40	4.20	28.00	40.00	68	98
SQFP-28x40-432	29.80	30.20	28.20	28.89	41.80	42.20	40.20	40.89	0.05	0.15	0.40	0.80	0.30	4.20	28.00	40.00	88	128
SQFP-28x40-440	29.80	30.20	28.20	28.89	41.80	42.20	40.20	40.89	0.05	0.15	0.40	0.80	0.30	4.20	28.00	40.00	90	130

Figure 2b SQFP/QFP (Rectangular) component dimensions



RLP No.	Component Identifier	Z1 (mm)	G1 (mm)	Z2 (mm)	G2 (mm)	X (mm)	Y (mm) ref	C1 (mm) ref	D1 (mm) ref	C2 (mm) ref	D2 (mm) ref	E (mm) ref	Placement Grid (No. of Grid Elements)
710A	QFP 14X20-80	18.00	14.40	24.00	20.40	0.50	1.80	16.20	12.00	22.20	18.40	0.80	38x50
711A	QFP 14X20-100	18.00	14.40	24.00	20.40	0.40	1.80	16.20	12.35	22.20	18.85	0.65	38x50
712A	SQFP 14X20-120	16.80	13.60	22.80	19.60	0.30	1.60	15.20	11.50	21.20	17.50	0.50	36x48
713A	SQFP 14X20-128	16.80	13.60	22.80	19.60	0.30	1.60	15.20	12.50	21.20	18.50	0.50	36x48
714A	SQFP 14X20-152	16.80	13.60	22.80	19.60	0.25	1.60	15.20	11.60	21.20	18.00	0.40	36x48
715A	SQFP 14X20-160	16.80	13.60	22.80	19.60	0.25	1.60	15.20	12.40	21.20	18.80	0.40	36x48
716A	SQFP 14X20-208	16.80	13.60	22.80	19.60	0.17	1.60	15.20	12.30	21.20	18.30	0.30	36x48
717A	SQFP 14X20-216	16.80	13.60	22.80	19.60	0.17	1.60	15.20	12.90	21.20	18.90	0.30	36x48
720A	SQFP 20X28-176	22.80	19.60	30.80	27.60	0.30	1.60	21.20	17.50	29.20	25.50	0.50	48x66
721A	SQFP 20X28-184	22.80	19.60	30.80	27.60	0.30	1.60	21.20	18.50	29.20	26.50	0.50	48x66
722A	SQFP 20X28-224	22.80	19.60	30.80	27.60	0.25	1.60	21.20	18.00	29.20	26.00	0.40	48x66
723A	SQFP 20X28-232	22.80	19.60	30.80	27.60	0.25	1.60	21.20	18.80	29.20	26.80	0.40	48x66
724A	SQFP 20X28-300	22.80	19.60	30.80	27.60	0.17	1.60	21.20	18.30	29.20	26.10	0.30	48x66
725A	SQFP 20X28-308	22.80	19.60	30.80	27.60	0.17	1.60	21.20	18.90	29.20	26.70	0.30	48x66
730A	SQFP 28X40-256	30.80	27.60	42.80	39.60	0.30	1.60	29.20	25.50	41.20	37.50	0.50	66x88
731A	SQFP 28X40-264	30.80	27.60	42.80	39.60	0.30	1.60	29.20	26.50	41.20	38.50	0.50	66x88
732A	SQFP 28X40-324	30.80	27.60	42.80	39.60	0.25	1.60	29.20	26.00	41.20	38.00	0.40	66x88
733A	SQFP 28X40-332	30.80	27.60	42.80	39.60	0.25	1.60	29.20	26.80	41.20	38.80	0.40	66x88
734A	SQFP 28X40-432	30.80	27.60	42.80	39.60	0.17	1.60	29.20	26.10	41.20	38.10	0.30	66x88
735A	SQFP 28X40-440	30.80	27.60	42.80	39.60	0.17	1.60	29.20	26.70	41.20	38.70	0.30	66x88

Figure 3b SQFP/QFP (Rectangular) land pattern dimensions

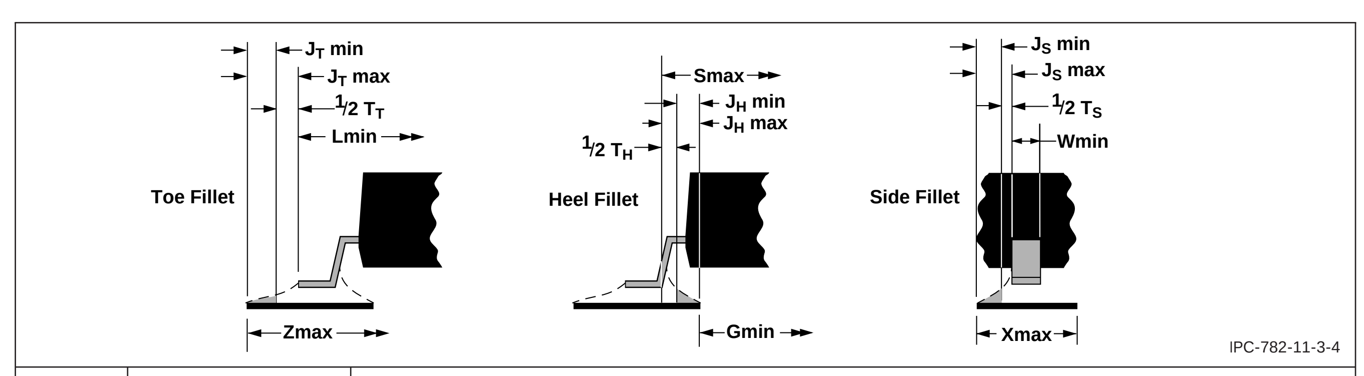
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



	Tolerance Assumptions (mm)		Solder Joint (Sides 1 and 2)								
			Toe (mm)			Heel (mm)			Side (mm)		
RLP No.	F	P	C_L	$J_T$min	$J_T$max	C_S	$J_H$min	$J_H$max	C_W	$J_S$min	$J_S$max
680/681A	0.10	0.10	0.49	0.29	0.50	0.75	0.29	0.65	0.35	-0.02	0.10
682/683A	0.10	0.10	0.49	0.29	0.50	0.75	0.29	0.65	0.33	-0.01	0.10
684/685A	0.10	0.10	0.49	0.29	0.50	0.75	0.29	0.65	0.30	-0.03	0.06
690/691A	0.10	0.10	0.49	0.29	0.50	0.75	0.29	0.65	0.35	-0.02	0.10
692/693A	0.10	0.10	0.49	0.29	0.50	0.75	0.29	0.65	0.33	-0.01	0.10
694/695A	0.10	0.10	0.49	0.29	0.50	0.75	0.29	0.65	0.30	-0.03	0.06
700/701A	0.10	0.10	0.49	0.29	0.50	0.75	0.29	0.65	0.35	-0.02	0.10
702/703A	0.10	0.10	0.49	0.29	0.50	0.75	0.29	0.65	0.33	-0.01	0.10
704/705A	0.10	0.10	0.49	0.29	0.50	0.75	0.29	0.65	0.30	-0.03	0.06
710A	0.10	0.10	0.57	0.27	0.53	0.76	0.22	0.58	0.32	-0.00	0.10
711A	0.10	0.10	0.57	0.27	0.53	0.76	0.22	0.58	0.33	-0.02	0.09
712/713A	0.10	0.10	0.49	0.29	0.50	0.75	0.29	0.65	0.35	-0.02	0.10
714/715A	0.10	0.10	0.49	0.29	0.50	0.75	0.29	0.65	0.33	-0.01	0.10
716/717A	0.10	0.10	0.49	0.29	0.50	0.75	0.29	0.65	0.30	-0.03	0.06
720/721A	0.10	0.10	0.49	0.29	0.50	0.75	0.29	0.65	0.35	-0.02	0.10
722/723A	0.10	0.10	0.49	0.29	0.50	0.75	0.29	0.65	0.33	-0.01	0.10
724/725A	0.10	0.10	0.49	0.29	0.50	0.75	0.29	0.65	0.30	-0.03	0.06
730/731A	0.10	0.10	0.49	0.29	0.50	0.75	0.29	0.65	0.35	-0.02	0.10
732/733A	0.10	0.10	0.49	0.29	0.50	0.75	0.29	0.65	0.33	-0.01	0.10
734/735A	0.10	0.10	0.49	0.29	0.50	0.75	0.29	0.65	0.30	-0.03	0.06

Figure 4 Tolerance and solder joint analysis

1.0 SCOPE

This subsection provides the component and land pattern dimensions for ceramic quad flat pack (CQFP) components. Basic construction of the CQFP device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

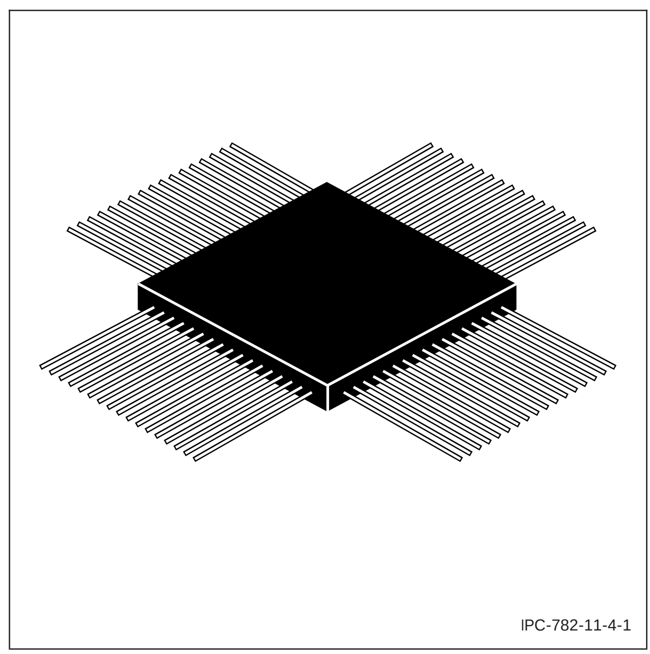
2.0 APPLICABLE DOCUMENTS

JEDEC Publication 95 Registered and Standard Outlines for Solid JEDEC Publication 95 State and Related Products, Outline MS 044

3.0 COMPONENT DESCRIPTIONS

3.1 Basic Construction See Figure 1. Leaded ceramic chip carriers are typically supplied with an open cavity for chip placement. Ceramic or metal lids are soldered, epoxied, or attached with glass frit around the cavity to provide a hermetic seal.

An exception to this construction is the JEDEC standard MS044, which has the chip bonded to a lead frame, which is then sealed between two ceramic bodies with glass frit, similar to CERDIP fabrication. The ceramic packages are available in 28- through 196-lead configurations, with 1.27, 0.80, and 0.64 mm center spacing.



CQFP construction

Pre-leaded ceramic chip carriers typically have copper alloy or Kovar leads that are attached by the manufacturer. Leads are typically bonded to metallization on the top surface of the chip carrier. However, leads can be attached to the package castellations as well. Brazing or thermocompression bonding is usually the attachment means.

Pre-leaded packages using lead-frame construction are also available. These chip carriers have ceramic bodies with two opposing halves which mate above and below a lead frame to which the chip has been previously bonded. The seal is preformed with glass frit.

Leads can be formed to different shapes, such as ‘‘J,’’ ‘‘L,’’ or ‘‘C’’ configurations. Leads bent in the ‘‘L’’ configuration are known as ‘‘gullwings.’’

Pre-leaded chip carriers may be supplied with leads straight and attached to a common strip. The user must detach the common strip and form the leads to the desired configuration. This is done to minimize lead bending during shipping and handling. Leads may be supplied pre-tinned or with gold plating, as is often done for packages intended for a high reliability user.

3.1.1 Termination Materials Leads must be solder-coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the leads by hot dipping or by plating from solution. Plated solder terminations should be subjected to post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in] thick.

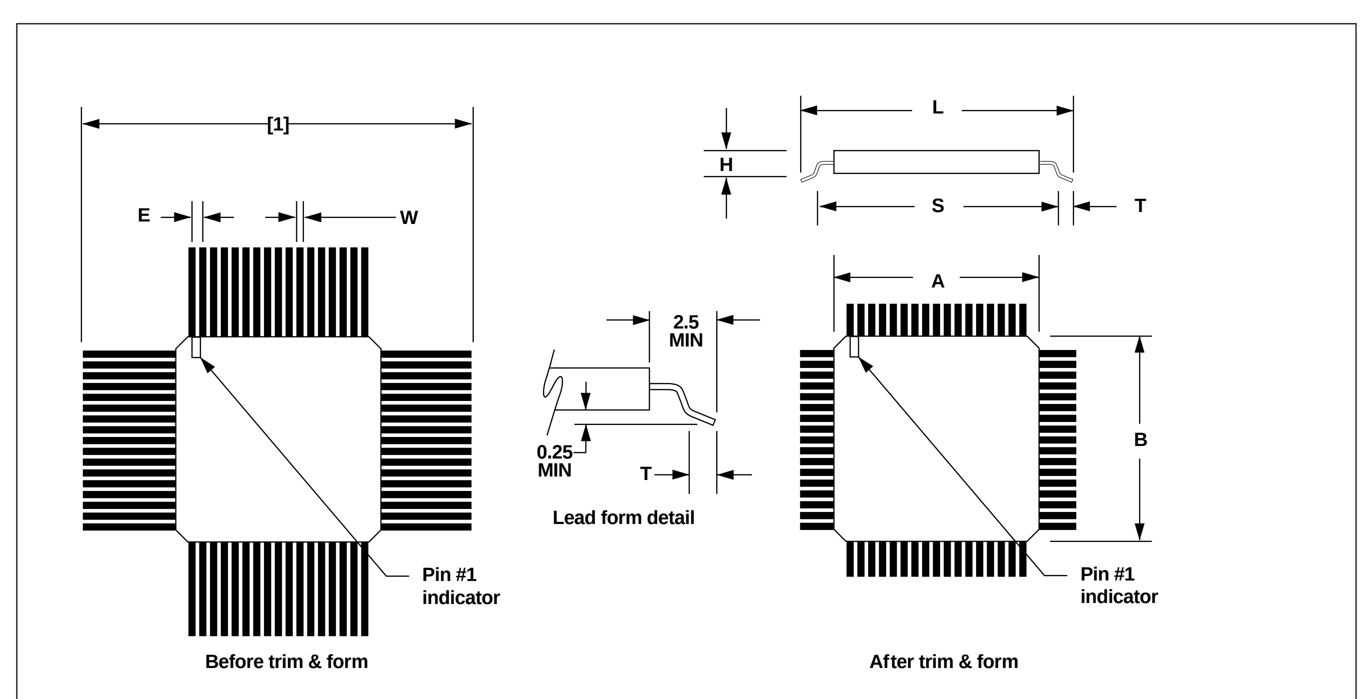
3.1.2 Marking All parts shall be marked with a part number and ‘‘Pin 1’’ location. Pin 1 location may be molded into the plastic body.

3.1.3 Carrier Package Format Tube carriers are preferred for best handling.

3.1.4 Process Considerations CQFPs are usually processed using standard solder reflow processes. Parts should be capable of withstanding ten cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C.

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for CQFP components.



The industry standard for the ceramic quad flat pack device family is not well defined.
The above details represent several configurations considered common but other sizes are available

IPC-782-11-4-2

Component Identifier	L (mm)		S (mm)		W (mm)		T (mm)		A (mm)		B (mm)		H (mm)	P (mm)
	min	max	min	max	min	max	min	max	min	max	min	max	max	basic
CQFP-28	14.40	14.80	11.86	12.39	0.32	0.48	1.02	1.27	9.05	10.05	9.05	10.05	2.30	1.270
CQFP-36	17.15	17.39	14.61	15.04	0.20	0.33	1.02	1.27	11.69	12.70	11.69	12.70	4.92	1.270
CQFP-44	19.69	19.93	17.15	17.58	0.20	0.33	1.02	1.27	14.23	15.24	14.23	15.24	4.92	1.270
CQFP-52	22.23	22.47	19.69	20.12	0.20	0.33	1.02	1.27	16.77	17.78	16.77	17.78	4.92	1.270
CQFP-68	27.31	27.55	24.77	25.20	0.20	0.33	1.02	1.27	21.85	22.86	21.85	22.86	4.92	1.270
CQFP-84	32.39	32.63	29.85	30.28	0.20	0.33	1.02	1.27	26.93	27.94	26.93	27.94	4.92	1.270
CQFP-100	37.47	37.71	34.93	35.36	0.20	0.33	1.02	1.27	32.01	33.02	32.01	33.02	4.92	1.270
CQFP-120	30.95	31.45	28.75	29.50	0.30	0.46	0.70	1.10	26.80	27.30	26.80	27.30	4.06	0.800
CQFP-128	30.95	31.45	28.75	29.50	0.30	0.46	0.70	1.10	26.80	27.30	26.80	27.30	4.06	0.800
CQFP-132	27.28	27.58	25.08	25.72	0.15	0.38	0.70	1.10	23.75	24.38	23.75	24.38	3.55	0.635
CQFP-144	30.95	31.45	28.75	29.50	0.30	0.46	0.70	1.10	26.80	27.30	26.80	27.30	4.06	0.800
CQFP-148	33.50	34.00	30.96	31.57	0.12	0.25	1.02	1.27	28.21	28.71	28.21	28.71	3.10	0.635
CQFP-160	30.95	31.45	28.75	29.50	0.30	0.46	0.70	1.10	26.80	27.30	26.80	27.30	4.06	0.800
CQFP-164	33.50	34.00	30.96	31.57	0.12	0.25	1.02	1.27	28.80	29.30	28.80	29.30	3.35	0.635
CQFP-196	35.75	36.25	33.21	33.82	0.12	0.25	1.02	1.27	33.80	34.30	33.80	34.30	3.45	0.635

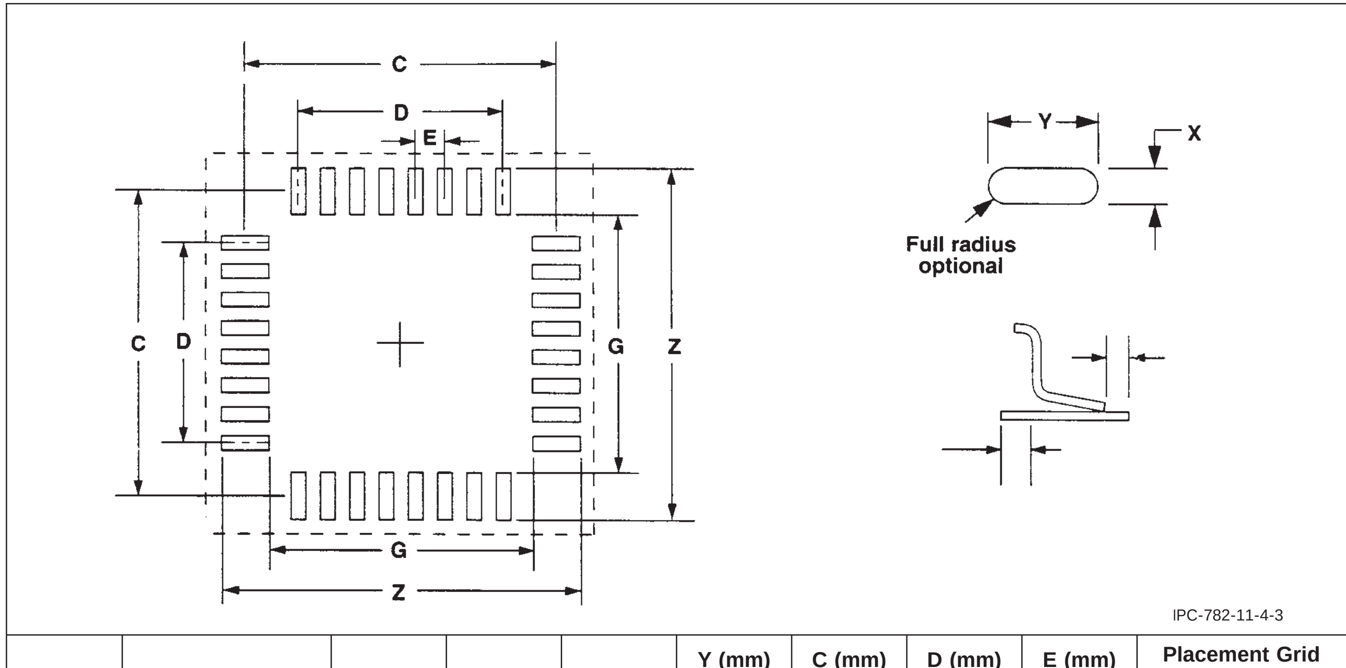
Figure 2 CQFP component dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for CQFP components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



RLP No.	Component Identifier	Z (mm)	G (mm)	X (mm)	Y (mm) ref	C (mm) ref	D (mm) ref	E (mm) ref	Placement Grid (No. of Grid Elements)
750A	CQFP-28	15.80	10.60	0.65	2.60	13.20	7.62	1.27	34x34
751A	CQFP-36	18.60	13.80	0.65	2.40	16.20	10.16	1.27	40x40
752A	CQFP-44	21.00	16.20	0.65	2.40	18.60	12.70	1.27	44x44
753A	CQFP-52	23.60	18.80	0.65	2.40	21.20	15.24	1.27	50x50
754A	CQFP-68	28.60	23.80	0.65	2.40	26.20	20.32	1.27	62x62
755A	CQFP-84	33.80	29.00	0.65	2.40	31.40	25.40	1.27	70x70
756A	CQFP-100	38.80	34.00	0.65	2.40	36.40	30.48	1.27	80x80
757A	CQFP-120	32.40	28.00	0.50	2.20	30.20	23.20	0.80	68x68
758A	CQFP-128	32.40	28.00	0.50	2.20	30.20	24.80	0.80	68x68
759A	CQFP-132	28.60	24.20	0.40	2.20	26.40	20.32	0.64	60x60
760A	CQFP-144	32.40	28.00	0.50	2.20	30.20	24.80	0.80	68x68
761A	CQFP-148	35.20	30.00	0.35	2.60	32.60	22.86	0.64	72x72
762A	CQFP-160	32.40	28.00	0.50	2.20	30.20	24.80	0.80	68x68
763A	CQFP-164	35.20	30.00	0.35	2.60	32.60	25.40	0.64	72x72
764A	CQFP-196	37.20	32.00	0.35	2.60	34.60	30.48	0.64	76x76

Figure 3 CQFP land pattern dimensions

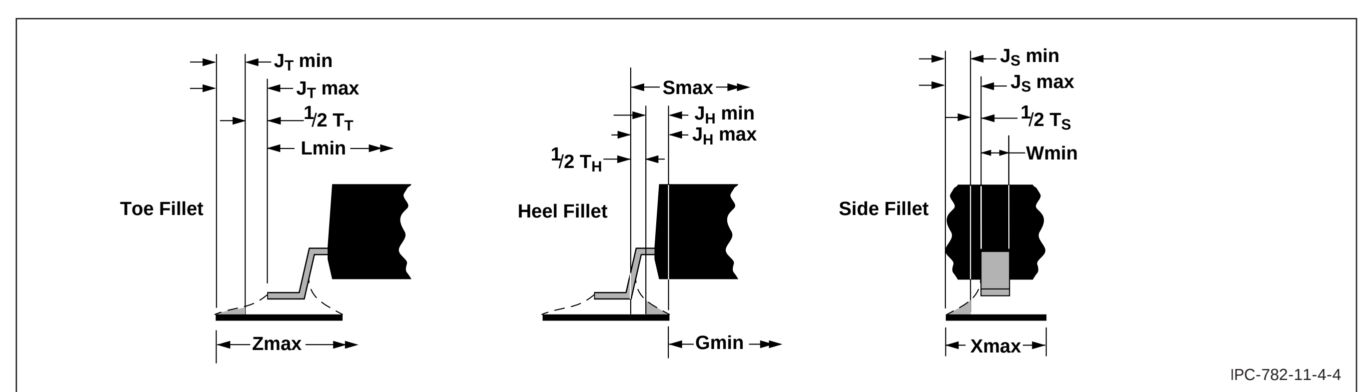
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



RLP No.	Tolerance Assumptions (mm)		Solder Joint								
			Toe (mm)			Heel (mm)			Side (mm)		
	F	P	C_L	$J_T$min	$J_T$max	C_S	$J_H$min	$J_H$max	C_W	$J_S$min	$J_S$max
750A	0.10	0.10	0.40	0.46	0.70	0.53	0.59	0.90	0.16	0.00	0.17
751A	0.10	0.10	0.24	0.54	0.72	0.43	0.36	0.62	0.13	0.07	0.23
752A	0.10	0.10	0.24	0.47	0.65	0.43	0.43	0.69	0.13	0.07	0.23
753A	0.10	0.10	0.24	0.50	0.68	0.43	0.40	0.66	0.13	0.07	0.23
754A	0.10	0.10	0.24	0.46	0.64	0.43	0.44	0.70	0.13	0.07	0.23
755A	0.10	0.10	0.24	0.52	0.70	0.43	0.38	0.64	0.13	0.07	0.23
756A	0.10	0.10	0.24	0.48	0.66	0.43	0.42	0.68	0.13	0.07	0.23
757A	0.10	0.10	0.50	0.47	0.73	0.76	0.37	0.75	0.16	–0.01	0.10
758A	0.10	0.10	0.50	0.47	0.73	0.76	0.37	0.75	0.16	–0.01	0.10
759A	0.10	0.10	0.30	0.49	0.66	0.64	0.43	0.76	0.23	–0.01	0.13
760A	0.10	0.10	0.50	0.47	0.73	0.76	0.37	0.75	0.16	–0.01	0.10
761A	0.10	0.10	0.50	0.59	0.85	0.61	0.47	0.79	0.13	0.02	0.12
762A	0.10	0.10	0.50	0.47	0.73	0.76	0.37	0.75	0.16	–0.01	0.10
763A	0.10	0.10	0.50	0.59	0.85	0.61	0.47	0.79	0.13	0.02	0.12
764A	0.10	0.10	0.50	0.47	0.73	0.61	0.60	0.91	0.13	0.02	0.12

Figure 4 Tolerance and solder joint analysis



IPC-SM-782

Surface Mount Design and Land Pattern Standard

Date	Section
8/93	12.0
Revision	Subject
	Components with J Leads on Four Sides

1.0 INTRODUCTION

This section covers land patterns for components with J leads on four sides. Each subsection contains information in accordance with the following format:

1.0 Scope
2.0 Applicable Documents
3.0 General Component Description (Figure 1)
4.0 Component Dimensions (Figure 2)
5.0 Land Pattern Dimensions (Figure 3)
6.0 Tolerance and Solder Joint Analysis (Figure 4)

The following is the table of contents for this section:

2.0 APPLICABLE DOCUMENTS

The following documents, of the issue in effect on the revision date of this section, form a part of this specification to the extent specified herein.

2.1 Electronic Industries Association (EIA)[1]

EIA-481-A Taping of Surface Mount Components for Automatic Placement

EIA-481-3 32 mm, 44 mm, and 56 mm Embossed Carrier Taping of Surface Mount Components for Automated Handling

JEDEC Publication 95 Registered and Standard Outlines for Solid State and Related Products

2.2 International Electrotechnical Commission (IEC)[2]

IEC 97 Grid Elements

3.0 General Information

3.1 General Component Description Leaded Chip Carriers are either ceramic or plastic packages with terminations which extend beyond the package outlines. These terminations typically space the body of the package from the packaging and interconnect structure for reasons of cleaning, inspecting, or accommodating differences in thermal expansion. The leads may be attached to the package body either before or after chip attachment.

In plastic leaded chip carriers, the primary packaging distinction concerns the point in which a chip is incorporated into the package. A pre-molded package is supplied as a leaded body with an open cavity for chip attachment. A post-molded body part typically has the chip attached to a lead frame with an insulating plastic body molded around the assembly. It is supplied from the manufacturer without apertures.

Leaded ceramic chip carriers may be similarly classified, but with a difference in category. The distinction concerns the point at which leads, if desired, are attached to the ceramic body. A pre-leaded ceramic chip carrier is supplied with copper or Kovar leads brazed to metallization integral with the ceramic package. Typically, the package is supplied with an open cavity for chip attach. A metal or ceramic lid is epoxied, soldered, or attached with glass frit to provide a hermetic seal around the chip. After these steps, the leaded assembly is attached to the printed board.

A post-leaded ceramic chip carrier typically has leads soldered to metallization on the ceramic package after chip attachment. These leads may take the form of edge clips or solder columns. Incorporation of leads into the assembly typically occurs immediately prior to board attachment.

High lead-end coplanarity in surface-mounted lead chip carriers is an important factor in reliable solder attachment to the printed board. Planarity may be measured from the lowest three leads of a leaded package. Coplanarity of 0.1 mm [0.004 in] maximum is recommended with 0.05 mm [0.002 in] preferred.

1. Application for copies should be addressed to Global Engineering Documents, 1990 M St. N.W., Washington, DC 20036.
2. Application for copes should be addressed to IEC, 3 rue de Varembe, PO Box 131 - 1211 Geneva 20, Switzerland

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1.0 SCOPE

This subsection provides the component and land pattern dimensions for plastic leaded chip carriers, square (PLCC components) with J leads on four sides. Basic construction of the PLCC device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

2.0 APPLICABLE DOCUMENTS

See Section 12.0 for documents applicable to the subsections.

2.1 Electronic Industries Association (EIA)

JEDEC Publication 95 Registered and Standard Outlines for Solid State and Related Products, ''Plastic Chip Carrier (PLCC) Family, 1.27 mm [0.050 in] Lead Spacing, Square,'' Outline MO-047, issue ''B,'' dated 11/88

Application for copies should be addressed to:
Global Engineering Documents
1990 M Street N.W.
Washington, DC

3.0 COMPONENT DESCRIPTIONS

Plastic leaded chip carriers are employed where a hermetic seal is not required. Other constraints include limited temperature range (typically 0°C or 70°C) and nominal environmental protection. As with plastic DIPs, they have the advantage of low cost as compared to ceramic packages.

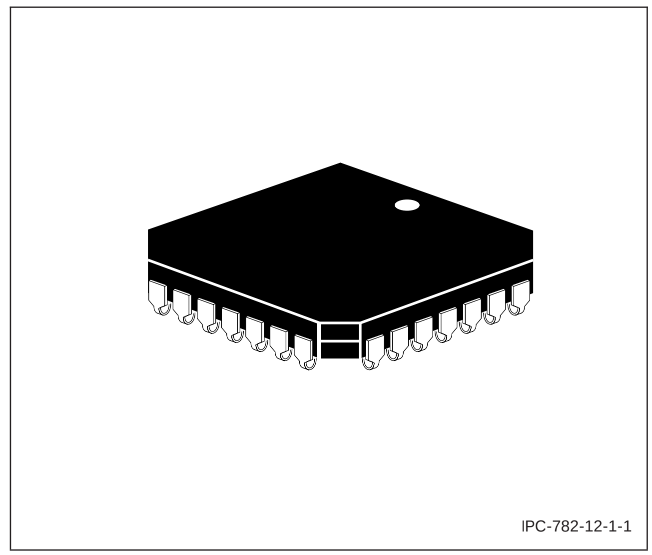


Figure 1 PLCC (Square)

3.1.1 Pre-molded Plastic Chip Carriers The pre-molded plastic chip carrier was designed to be connected to the P&I substrate by means of a socket. Spring pressure on both sides of the package is intended to constrain movement as well as allow for substrate warpage as high as 0.5%. Solder attach to the P&I substrate is also possible. The design is also intended to make use of silicone encapsulant technology for chip coverage and protection.

3.1.2 Post-molded Plastic Chip Carriers The post-molded plastic leaded chip carrier is composed of a composite metal/dielectric assembly that includes a conductor lead frame and a molded insulating body. Compared to the pre-molded package which has an aperture for mounting micro-electronic components, the post-molded package comes complete with no apertures. In both types of plastic chip carriers, all necessary plating operations are performed by the package manufacturer to eliminate tinning or plating by the user.

The Joint Device Engineering Council (JEDEC) defines the Type A Leaded Chip Carrier as a plastic package with leads wrapped down and around the body on all four sides. This package can be either directly mounted to a printed wiring board or used with a socket. It is available with 28, 44, 52, 68, 84, 100, or 124 leads. This family is based on 1.27 mm [0.050 in] lead pitch. The original mechanical outline drawing of this package was defined based on a premolded package. However, actual construction is not specified and the package could be of post-molded construction.

Post-molded packages which have J-lead configuration and are JEDC standard MO-047, are available in 20-, 28-, 44-, 52-, 68-, 84-, 100- and 124-lead counts with the same spacing.

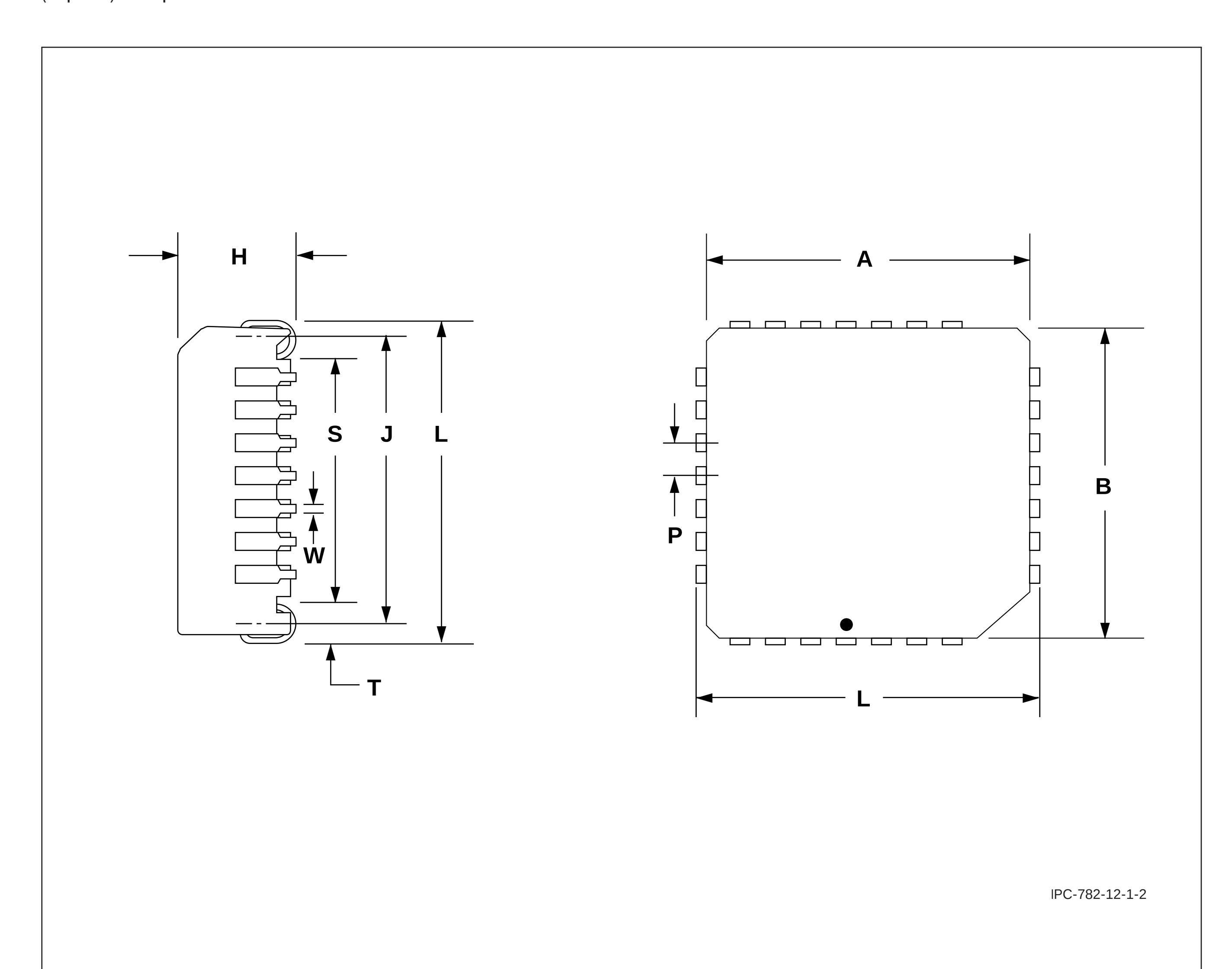
3.1.3 Marking All parts shall be marked with a part number and ''Pin 1'' location. ''Pin 1'' location may be molded into the plastic body.

3.1.4 Carrier Package Format Bulk rods, 24 mm tape/ 8–12 mm pitch is preferred for best handling. Tube carriers are also used.

3.1.5 Resistance to Soldering Parts should be capable of withstanding ten cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260°C.

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for PLCC (Square) components.



Component Identifier	L (mm)		S (mm)		W (mm)		T (mm)		A (mm)		B (mm)		J (mm)	H (mm)	P (mm)
	min	max	min	max	min	max	min	max	min	max	min	max	ref	max	basic
PLCC-20	9.78	10.03	5.78	6.53	0.33	0.53	1.50	2.00	8.89	9.04	8.89	9.04	7.87	4.57	1.27
PLCC-28	12.32	12.57	8.32	9.07	0.33	0.53	1.50	2.00	11.43	11.58	11.43	11.58	10.41	4.57	1.27
PLCC-44	17.40	17.65	13.40	14.15	0.33	0.53	1.50	2.00	16.51	16.66	16.51	16.66	15.49	4.57	1.27
PLCC-52	19.94	20.19	15.94	16.69	0.33	0.53	1.50	2.00	19.05	19.20	19.05	19.20	18.03	5.08	1.27
PLCC-68	25.02	25.27	21.02	21.77	0.33	0.53	1.50	2.00	24.13	24.33	24.13	24.33	23.11	5.08	1.27
PLCC-84	30.10	30.35	26.10	26.85	0.33	0.53	1.50	2.00	29.21	29.41	29.21	29.41	28.19	5.08	1.27
PLCC-100	35.18	35.43	31.18	31.93	0.33	0.53	1.50	2.00	34.29	34.49	34.29	34.49	33.27	5.08	1.27
PLCC-124	42.80	43.05	38.80	39.55	0.33	0.53	1.50	2.00	41.91	42.11	41.91	42.11	40.89	5.08	1.27

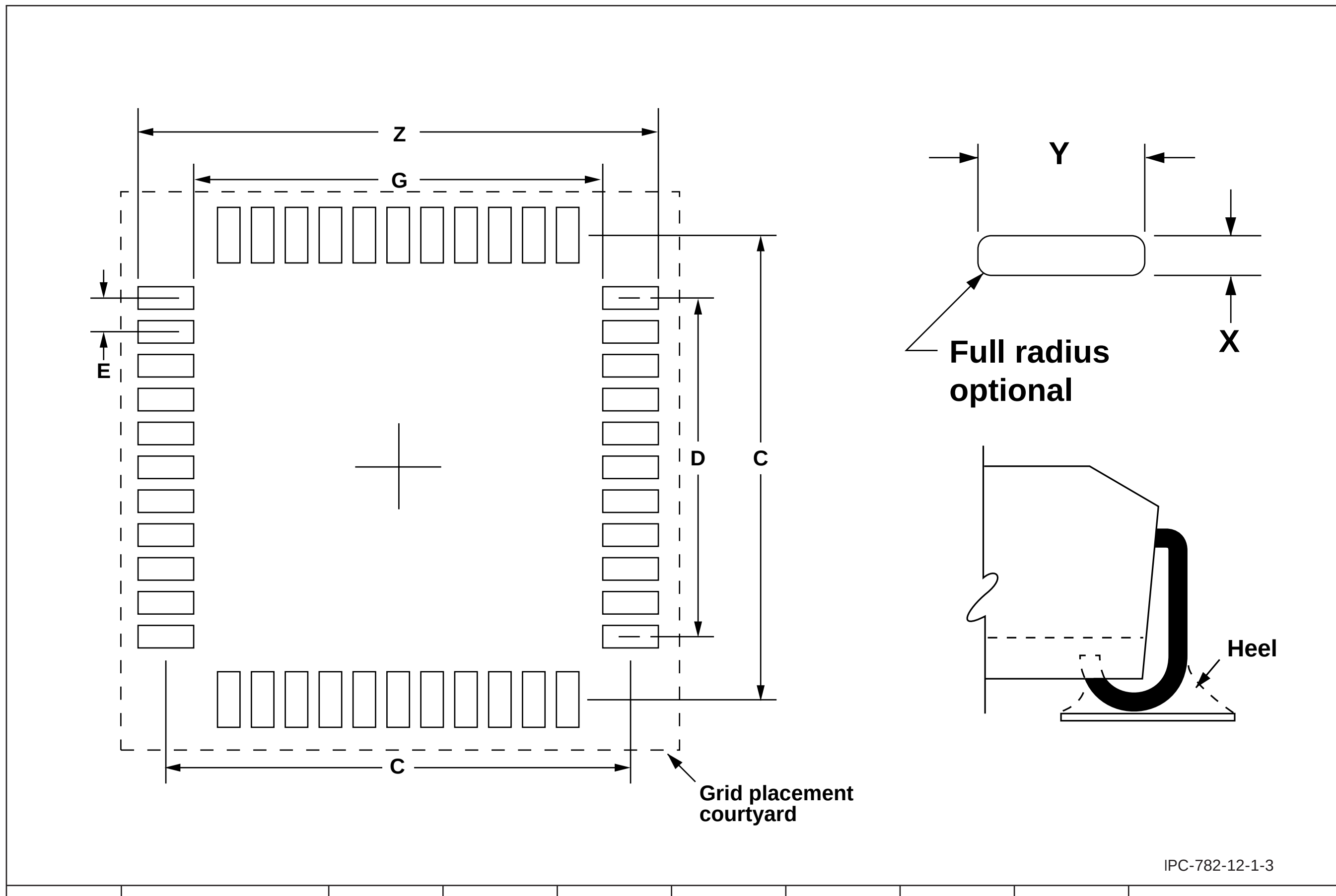
Figure 2 PLCC (Square)

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for PLCC (Square) components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



RLP No.	Component Identifier	Z (mm)	G (mm)	X (mm)	Y (mm) ref	C (mm) ref	D (mm) ref	E (mm) ref	Placement Grid (No. of Grid Elements)
790A	PLCC-20	10.80	6.40	0.60	2.20	8.60	5.08	1.27	24x24
791A	PLCC-28	13.40	9.00	0.60	2.20	11.20	7.62	1.27	30x30
792A	PLCC-44	18.40	14.00	0.60	2.20	16.20	12.70	1.27	40x40
793A	PLCC-52	21.00	16.60	0.60	2.20	18.80	15.24	1.27	44x44
794A	PLCC-68	26.00	21.60	0.60	2.20	23.80	20.32	1.27	54x54
795A	PLCC-84	31.20	26.80	0.60	2.20	29.00	25.40	1.27	66x66
796A	PLCC-100	36.20	31.80	0.60	2.20	34.00	30.48	1.27	76x76
797A	PLCC-124	43.80	39.40	0.60	2.20	41.60	38.10	1.27	90x90

Figure 3 PLCC (Square) land pattern dimensions

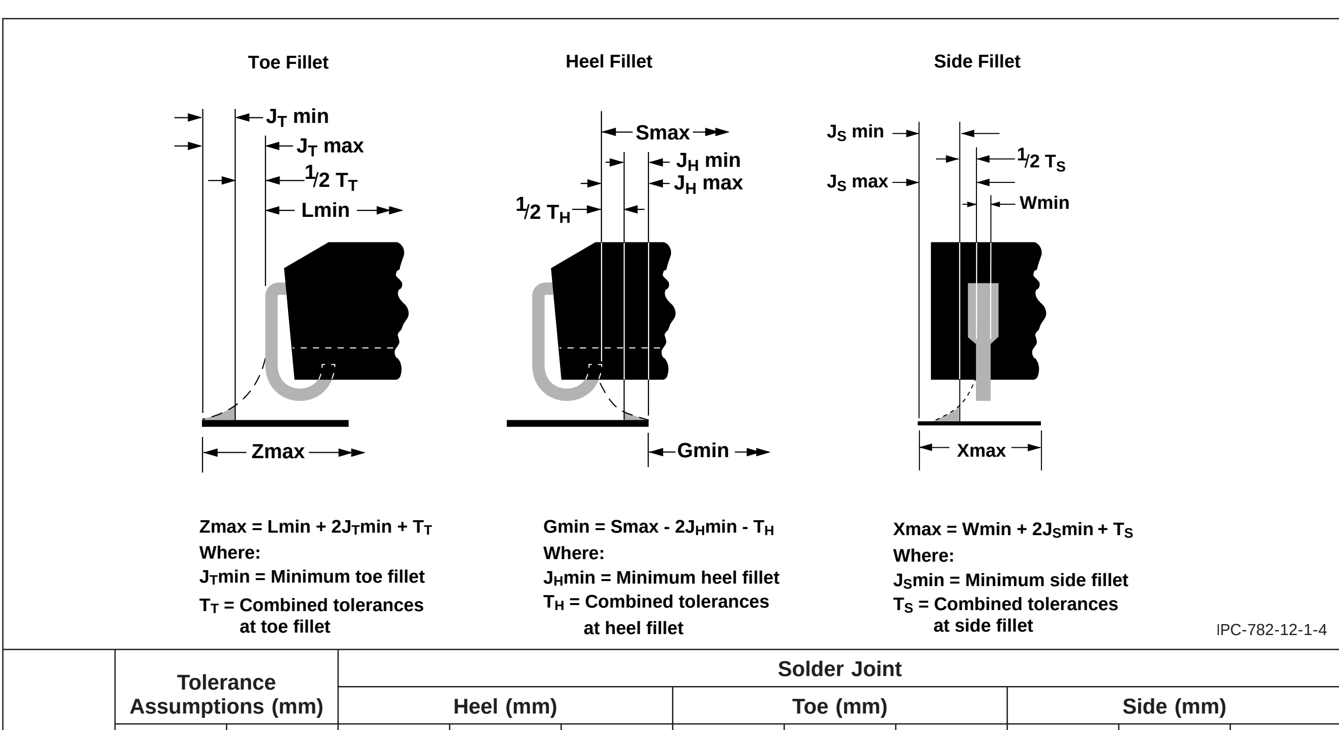
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be asgiven in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



RLP No.	Tolerance Assumptions (mm)		Solder Joint								
			Heel (mm)			Toe (mm)			Side (mm)		
	F	P	C_L	$J_H$min	$J_H$max	C_S	$J_T$min	$J_T$max	C_W	$J_S$min	$J_S$max
790A	0.10	0.10	0.25	0.37	0.51	0.75	-0.32	0.06	0.20	0.01	0.14
791A	0.10	0.10	0.25	0.40	0.54	0.75	-0.35	0.04	0.20	0.01	0.14
792A	0.10	0.10	0.25	0.36	0.50	0.75	-0.31	0.07	0.20	0.01	0.14
793A	0.10	0.10	0.25	0.39	0.53	0.75	-0.34	0.04	0.20	0.01	0.14
794A	0.10	0.10	0.25	0.35	0.49	0.75	-0.30	0.08	0.20	0.01	0.14
795A	0.10	0.10	0.25	0.41	0.55	0.75	-0.36	0.03	0.20	0.01	0.14
796A	0.10	0.10	0.25	0.37	0.51	0.75	-0.32	0.06	0.20	0.01	0.14
797A	0.10	0.10	0.25	0.36	0.50	0.75	-0.31	0.07	0.20	0.01	0.14

Figure 4 Tolerance and solder joint analysis



IPC-SM-782

Surface Mount Design and Land Pattern Standard

Date	Section
5/96	12.2
Revision	Subject
A	PLCC (Rectangular)

1.0 SCOPE

This subsection provides the component and land pattern dimensions for plastic leaded chip carriers, rectangular (PLCC components) with J leads on four sides. Basic construction of the PLCC device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

2.0 APPLICABLE DOCUMENTS

See Section 12.0 for documents applicable to the subsections.

2.1 Electronic Industries Association (EIA)

JEDEC Publication 95 Registered and Standard Outlines for Solid State and Related Products, ''Plastic Chip Carrier (PLCC) Family, 1.27 mm [0.050 in] Lead Spacing, Square,'' Outline MO-052, issue ''B,'' dated 8/85

Application for copies should be addressed to:
Global Engineering Documents
1990 M Street N.W.
Washington, DC

3.0 COMPONENT DESCRIPTIONS

Plastic leaded chip carriers are employed where a hermetic seal is not required. Other constraints include limited temperature range (typically 0°C or 70°C) and nominal environmental protection. As with plastic DIPs, they have the advantage of low cost as compared to ceramic packages.

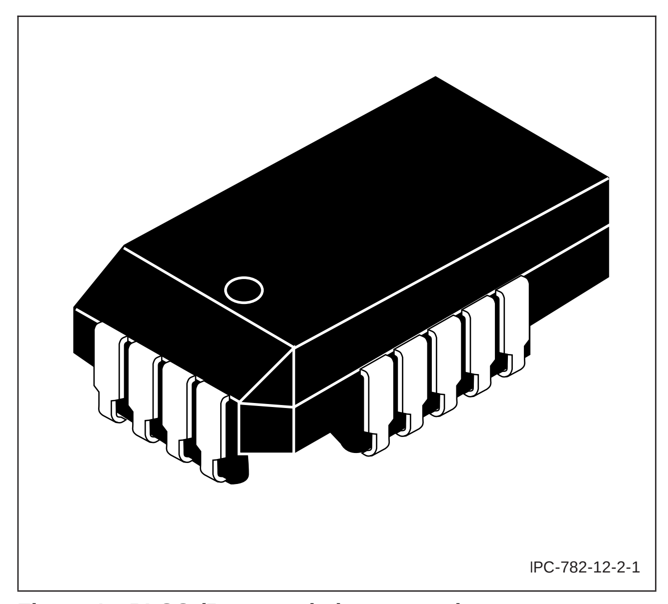


Figure 1 PLCC (Rectangular) construction

3.1.1 Pre-molded Plastic Chip Carriers The pre-molded plastic chip carrier was designed to be connected to the P&I substrate by means of a socket. Spring pressure on both sides of the package is intended to constrain movement as well as allow for substrate warpage as high as 0.5%. Solder attach to the P&I substrate is also possible. The design is also intended to mae use of silicone encapsulant technology for chip coverage and protection.

3.1.2 Post-molded Plastic Chip Carriers The post-molded plastic leaded chip carrier is composed of a composite metal/dielectric assembly that includes a conductor lead frame and a molded insulating body. Compared to the pre-molded package which has an aperture for mounting microelectronic components, the post-molded package comes complete with no apertures. In both types of plastic chip carriers, all necessary plating operations are performed by the package manufacturer to eliminate tinning or plating by the user.

The Joint Device Engineering Council (JEDEC) defines the Type A Leaded Chip Carrier as a plastic package with leads wrapped down and around the body on all four sides. This package can be either directly mounted to a printed wiring board or used with a socket. It is available with 28, 44, 52, 68, 84, 100, or 124 leads. This family is based on 1.27 mm [0.050 in] lead pitch. The original mechanical outline drawing of this package was defined based on a premolded package. However, actual construction is not specified and the package could be of post-molded construction.

Post-molded packages which have J-lead configuration and are JEDC standard MO-052, are available in 20-, 28-, 44-, 52-, 68-, 84-, 100- and 124-lead counts with the same spacing.

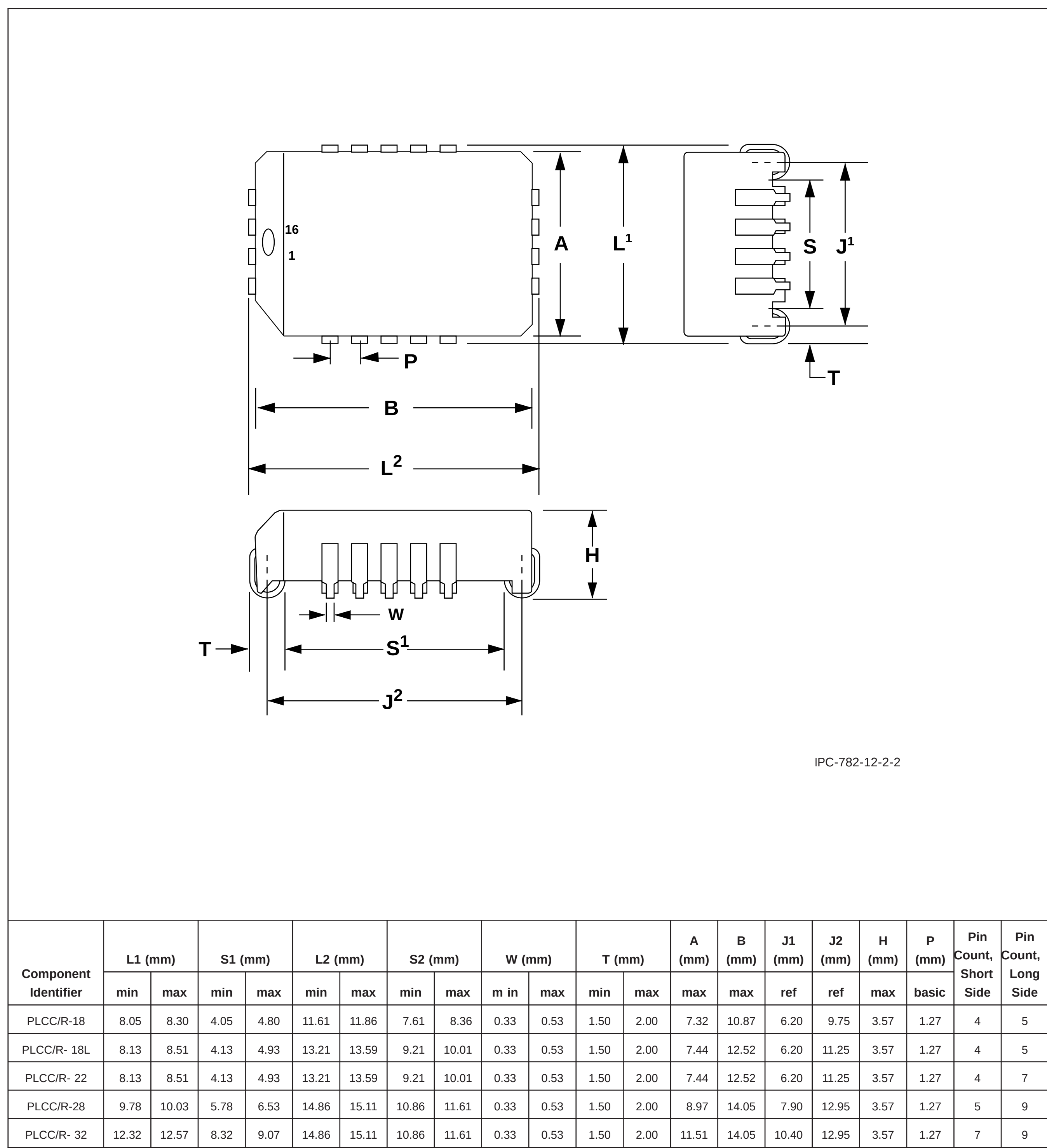
3.1.3 Marking All parts shall be marked with a part number and ''Pin 1'' location. ''Pin 1'' location may be molded into the plastic body.

3.1.4 Carrier Package Format Bulk rods, 24 mm tape/ 8–12 mm pitch is preferred for best handling. Tube carriers are also used.

3.1.5 Resistance to Soldering Parts should be capable of withstanding ten cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C. Parts must also be capable of withstanding a minimum of 10 seconds immersion in molten solder at 260°C.

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for PLCC (Rectangular) components.



Component Identifier	L1 (mm)		S1 (mm)		L2 (mm)		S2 (mm)		W (mm)		T (mm)		A (mm)	B (mm)	J1 (mm)	J2 (mm)	H (mm)	P (mm)	Pin Count, Short Side	Pin Count, Long Side
	min	max	min	max	min	max	min	max	m in	max	min	max	max	max	ref	ref	max	basic		
PLCC/R-18	8.05	8.30	4.05	4.80	11.61	11.86	7.61	8.36	0.33	0.53	1.50	2.00	7.32	10.87	6.20	9.75	3.57	1.27	4	5
PLCC/R- 18L	8.13	8.51	4.13	4.93	13.21	13.59	9.21	10.01	0.33	0.53	1.50	2.00	7.44	12.52	6.20	11.25	3.57	1.27	4	5
PLCC/R- 22	8.13	8.51	4.13	4.93	13.21	13.59	9.21	10.01	0.33	0.53	1.50	2.00	7.44	12.52	6.20	11.25	3.57	1.27	4	7
PLCC/R-28	9.78	10.03	5.78	6.53	14.86	15.11	10.86	11.61	0.33	0.53	1.50	2.00	8.97	14.05	7.90	12.95	3.57	1.27	5	9
PLCC/R- 32	12.32	12.57	8.32	9.07	14.86	15.11	10.86	11.61	0.33	0.53	1.50	2.00	11.51	14.05	10.40	12.95	3.57	1.27	7	9

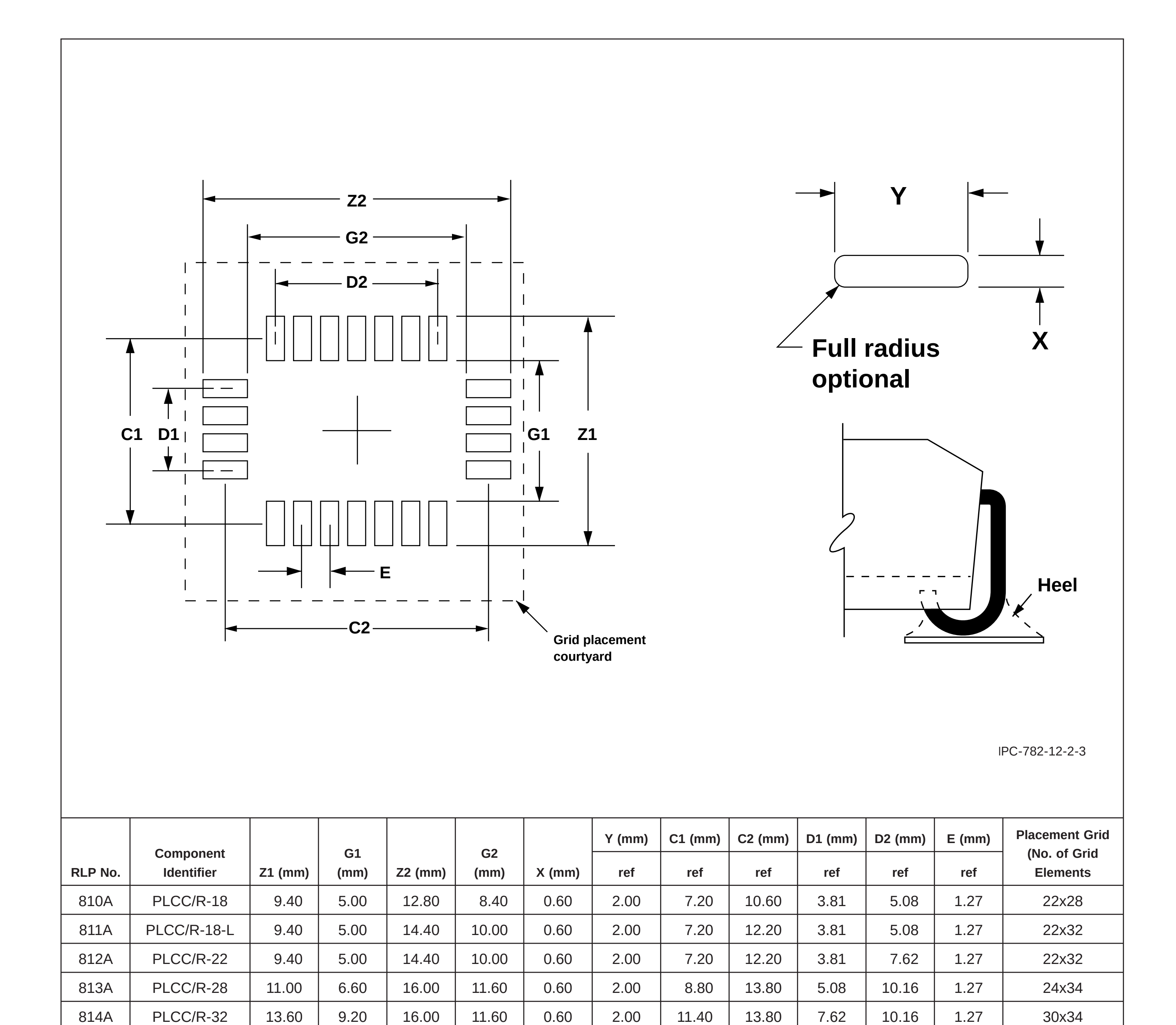
Figure 2 PLCC (Rectangular) component dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for PLCC (Rectangular) components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



RLP No.	Component Identifier	Z1 (mm)	G1 (mm)	Z2 (mm)	G2 (mm)	X (mm)	Y (mm) ref	C1 (mm) ref	C2 (mm) ref	D1 (mm) ref	D2 (mm) ref	E (mm) ref	Placement Grid (No. of Grid Elements)
810A	PLCC/R-18	9.40	5.00	12.80	8.40	0.60	2.00	7.20	10.60	3.81	5.08	1.27	22x28
811A	PLCC/R-18-L	9.40	5.00	14.40	10.00	0.60	2.00	7.20	12.20	3.81	5.08	1.27	22x32
812A	PLCC/R-22	9.40	5.00	14.40	10.00	0.60	2.00	7.20	12.20	3.81	7.62	1.27	22x32
813A	PLCC/R-28	11.00	6.60	16.00	11.60	0.60	2.00	8.80	13.80	5.08	10.16	1.27	24x34
814A	PLCC/R-32	13.60	9.20	16.00	11.60	0.60	2.00	11.40	13.80	7.62	10.16	1.27	30x34

Figure 3 PLCC (Rectangular) land pattern dimensions

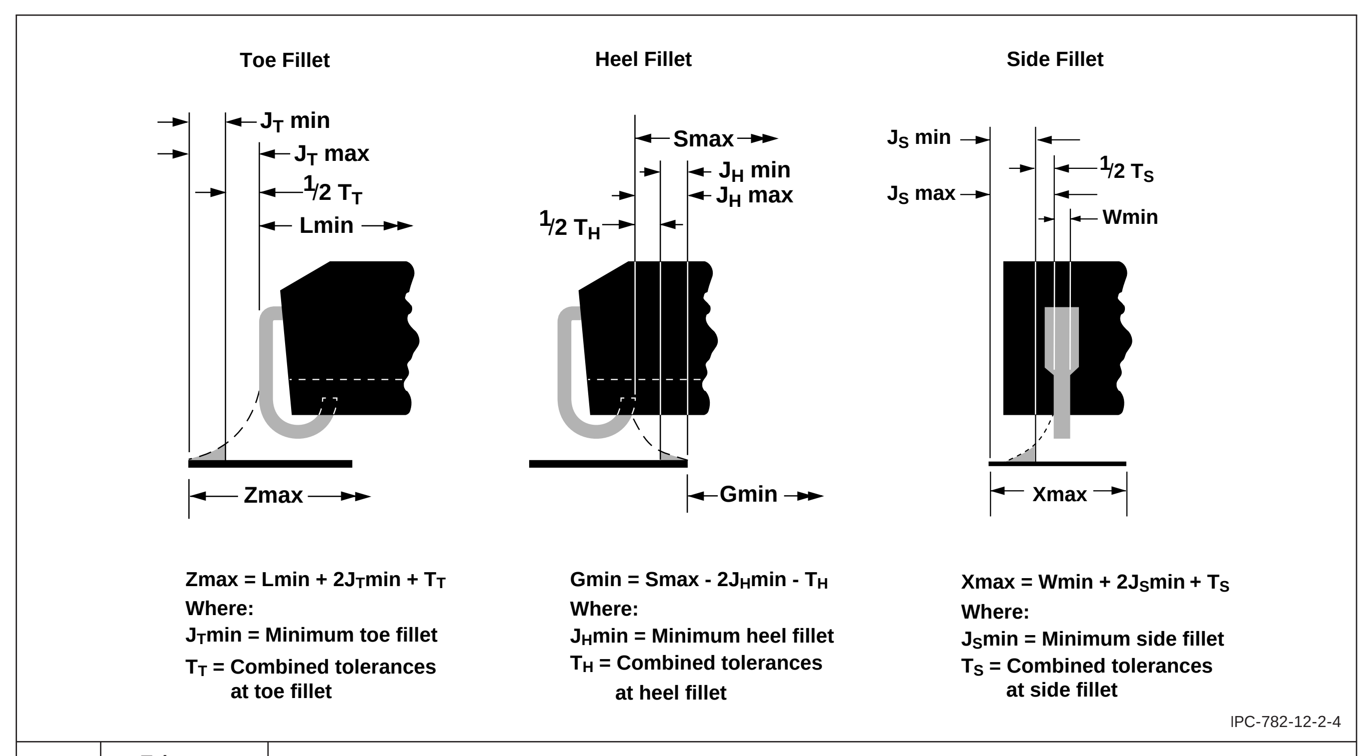
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be asgiven in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



RLP No.	Tolerance Assumptions (mm)		Solder Joint													
			Heel 1 and 2 (mm)					Toe 1 and 2 (mm)					Side 1 and 2 (mm)		
	F	P	C_L	J_{H1}min	J_{H1}max	J_{H2}min	J_{H2}max	C_S	J_{T1}min	J_{T1}max	J_{T2}min	J_{T2}max	C_W	$J_S$min	$J_S$max
810A	0.10	0.10	0.25	0.53	0.67	0.45	0.60	0.75	–0.48	–0.10	–0.40	–0.02	0.20	0.01	0.14
811A	0.10	0.10	0.38	0.43	0.64	0.39	0.60	0.80	–0.44	–0.03	–0.40	0.01	0.20	0.01	0.14
812A	0.10	0.10	0.38	0.43	0.64	0.39	0.60	0.80	–0.44	–0.03	–0.40	0.01	0.20	0.01	0.14
813A	0.10	0.10	0.25	0.47	0.61	0.43	0.57	0.75	–0.42	–0.04	–0.38	0.00	0.20	0.01	0.14
814A	0.10	0.10	0.25	0.50	0.64	0.43	0.57	0.75	–0.45	–0.06	–0.38	0.00	0.20	0.01	0.14

Figure 4 Tolerance and solder joint analysis



IPC-SM-782

Surface Mount Design and Land Pattern Standard

Date	Section
8/93	12.3
Revision	Subject
	LCC

1.0 SCOPE

This subsection provides the component and land pattern dimensions for leadless ceramic chip carriers (LCC components). Basic construction of the LCC device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

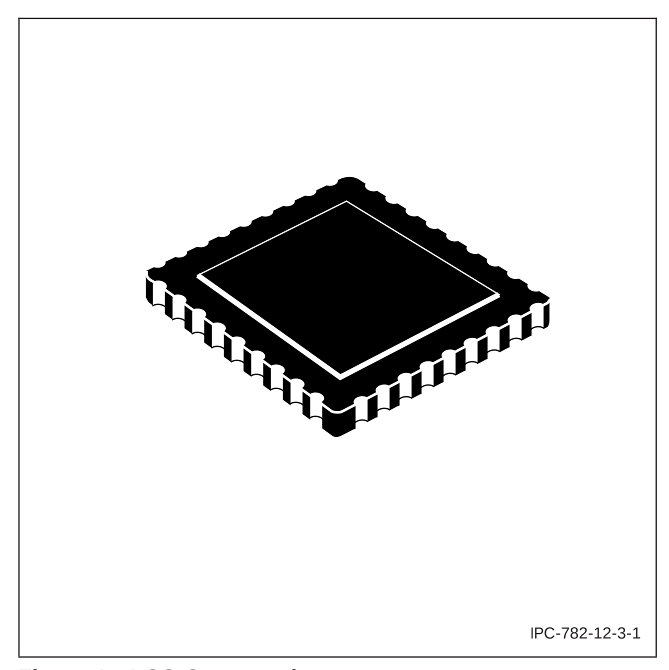
2.0 APPLICABLE DOCUMENTS

See Section 12.0 and the following for documents applicable to this subsection.

2.1 Electronic Industries Association (EIA)

JEDEC Publication 95

Registered and Standard Outlines for Solid JEDEC Publication 95 State and Related Products, ''0.050 In. Center, Leadless Type A,'' Outline MS002, issue ''A,'' dated 9/29/80, and ''0.050 In. Center, Leadless Type C,'' Outline MS004, issue ''B,'' dated 5/90



IPC-782-12-3-1

Figure 1 LCC Construction

3.0 Component Descriptions

3.1 Basic Construction A leadless chip carrier is a ceramic package with integral surface-metallized terminations. Leadless Types A, B, and D chip carriers have a chamfered index corner that is larger than that of Type C. Another difference between the A, B, and D types and Type C is the feature in the other three corners. The types A, B, and D, were designed for socket applications and printed wiring interconnections. The Type C is primarily intended for direct attachment through reflow soldering. This application difference is the main reason for their mechanical differences. These packages mount in different orientations, depending on type, mounting structure and preferred thermal orientation.

Leadless Type A is intended for lid-down mounting in a socket, which places the primary heat-dissipating surface away from the mounting surface for more effective cooling in air-cooled systems.

Type C is a ceramic package similar to leadless Type B except for corner configuration. The 50 mil center family, which includes both leadless and leaded devices, is designed to mount on a common mounting pattern. They may be directly attached to the mounting structure, or can be plugged into sockets. One basic restriction is that there shall be no terminals in the corners of the package. There are a number of common sizes.

3.1.1 Termination Materials Leads must be solder-coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the leads by hot dipping or by plating from solution. Plated solder terminations should be subjected to post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.0075 mm [0.0003 in.] thick.

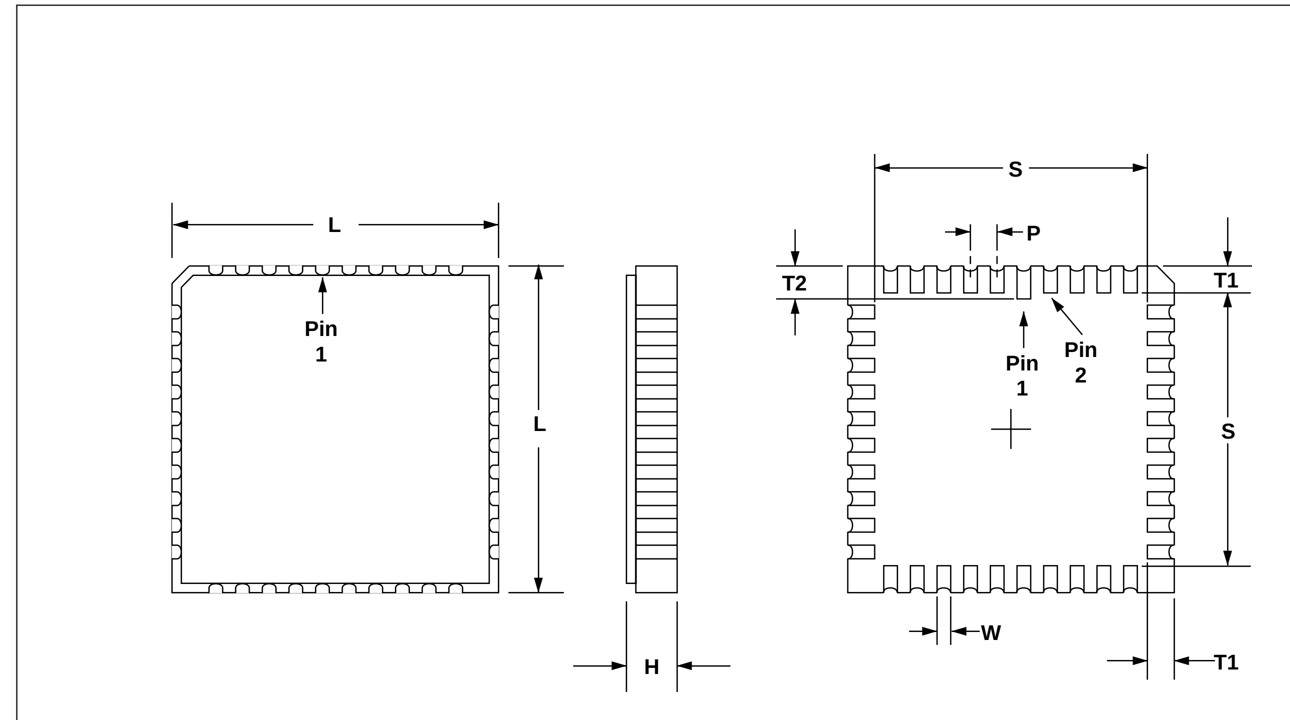
3.1.2 Marking All parts shall be marked with a part number and ''Pin 1'' location. Pin 1 location may be molded into the plastic body.

3.1.3 Carrier Package Format Tube carriers are preferred for best handling.

3.1.4 Process Considerations LCCs are usually processed using standard solder reflow processes. Parts should be capable of withstanding ten cycles through a standard reflow system operating at 215°C. Each cycle shall consist of 60 seconds exposure at 215°C.

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for LCC components.



Note: Component body Widths normally described as "A" & "B" on other components are equal to "L".

IPC-782-12-3-2

Component Identifier	Type	L (mm)		S (mm)		W (mm)		T1 (mm)		T2 (mm)		H (mm)	P (mm)
		min	max	min	max	min	max	min	max	m in	max	max	basic
LCC-16	Type C	7.42	7.82	4.64	5.16	0.56	1.04	1.15	1.39	1.96	2.36	2.54	1.27
LCC-20	Type C	8.69	9.09	5.91	6.43	0.56	1.04	1.15	1.39	1.96	2.36	2.54	1.27
LCC-24	Type C	10.04	10.41	7.26	7.76	0.56	1.04	1.15	1.39	1.96	2.36	2.54	1.27
LCC-28	Type C	11.23	11.63	8.45	8.97	0.56	1.04	1.15	1.39	1.96	2.36	2.54	1.27
LCC-44	Type C	16.26	16.76	13.48	14.08	0.56	1.04	1.15	1.39	1.96	2.36	3.04	1.27
LCC-52	Type C	18.78	19.32	16.00	16.64	0.56	1.04	1.15	1.39	1.96	2.36	3.04	1.27
LCC-68	Type C	23.83	24.43	21.05	21.74	0.56	1.04	1.15	1.39	1.96	2.36	3.04	1.27
LCC-84	Type C	28.83	29.59	26.05	26.88	0.56	1.04	1.15	1.39	1.96	2.36	3.04	1.27
LCC-100	Type A	34.02	34.56	31.24	31.88	0.56	1.04	1.15	1.39	1.96	2.36	4.06	1.27
LCC-124	Type A	41.64	42.18	38.86	39.50	0.56	1.04	1.15	1.39	1.96	2.36	4.06	1.27
LCC-156	Type A	51.80	52.34	49.02	49.66	0.56	1.04	1.15	1.39	1.96	2.36	4.06	1.27

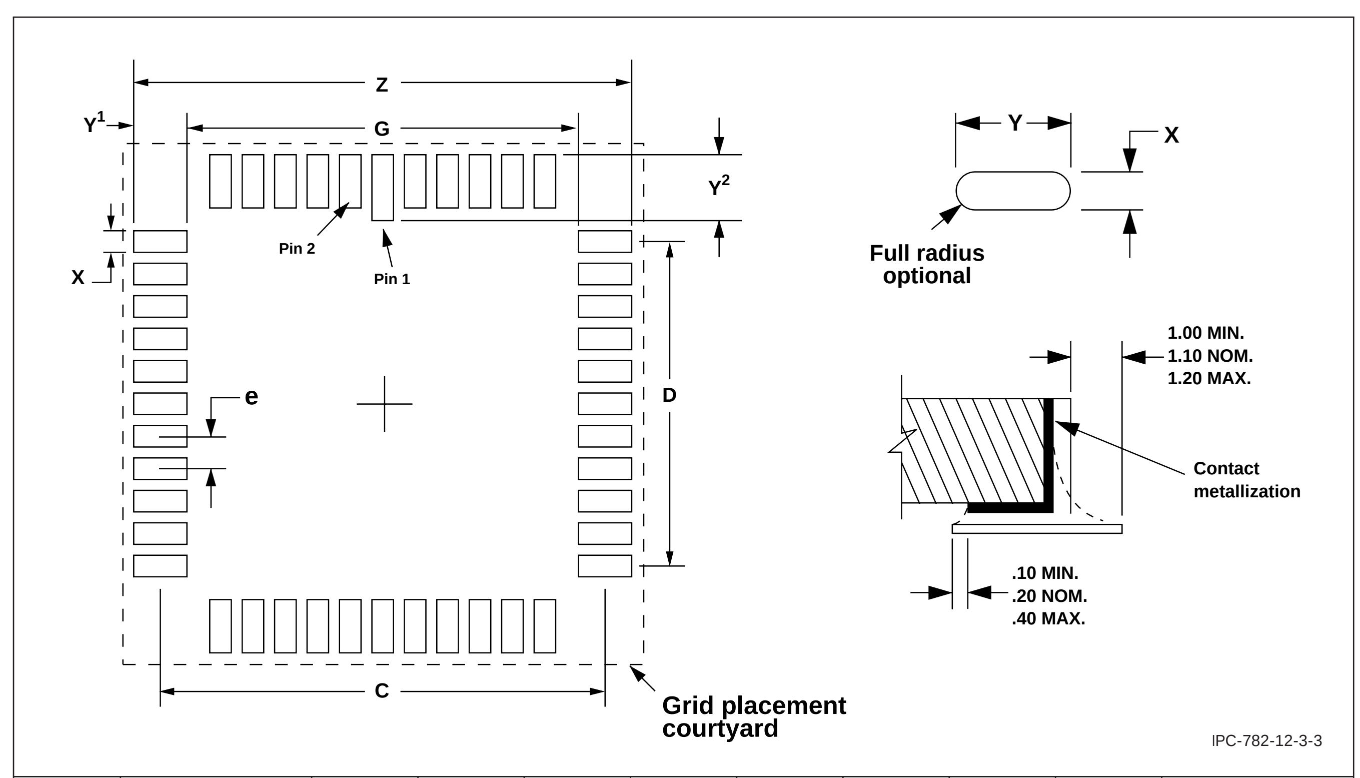
Figure 2 LCC component dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for LCC components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



RLP No.	Component Identifier	Z (mm)	G (mm)	X (mm)	Y1 (mm) ref	Y2 (mm) ref	C (mm) ref	D (mm) ref	E (mm) ref	Placement Grid (No. of Grid Elements)
830	LCC-16	9.80	4.60	0.80	2.60	3.40	7.20	3.81	1.27	22X22
831	LCC-20	11.00	5.80	0.80	2.60	3.40	8.40	5.08	1.27	24X24
832	LCC-24	12.40	7.20	0.80	2.60	3.40	9.80	6.35	1.27	26X26
833	LCC-28	13.60	8.40	0.80	2.60	3.40	11.00	7.62	1.27	30X30
834	LCC-44	18.80	13.60	0.80	2.60	3.40	16.20	12.70	1.27	40X40
835	LCC-52	21.20	16.00	0.80	2.60	3.40	18.60	15.24	1.27	44X44
836	LCC-68	26.20	21.00	0.80	2.60	3.40	23.60	20.32	1.27	54X54
837	LCC-84	31.40	26.20	0.80	2.60	3.40	28.80	25.40	1.27	64X64
838	LCC-100	36.40	31.20	0.80	2.60	3.40	33.80	30.48	1.27	74X74
839	LCC-124	44.20	39.00	0.80	2.60	3.40	41.60	38.10	1.27	90X90
840	LCC-156	54.20	49.00	0.80	2.60	3.40	51.60	48.26	1.27	110X110

Figure 3 LCC land pattern dimensions

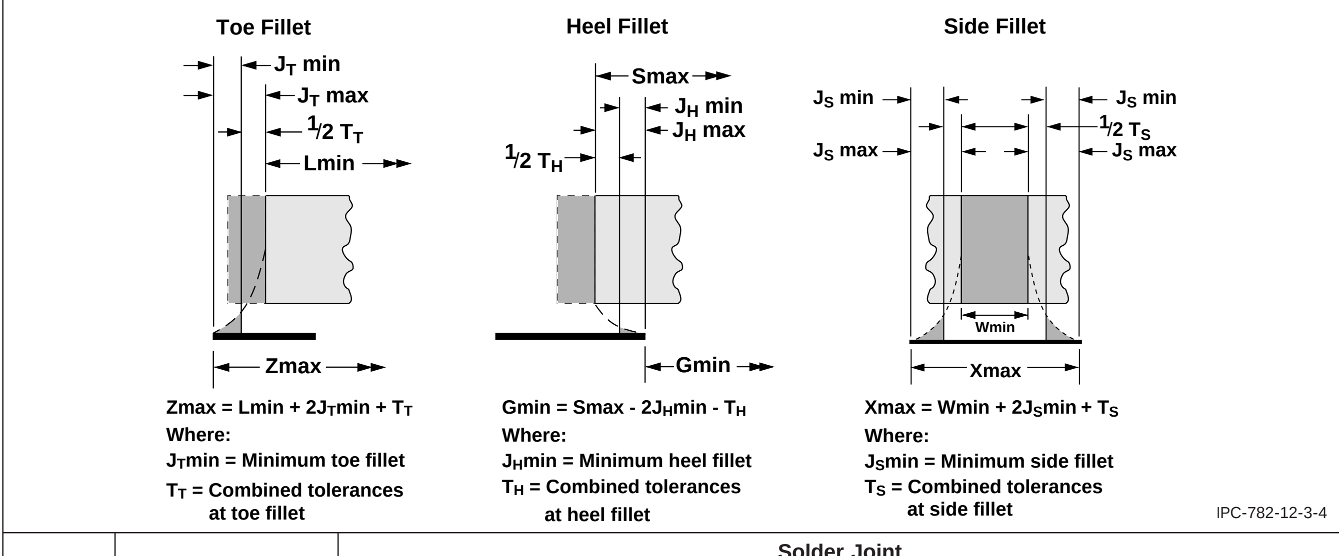
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



	Tolerance Assumptions (mm)		Solder Joint								
			Toe (mm)			Heel (mm)			Side (mm)		
RLP No.	F	P	C_L	$J_T$min	$J_T$max	C_S	$J_H$min	$J_H$max	C_W	J_Sm in	$J_S$max
830	0.20	0.20	0.40	0.95	1.19	0.525	–0.02	0.28	0.480	–0.16	0.12
831	0.20	0.20	0.40	0.91	1.15	0.525	0.02	0.32	0.480	–0.16	0.12
832	0.20	0.20	0.37	0.95	1.18	0.502	–0.01	0.28	0.480	–0.16	0.12
833	0.20	0.20	0.40	0.94	1.18	0.525	–0.01	0.29	0.480	–0.16	0.12
834	0.20	0.20	0.50	0.98	1.27	0.604	–0.09	0.24	0.480	–0.16	0.12
835	0.20	0.20	0.54	0.91	1.21	0.638	-0.03	0.32	0.480	–0.16	0.12
836	0.20	0.20	0.60	0.85	1.19	0.689	–0.00	0.37	0.480	–0.16	0.12
837	0.20	0.20	0.76	0.88	1.28	0.832	–0.10	0.34	0.480	–0.16	0.12
838	0.20	0.20	0.54	0.89	1.19	0.638	–0.01	0.34	0.480	–0.16	0.12
839	0.20	0.20	0.54	0.98	1.28	0.638	–0.10	0.25	0.480	–0.16	0.12
840	0.20	0.20	0.54	0.90	1.20	0.638	–0.02	0.33	0.480	–0.16	0.12

Figure 4 Tolerance and solder joint analysis



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Surface Mount Design and Land Pattern Standard

Date	Section
8/93	13.0
Revision	Subject
	DIPs

1.0 INTRODUCTION

This section covers land patterns for DIPs (Modified Dual-In-Line components). Each subsection contains information in accordance with the following format:

1.0 Scope
2.0 Applicable Documents
3.0 General Component Description (Figure 1)
4.0 Component Dimensions (Figure 2)
5.0 Land Pattern Dimensions (Figure 3)
6.0 Tolerance and Solder Joint Analysis (Figure 4)

The following is the table of contents for this section:

Table of Contents
Modified Dual-In-Line Components

2.0 APPLICABLE DOCUMENTS

The following documents, of the issue in effect on the revision date of this section, form a part of this specification to the extent specified herein.

2.1 Electronic Industries Association (EIA)[1]

EIA-481-A Taping of Surface Mount Components for Automatic Placement

EIA-481-2 16 mm and 24 mm Embossed Carrier Taping of Surface Mount Components for Automated Handling

EIA-481-3 32 mm, 44 mm, and 56 mm Embossed Carrier Taping of Surface Mount Components for Automated Handling

JEDEC Publication Registered and Standard Outlines for Solid State and Related Products:

Outline	Issue	Title
MS-001	C	Standard Dual-In-Line Family, 0.300 in. Row Spacing (Plastic)
MS-010	B	Standard Dual-In-Line Family, 0.400 in. Row Spacing (Plastic)
MS-011	B	Standard Dual-In-Line Family, 0.600 in. Row Spacing (Plastic)

2.2 International Electrotechnical Commission (IEC)[2]

IEC 97 Grid Elements

3.0 GENERAL INFORMATION

3.1 General Component Description A method of modifying DIPs for surface mounting is the ''I'' mounting technique. This involves simply cutting the DIP leads to a short length and placing the device on a pattern of lands to be soldered along with the other surface mounted devices.

1. Application for copies should be addressed to Global Engineering Documents, 1990 M St. N.W., Washington, DC 20036.
2. Application for copes should be addressed to IEC, 3 rue de Varembe, PO Box 131 - 1211 Geneva 20, Switzerland

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IPC-SM-782

Surface Mount Design and Land Pattern Standard

Date	Section
8/93	13.1
Revision	Subject
	DIP

1.0 SCOPE

This subsection provides the component and land pattern dimensions for DIPs (Modified Dual-In-Line components). Basic construction of the DIP device is also covered. At the end of this subsection is a listing of the tolerances and target solder joint dimensions used to arrive at the land pattern dimensions.

2.0 APPLICABLE DOCUMENTS

See Section 13.0 for documents applicable to the subsections.

3.0 COMPONENT DESCRIPTIONS

3.1 Basic Construction See Figure 1. Construction is usually made of plastic or ceramics.

3.1.1 Termination Materials Leads should be solder-coated with a tin/lead alloy. The solder should contain between 58 to 68% tin. Solder may be applied to the termination by hot dipping or by plating from solution. Plated solder terminations should be subjected to a post-plating reflow operation to fuse the solder. The tin/lead finish should be at least 0.00075 mm [0.0003 in] thick.

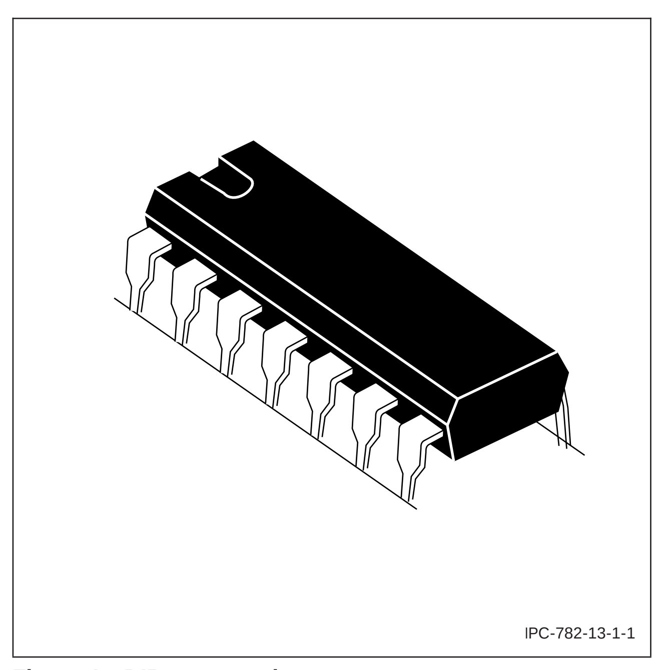


Figure 1 DIP construction

Solder finish applied over precious-metal leads shall have a diffusion-barrier layer between the lead metallization and the solder finish. The barrier layer should be nickel or an equivalent diffusion barrier, and should be at least 0.00125 mm [0.00005 in] thick.

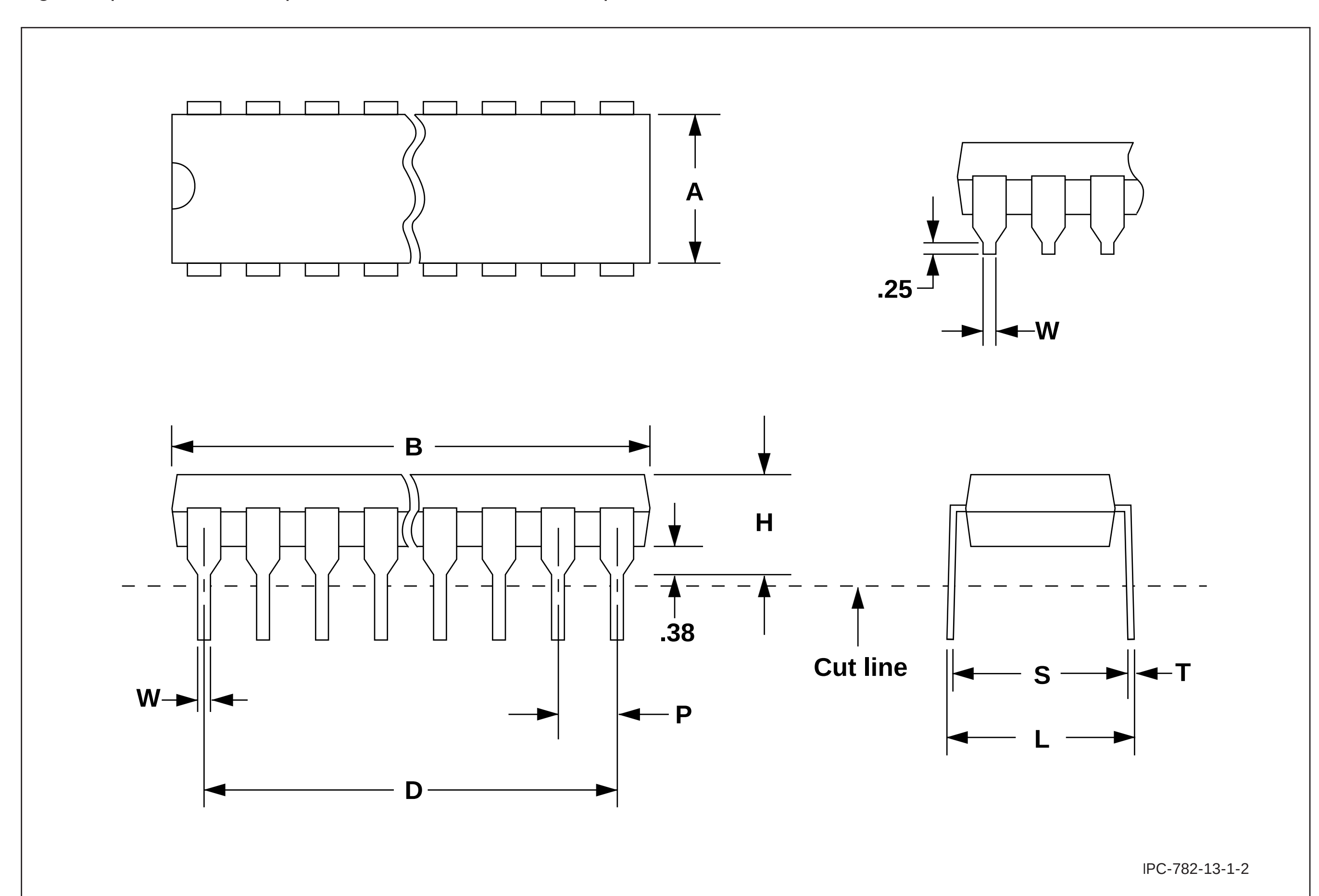
3.1.2 Marking Parts shall be marked with the part number and a date code. In addition, pin 1 shall be identified.

3.1.3 Carrier Package Format Carrier format may be tubes or as agreed to between user and vendor.

3.1.4 Resistance to Soldering The parts should be capable of withstanding ten cycles through a standard reflow system operating at 215°C. Each cycle shall consist of a minimum of 60 seconds exposure at 215°C.

4.0 COMPONENT DIMENSIONS

Figure 2 provides the component dimensions for DIP components.



Component Identifier	L (mm)		S (mm)		W (mm)		T (mm)		A (mm)		B (mm)		H (mm)	P (mm)
	min	max	min	max	min	max	min	max	m in	max	min	max	max	basic
DIP 8	7.62	8.25	6.86	7.54	0.36	0.56	0.20	0.38	6.10	7.11	8.84	10.92	5.33	2.54
DIP 14	7.62	8.25	6.86	7.54	0.36	0.56	0.20	0.38	6.10	7.11	18.42	20.19	5.33	2.54
DIP 16	7.62	8.25	6.86	7.54	0.36	0.56	0.20	0.38	6.10	7.11	18.93	21.33	5.33	2.54
DIP 18	7.62	8.25	6.86	7.54	0.36	0.56	0.20	0.38	6.10	7.11	21.47	23.49	5.33	2.54
DIP 20	7.62	8.25	6.86	7.54	0.36	0.56	0.20	0.38	6.10	7.11	23.50	26.90	5.33	2.54
DIP 22L	9.91	10.79	9.15	10.07	0.36	0.56	0.20	0.38	8.39	9.65	26.67	28.44	5.33	2.54
DIP 24	7.62	8.25	6.86	7.54	0.36	0.56	0.20	0.38	6.10	7.11	28.60	32.30	5.33	2.54
DIP 24L	9.91	10.79	9.15	10.07	0.36	0.56	0.20	0.38	8.39	9.65	29.21	30.98	5.33	2.54
DIP 24X	15.24	15.87	14.48	15.16	0.36	0.56	0.20	0.38	12.32	14.73	29.30	32.70	6.35	2.54
DIP 28	7.62	8.25	6.86	7.54	0.36	0.56	0.20	0.38	6.10	7.11	34.20	36.20	5.33	2.54
DIP 28X	15.24	15.87	14.48	15.16	0.36	0.56	0.20	0.38	12.32	14.73	35.10	39.70	6.35	2.54
DIP 40X	15.24	15.87	14.48	15.16	0.36	0.56	0.20	0.38	12.32	14.73	50.30	53.20	6.35	2.54
DIP 48X	15.24	15.87	14.48	15.16	0.36	0.56	0.20	0.38	12.32	14.73	60.70	63.10	6.35	2.54

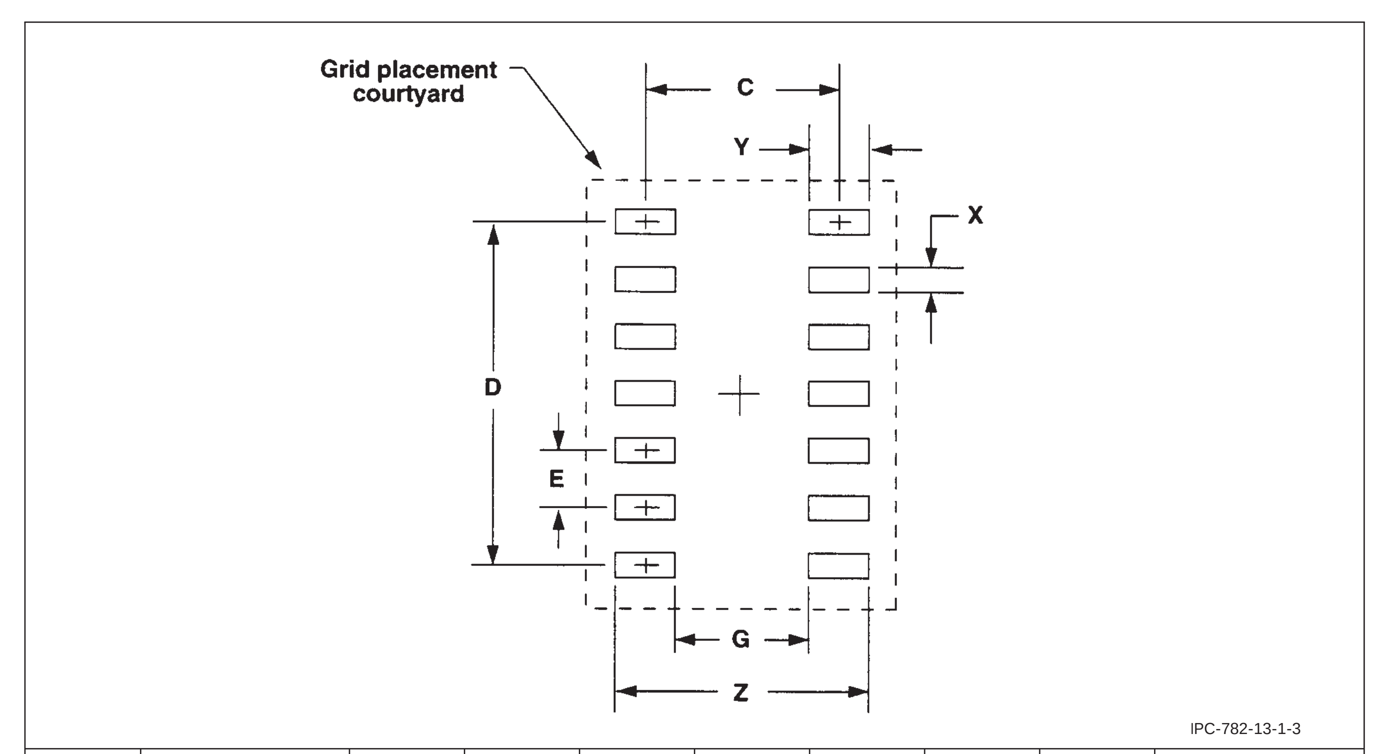
Figure 2 DIP component dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 3 provides the land pattern dimensions for DIP components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

In the table, the dimensions shown are at maximum material condition (MMC). The least material condition (LMC) should not exceed the fabrication (F) allowance shown on page 4. The LMC and the MMC provide the limits for each dimension.

The dotted line in Figure 3 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



RLP No.	Component Identifier	Z (mm)	G (mm)	X (mm)	Y (mm) ref	C (mm) ref	D (mm) ref	E (mm) ref	Placement Grid (No. of Grid Elements)
860	DIP 8	9.80	5.40	1.20	2.20	7.60	7.62	2.54	22x24
861	DIP 14	9.80	5.40	1.20	2.20	7.60	15.24	2.54	22x42
862	DIP 16	9.80	5.40	1.20	2.20	7.60	17.78	2.54	22x44
863	DIP 18	9.80	5.40	1.20	2.20	7.60	20.32	2.54	22x48
864	DIP 20	9.80	5.40	1.20	2.20	7.60	22.86	2.54	22x56
865	DIP 22L	12.40	8.00	1.20	2.20	10.20	25.40	2.54	26x58
866	DIP 24	9.80	5.40	1.20	2.20	7.60	27.94	2.54	38x66
867	DIP 24L	12.40	8.00	1.20	2.20	10.20	27.94	2.54	26x64
867	DIP 24X	17.40	13.00	1.20	2.20	15.20	27.94	2.54	36x68
869	DIP 28	9.80	5.40	1.20	2.20	7.60	33.02	2.54	22x74
870	DIP 28X	17.40	13.00	1.20	2.20	15.20	33.02	2.54	36x84
871	DIP 40X	17.40	13.00	1.20	2.20	15.20	48.26	2.54	36x110
872	DIP 48X	17.40	13.00	1.20	2.20	15.20	58.42	2.54	36x130

Figure 3 DIP land pattern dimensions

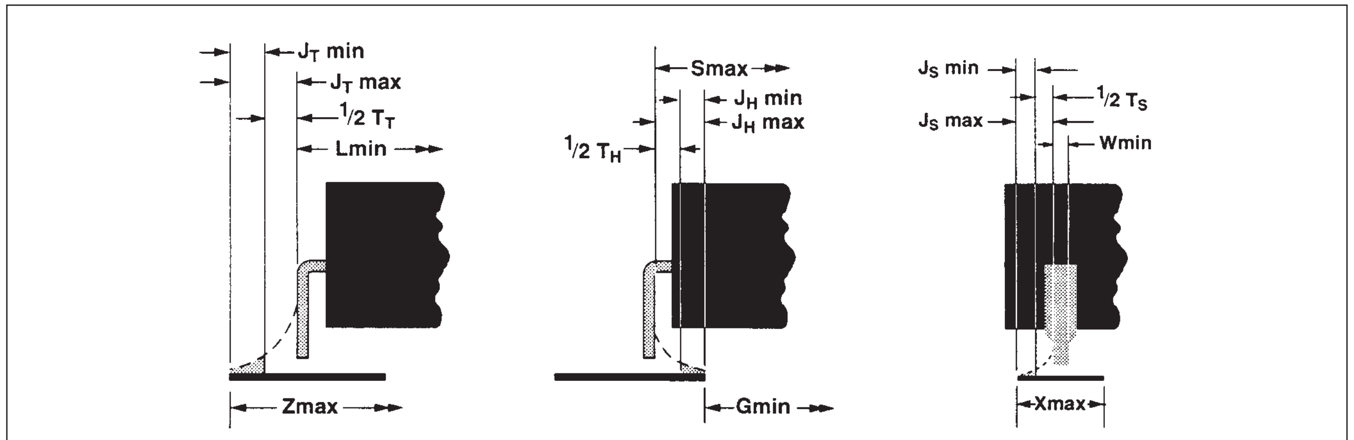
6.0 TOLERANCE AND SOLDER JOINT ANALYSIS

Figure 4 provides an analysis of tolerance assumptions and resultant solder joints based on the land pattern dimensions shown in Figure 3. Tolerances for the component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration.

Figure 4 provides the solder joint minimums for toe, heel, and side fillets, as discussed in Section 3.3. The tolerances are addressed in a statistical mode, and assume even distribution of the tolerances for component, fabrication, and placement accuracy.

Individual tolerances for fabrication (''F'') and component placement equipment accuracy (''P'') are assumed to be as given in the table. These numbers may be modified based on user equipment capability or fabrication criteria. Component tolerance ranges (C_L, C_S, and C_W) are derived by subtracting minimum from maximum dimensions given in Figure 2. The user may also modify these numbers, based on experience with their suppliers. Modification of tolerances may result in alternate land patterns (patterns with dimensions other than the IPC registered land pattern dimensions).

The dimensions for minimum solder fillets at the toe, heel, or side (J_T, J_H, J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the table usually provide for a positive solder fillet. Nevertheless, the user may increase or decrease the minimum value based on process capability.



RLP No.	Tolerance Assumptions (mm)		Solder Joint								
			Toe (mm)			Heel (mm)			Side (mm)		
	F	P	C_L	$J_T$min	$J_T$max	C_S	$J_H$min	$J_H$max	C_W	$J_S$min	$J_S$max
860	0.20	0.20	0.630	0.74	1.09	0.679	0.70	1.07	0.200	0.25	0.42
861	0.20	0.20	0.630	0.74	1.09	0.679	0.70	1.07	0.200	0.25	0.42
862	0.20	0.20	0.630	0.74	1.09	0.679	0.70	1.07	0.200	0.25	0.42
863	0.20	0.20	0.630	0.74	1.09	0.679	0.70	1.07	0.200	0.25	0.42
864	0.20	0.20	0.630	0.74	1.09	0.679	0.70	1.07	0.200	0.25	0.42
865	0.20	0.20	0.880	0.78	1.25	0.916	0.55	1.03	0.200	0.25	0.42
866	0.20	0.20	0.630	0.74	1.09	0.679	0.70	1.07	0.200	0.25	0.42
867	0.20	0.20	0.880	0.78	1.25	0.916	0.55	1.03	0.200	0.25	0.42
868	0.20	0.20	0.630	0.73	1.08	0.679	0.71	1.08	0.200	0.25	0.42
869	0.20	0.20	0.630	0.74	1.09	0.679	0.70	1.07	0.200	0.25	0.42
870	0.20	0.20	0.630	0.73	1.08	0.679	0.71	1.08	0.200	0.25	0.42
871	0.20	0.20	0.630	0.73	1.08	0.679	0.71	1.08	0.200	0.25	0.42
872	0.20	0.20	0.630	0.73	1.08	0.679	0.71	1.08	0.200	0.25	0.42

Figure 4 Tolerance and solder joint analysis



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Surface Mount Design and Land Pattern Standard

Date	Section
4/99	14.0
Revision	Subject
—	Components with Ball Grid Array Contacts

1.0 INTRODUCTION

This section covers land pattern recommendations for ball grid array (BGA) contact devices. Each subsection contains information in accordance with the following format.

1.0 Scope
2.0 Applicable Documents
3.0 General Component Description
4.0 Component Outline
5.0 Land Pattern Dimensions
6.0 Land Pattern Analysis

The following is the table of contents for this section:

Table of Contents
Components with Ball Grid Array Contacts

2.0 APPLICABLE DOCUMENTS

The following documents, of the issue in effect on the current revision date of this section, form a part of this specification to the extent specified herein.

2.1 Electronic Industries Alliance (EIA) Automated Component Handling (ACH) Convention[1]

ACH:EIA-481-A Taping of Surface Mount Components for Automated Placement.

ACH:EIA-481-3 32, 44 and 56 mm Embossed Carrier Taping of Surface Mount Components for Automated Handling.

2.2 Joint Electronic Device Engineering Council[2]

JEDEC Publication 95 Registered and Standard Outlines for Solid State and Related Products:

- Plastic Ball Grid Array (PBGA), MO-151 and MS-028
- Thick Matrix Tray for Handling/Shipping of Ball Grid Array Packages, CO-028
- Thin Matrix Tray for Shipping and Handling of Ball Grid Packages, CO-029.

2.3 Electronic Industries Association of Japan (EIAJ)[3]

EIAJ-ED-7404 General Rules for the Preparation of Outline Drawings of Integrated Circuits

2.4 International Electrotechnical Commission (IEC)[4]

IEC-97 Requirements for Uniform Grid Elements

IEC-60191-2 Mechanical Standardization of Solid State Products

2.5 Joint Industry Standards[5]

J-STD-013 Implementation of Ball Grid Array and Other High Density Technology

3.0 GENERAL INFORMATION

3.1 Component Description The Grid Array device family includes square and rectangular package configurations and is furnished in a variety of base materials. Figure 3-1 shows the elements of a BGA. Base material serves as a mounting structure for attaching the die. Depending on the physical characteristics of the material, flip-chip or wire bond technologies may be employed to route the signal from the die bond pads to the array matrix on the base interface structure. Figure 3-2 compares the top surface attached die to the cavity down configuration.

BGA
Metal Plate Heat Sink
IPC-782143-1

Figure 3-1 Ball Grid Array IC package example

The interface contact or grid is arranged in a uniform column and row format. The standard basic spacing or pitch for the

1. EIA: 2500 Wilson Blvd., Arlington, VA, 22201-3834, USA.
2. JEDEC: 2500 Wilson Blvd., Arlington, VA, 22201-3834, USA.
3. EIAJ: 8th Toyo Kaiji Building 6F, 1-5-13 Nishi-Shinbashi, Minato-ku Tokyo 105, Japan.
4. IEC: 3 rue de Verembe, PO Box 131-1211, Geneva 20, Switzerland.
5. IPC: 2215 Sanders Road, Northbrook, IL 60062

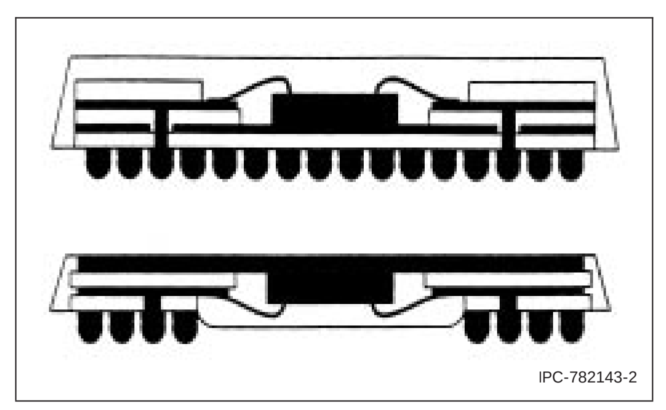


Figure 3-2 Examples of plastic BGA package configurations

contacts is typically 1.0 mm, 1.27 mm and 1.5 mm. The contacts accommodate the electrical and mechanical interface between device and host interconnecting structure (printed board). The contact material will allow conventional reflow solder or other attachment processes.

3.2 Marking The Ball Array device families are generally marked with the manufacturers name or symbol, part number, date code and orientation mark in the corner near contact location A1.

3.3 Carrier Package Format Devices may be furnished in matrix tray or tape and reel packaging formats. Tape and reel packaging is generally preferred for high volume assembly. Plastic trays and reels must be transported and stored in moisture proof containers. When plastic array devices are exposed to the environment for an extended period of time, moisture may absorb into the device. The absorbed moisture, if excessive, may expand (when exposed to higher temperatures typical of reflow solder process), causing cracking and other physical damage.

3.4 Assembly Process Conditions The Grid Array devices are typically attached to the host interface structure using eutectic solder alloy however, optional methods of attachment may include electrically conductive epoxy or polymer. Array package assembly should not require specialized equipment or processes beyond that used for vision assisted SMT pick and place.

4.0 GENERAL CONFIGURATION ISSUES

4.1 Device Outlines The Grid Array package outlines detailed in this document are furnished in JEDEC Publication 95. The overall outline specification for the array device allows a great deal of flexibility as far as lead pitch, contact matrix pattern and construction. The JEDEC standards allow for die attachment on either side of the interface structure (cavity up or cavity down). Refer to J-STD-013 for further definition and interconnect schemes for BGAs.

The example shown in Figure 4-1 illustrates two 225 I/O devices with a common package outline but, with the variation of contact pitch, a unique matrix format is provided.

4.2 Contact Matrix Options Contacts may be distributed in a uniform pattern, however the matrix is always centered about the centerline of the package (see Figure 4-2). Contact depopulation is permitted at the discretion of the device manufacturer. Contact patterns can usually be described in the following methods: full even matrix, full odd matrix, perimeter matrix, or staggered matrix.

4.2.1 Full Matrix For a given package size, there are two full matrix possibilities: even and odd. One of them is the largest matrix that theoretically could fit on the package, given the size and pitch of the contacts. The other matrix is smaller by one row and column. See Figure 4-2.

4.2.2 Perimeter Matrix A perimeter matrix is achieved by removing an array of contacts from the center of the matrix. Center-depopulation does not affect the centerline of the matrix. See Figure 4-3. In addition, Perimeter matrices are usually described by the number of contact perimeters.

4.2.3 Thermally Enhanced Matrix A thermally enhanced matrix is a perimeter matrix with contacts added back in the center. See Figure 4-3.

4.2.4 Staggered Matrix A staggered matrix is defined by the removal of every other contact in an interstitial pattern. This provides an effective minimum center-to-center contact spacing of $\sqrt{2}$ x pitch of the full matrix. See Figure 4-4. In order to retain the A1 contact position, the staggered matrix must be developed using a full odd matrix.

4.3 Selective Depopulation In addition to depopulation methods which lead to the matrices described above, contacts may be removed selectively. Selective depopulation can be accomplished in any manner as long as the pattern matrix is not shifted from the center of the package outline. See Figure 4-5.

4.4 Attachment Site Planning The attachment site or land pattern geometry recommended for BGA devices is round with the diameter adjusted to meet contact pitch and size variation. The diameter of the land should be no larger than the diameter of the land at the package interface and is typically 20% smaller than the normal diameter specified for the ball contact for pitches greater than 1.0 mm and 10%

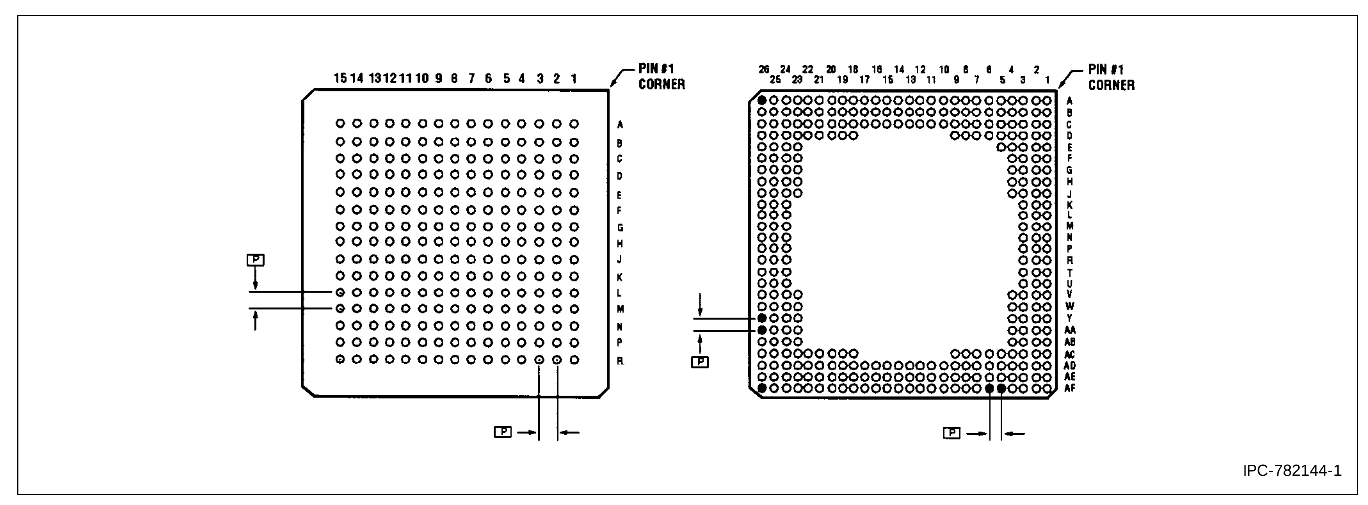


Figure 4-1 Bottom view of BGA devices

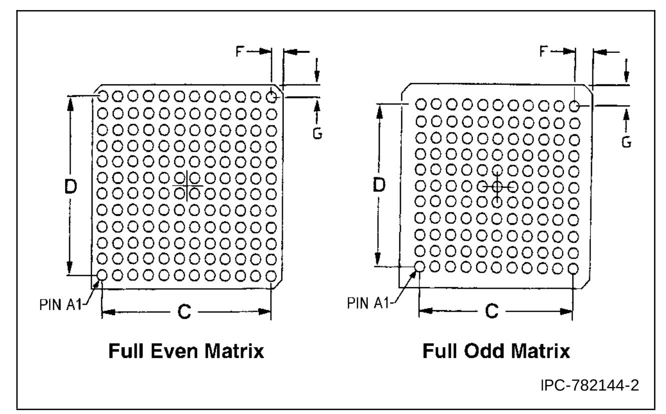


Figure 4-2 One package size, two full matrices

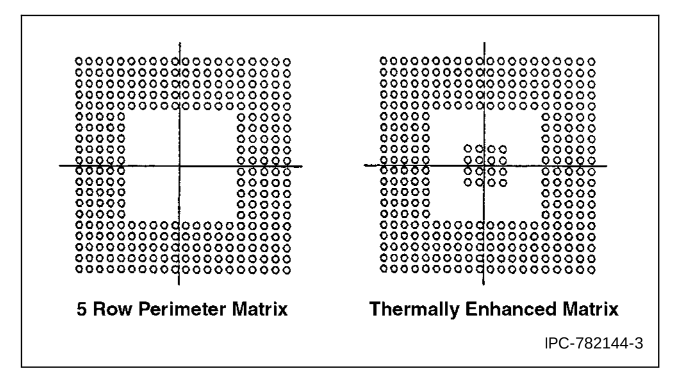


Figure 4-3 Perimeter and thermally enhanced matrices

smaller for pitches less than 1.0 mm. Refer to the manufacturer specification before finalizing land pattern array and geometry.

4.4.1 Copper Defined Land Pattern The land patterns described are defined by the etched copper. Solder mask

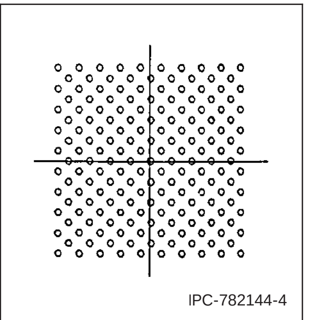




Figure 4-4 Staggered matrix

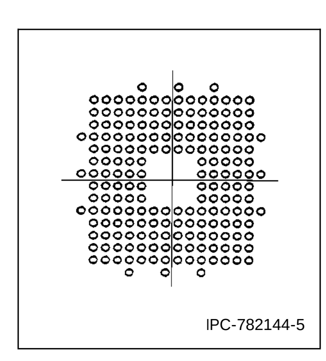


Figure 4-5 Selective depopulation

clearance should be a minimum of 0.075 mm from the etched copper land. For applications requiring a clearance that is less than recommended, consult with the printed board supplier.

4.4.2 Solder Mask Defined Land Pattern If solder mask defined patterns are used, then adjust land pattern diameter accordingly. See Section 6.0.

4.5 Defining Contact Assignment Array contact identification is assigned by the column and row location. For example, A1 contact position is always at an outside corner position with alpha characters arranged in a vertical (row) pattern from top to bottom. Numeric characters are assigned in a horizontal (column) axis (I, O, Q, S, X and Z are omitted). See Figure 4-6.

The designer should note that the A1 position is at the upper left hand corner when the device is viewed from the top. Contact pattern is defined when viewed from the bottom. The land pattern provided on the host substrate is opposite of the contact pattern (with A1 contact position again at the upper left).

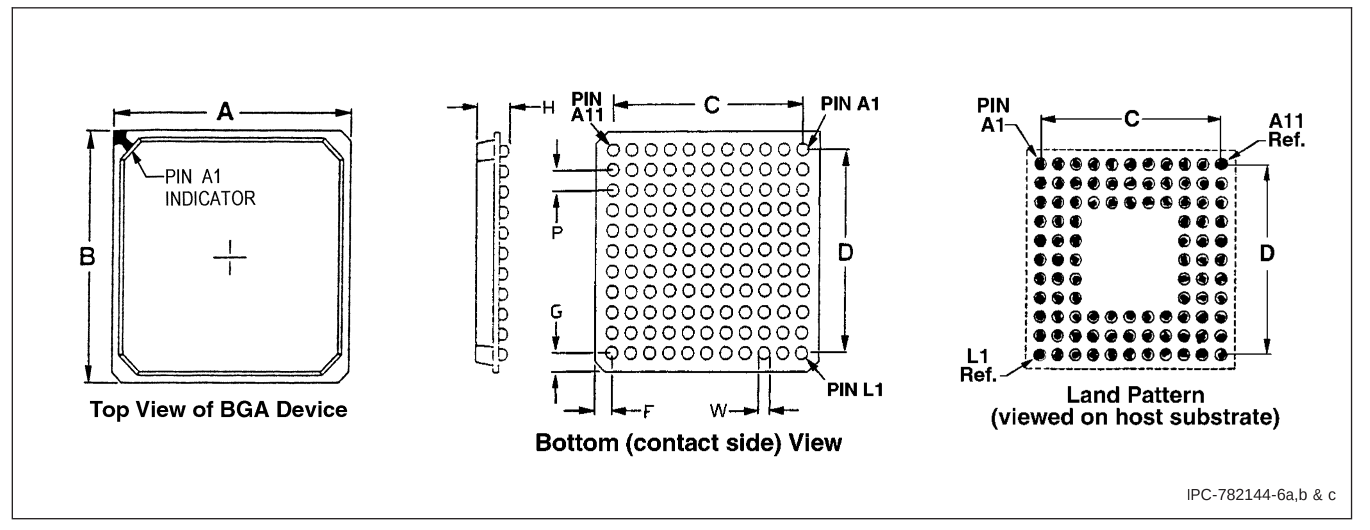


Figure 4-6 Device orientation and contact A1 position

5.0 HANDLING AND SHIPPING

For information on trays and shipping containers refer to ACH:EIA-481-A, ACH:EIA-481-3, JEDEC CO-028, and JEDEC CO-029.

6.0 LAND PATTERN ANALYSIS

The following provides an analysis of tolerance assumptions and result in solder joints based on the land pattern dimensions shown in Figure 4-6. The variations that exist in determining these land patterns include the diameter of the individual ball, the positional accuracy of the ball in relationship to a true position on the component and the board, and the manufacturing allowance that can be held for the land on the substrate that mount the particular ball. The land pattern of the component (where the ball is attached) and the land pattern of the substrate mounting structure (printed board) should be as similar as possible. Component manufacturers have made their determinations that the land pattern of pad on the component should be less than the ball diameter. They base their conclusions on the resulting nominal ball diameter with a slight reduction in the land approximation. Pitch plays a large role in the determination of what ball diameters can be used in various combinations. Table 6-1 shows the characteristics of those balls that are used with pitches of 1.5 mm through 1.0 mm, as well as future ball sizes whose pitches fall between 0.80 mm and 0.25 mm.

6.1 Land Approximation In each instance, component manufacturers and board designers are encouraged to reduce the land size by some percentage of the nominal ball diameter. The amount of reduction is based on the original ball size, which is used to determine the average land. In determining the relationship between nominal characteristics, a manufacturing allowance for land size has been determined

Table 6-1 Ball Diameter Sizes

Nominal Ball Diameter (mm)	Tolerance Variation (mm)	Pitch (mm)
0.75	0.90 - 0.65	1.5, 1.27
0.60	0.70 - 0.50	1.0
0.50	0.55 - 0.45	1.0, 0.8
0.45	0.50 - 0.40	1.0, 0.8, 0.75
0.40	0.45 - 0.35	0.80, 0.75, 0.65
0.30	0.35 - 0.25	0.8, 0.75, 0.65, 0.50
0.25	0.28 - 0.22	0.40
0.20	0.22 - 0.18	0.30
0.15	0.17 - 0.13	0.25

to be 0.1 mm between the Maximum Material Condition (MMC) and Least Material Condition (LMC). Table 6-2 shows the reduction characteristics, the nominal land size, and the target land dimensions, as well as future approximations for ball diameters of 0.40 mm and below.

6.2 Total Variation The total variation of the system considers three major issues: positioning, ball tolerance, and substrate tolerance. All three attributes added together result in a worst case analysis, however as with other land patterns in the standard, a statistical average is determined by using the RMS (root, mean, square) value. Table 6-3 shows the total variation in the system for each of the four ball sizes identified in the standard.

It should be noted that the target value for lands on the substrate of the component or the board should be at Maximum Material Condition. The variation from the Maximum Material Condition indicates that ball-to-land misalignment is achieved

Table 6-2 Land Approximation

Nominal Ball Diameter (mm)	Reduction	Nominal Land Diameter (mm)	Land Variation (mm)
0.75	25%	0.55	0.60 - 0.50
0.60	25%	0.45	0.50 - 0.40
0.50	20%	0.40	0.45 - 0.35
0.45	20%	0.35	0.40 - 0.30
0.40	20%	0.30	0.35 - 0.25
0.30	20%	0.25	0.25 - 0.20
0.25	20%	0.20	0.20 - 0.17
0.20	20%	0.15	0.15 - 0.12
0.15	20%	0.10	0.10 - 0.08

Table 6-3 BGA Variation Attributes

Nominal Ball Size (mm)	Positional Allowance	Ball Tolerance (mm)	Substrate Tolerance (mm)	Variation RMS Value
0.75	0.1 dia. DTP	0.25	0.10	0.25
0.60	0.1 dia. DTP	0.20	0.10	0.24
0.50	0.1 dia. DTP	0.10	0.10	0.17
0.45	0.1 dia. DTP	0.10	0.10	0.17

by taking the maximum land size and subtracting the variation. The resulting dimension would indicate the amount of attachment area that would result from a system where all conditions are at a negative instance. For lands that are solder mask-defined, the land size should be increased by the amount of encroachment of the solder mask. As an example, if the requirement is that solder mask should be on the land by 0.05 mm, then the maximum land size should be increased by 0.1. It should be noted that for solder mask-defined lands, since the land size increases, the opportunity to route conductors between lands is impacted by reducing the available area for conductor width and spacing.

6.3 Future Ball Conditions Although not required for the BGAs shown in the present release of 14.0, future ball sizes contemplated are shown in Table 6-1. Their land size approximations are shown in Table 6-2.

6.4 Land Pattern Calculator The land pattern calculations for BGAs are based on ball size. As a result of ball variation and component conditions, Table 6-4 shows the land pattern calculator headings needed to describe the variations in the system. The RLP number pertains to a single land. It is applicable to all the registered land pattern numbers for the various registered packages shown in Section 14. This data is usually described at the Maximum Material Condition for non-solder mask-defined lands and is dimension X in the various sections. The registered single land pattern numbers for the various ball sizes are shown in Table 6-4.

Table 6-4 Land-to-Ball Calculations for Current and Future BGA Packages (mm)

RLP	Land Size		Location Allowance	Ball Variation	PCB Fabrication Allowance	Ball Size			% Reduction From Nom.	Variation Allowance
	MMC	LMC				Nominal	MMC	LMC		
050	0.60	0.50	0.10	0.25	0.10	0.75	0.90	0.65	25%	0.25
051	0.50	0.40	0.10	0.20	0.10	0.60	0.70	0.50	25%	0.20
052	0.45	0.35	0.10	0.10	0.10	0.50	0.55	0.45	20%	0.17
053	0.40	0.30	0.10	0.10	0.10	0.45	0.50	0.40	20%	0.17
054	0.35	0.25	0.10	0.10	0.10	0.40	0.45	0.35	20%	0.17
055	0.25	0.20	0.05	0.10	0.05	0.30	0.35	0.25	20%	0.15
056	0.20	0.17	0.05	0.06	0.03	0.25	0.28	0.22	20%	0.08
057	0.15	0.12	0.05	0.04	0.03	0.20	0.22	0.18	20%	0.07
058	0.10	0.08	0.05	0.04	0.02	0.15	0.17	0.13	20%	0.07

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1.0 INTRODUCTION

This section covers land pattern recommendations for ball grid array (BGA) contact devices. Each subsection contains information in accordance with the following format.

1.0 Scope
2.0 Applicable Documents
3.0 General Component Description
4.0 Component Outline
5.0 Land Pattern Dimensions
6.0 Land Pattern Analysis

The following is the table of contents for this section:

Table of Contents
Components with Ball Grid Array Contacts

2.0 APPLICABLE DOCUMENTS

The following documents, of the issue in effect on the current revision date of this section, form a part of this specification to the extent specified herein.

2.1 Joint Electronic Device Engineering Council[1]

JEDEC Publication 95 Registered and Standard Outlines for Solid State and Related Products:

- Plastic Ball Grid Array (PBGA), MO-151

3.0 GENERAL INFORMATION

3.1 Component Description The Grid Array device family includes square and rectangular package configurations and is furnished in a plastic base material. Figure 3-1 shows the elements of a BGA. Base material serves as a mounting structure for attaching the die. Depending on the physical characteristics of the material, flip-chip or wire bond technologies may be employed to route the signal from the die bond pads to the array matrix on the base interface structure.

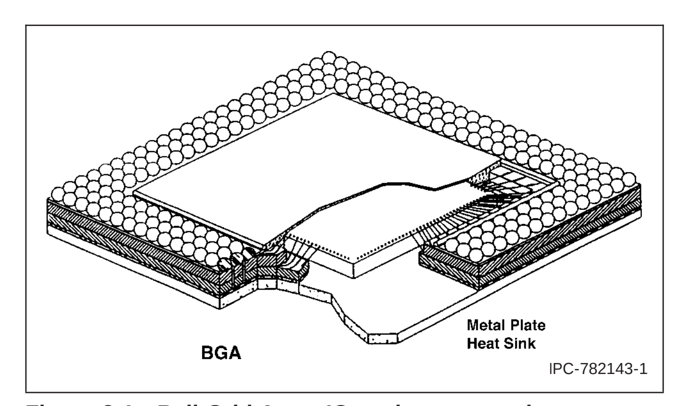


Figure 3-1 Ball Grid Array IC package example

1. JEDEC: 2500 Wilson Blvd., Arlington, VA, 22201-3834, USA.

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IPC-SM-782

Surface Mount Design and Land Pattern Standard

Date	Section
4/99	14.1.1
Revision	Subject
—	1.5 mm Pitch PBGA JEDEC MO-151

1.0 SCOPE

This subsection provides the component and land pattern dimensions for square 1.5 mm pitch Plastic Ball Grid Arrays (PBGA).

2.0 APPLICABLE DOCUMENTS

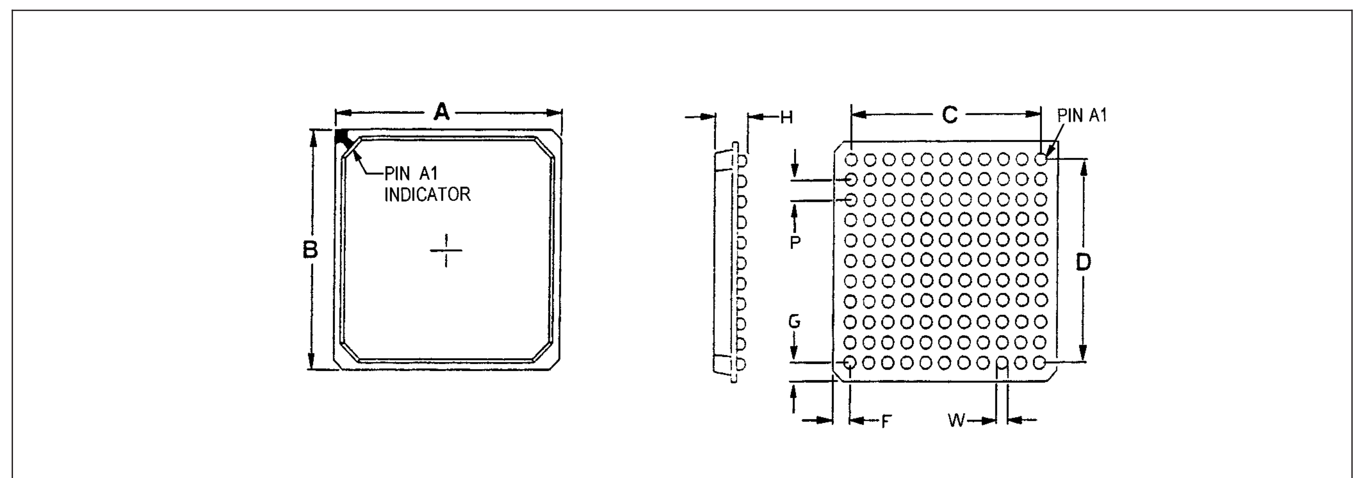
See Section 14.0 for documents applicable to the subsection.

3.0 COMPONENT DESCRIPTION

These components are all on 1.5 mm pitch. They are available in a wide variety of body sizes. The data supplied in the detail and table reflect a full matrix. Specific contact and depopulation and pin assignment must be furnished by the device manufacturer (see Section 14.0 for more information on depopulation methods).

4.0 COMPONENT DIMENSIONS

Figures 1a-1b provides the component dimensions for square PBGAs.



FE = Full Even Matrix
FO = Full Odd Matrix

Component	Contact Array	A	B	C	D	W	P	H	F or G
Identifier	Rows x Cols.	max	max	max	max	nom.	basic	max	nom.
PBGA 7x7 FE16	4x4	7.00	7.00	4.50	4.50	0.75	1.50	3.50	1.25
PBGA 7x7 FO9	3x3	7.00	7.00	3.00	3.00	0.75	1.50	3.50	2.00
PBGA 8x8 FO25	5x5	8.00	8.00	6.00	6.00	0.75	1.50	3.50	1.00
PBGA 8x8 FE16	4x4	8.00	8.00	4.50	4.50	0.75	1.50	3.50	1.75
PBGA 9x9 FE36	6x6	9.00	9.00	7.50	7.50	0.75	1.50	3.50	0.75
PBGA 9x9 FO25	5x5	9.00	9.00	6.00	6.00	0.75	1.50	3.50	1.50
PBGA 10x10 FE36	6x6	10.00	10.00	7.50	7.50	0.75	1.50	3.50	1.25
PBGA 10x10 FO25	5x5	10.00	10.00	6.00	6.00	0.75	1.50	3.50	2.00
PBGA 11x11 FO49	7x7	11.00	11.00	9.00	9.00	0.75	1.50	3.50	1.00
PBGA 11x11 FE36	6x6	11.00	11.00	7.50	7.50	0.75	1.50	3.50	1.75
PBGA 12x12 FE64	8x8	12.00	12.00	10.50	10.50	0.75	1.50	3.50	0.75
PBGA 12x12 FO49	7x7	12.00	12.00	9.00	9.00	0.75	1.50	3.50	1.50
PBGA 13x13 FE64	8x8	13.00	13.00	10.50	10.50	0.75	1.50	3.50	1.25
PBGA 13x13 FO49	7x7	13.00	13.00	9.00	9.00	0.75	1.50	3.50	2.00
PBGA 14x14 FO81	9x9	14.00	14.00	12.00	12.00	0.75	1.50	3.50	1.00
PBGA 14x14 FE64	8x8	14.00	14.00	10.50	10.50	0.75	1.50	3.50	1.75
PBGA 15x15 FE100	10x10	15.00	15.00	13.50	13.50	0.75	1.50	3.50	0.75
PBGA 15x15 FO81	9x9	15.00	15.00	12.00	12.00	0.75	1.50	3.50	1.50
PBGA 17x17 FO121	11x11	17.00	17.00	15.00	15.00	0.75	1.50	3.50	1.00
PBGA 17x17 FE100	10x10	17.00	17.00	13.50	13.50	0.75	1.50	3.50	1.75
PBGA 19X19 FE144	12x12	19.00	19.00	16.50	16.50	0.75	1.50	3.50	1.25
PBGA 19X19 FO121	11x11	19.00	19.00	15.00	15.00	0.75	1.50	3.50	2.00
PBGA 21X21 FE196	14x14	21.00	21.00	19.50	19.50	0.75	1.50	3.50	0.75 0

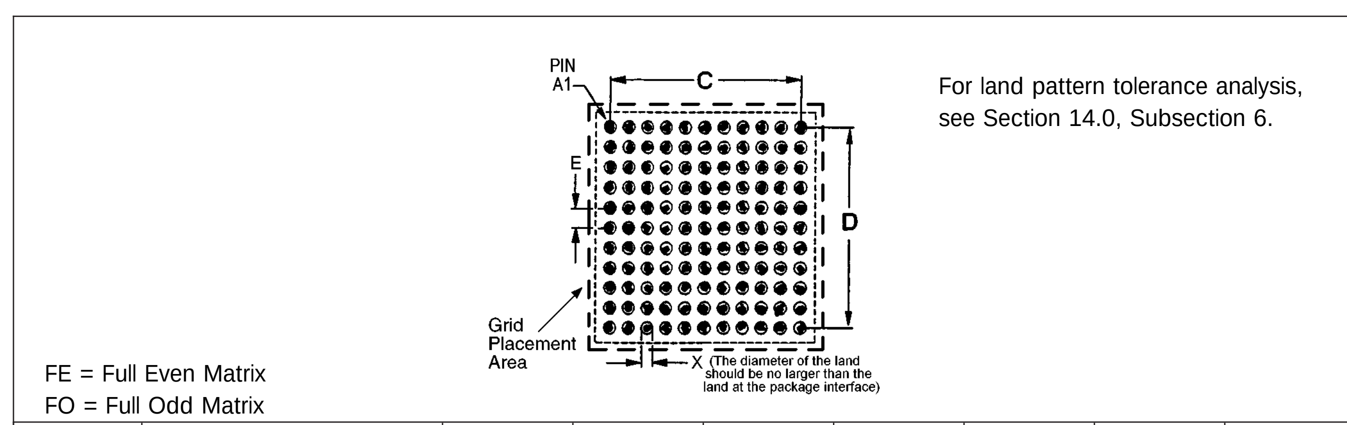
Figure 1a PBGA component dimension

5.0 LAND PATTERN DIMENSIONS

Figures 2a-2b provide the land pattern dimensions for square PBGA components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

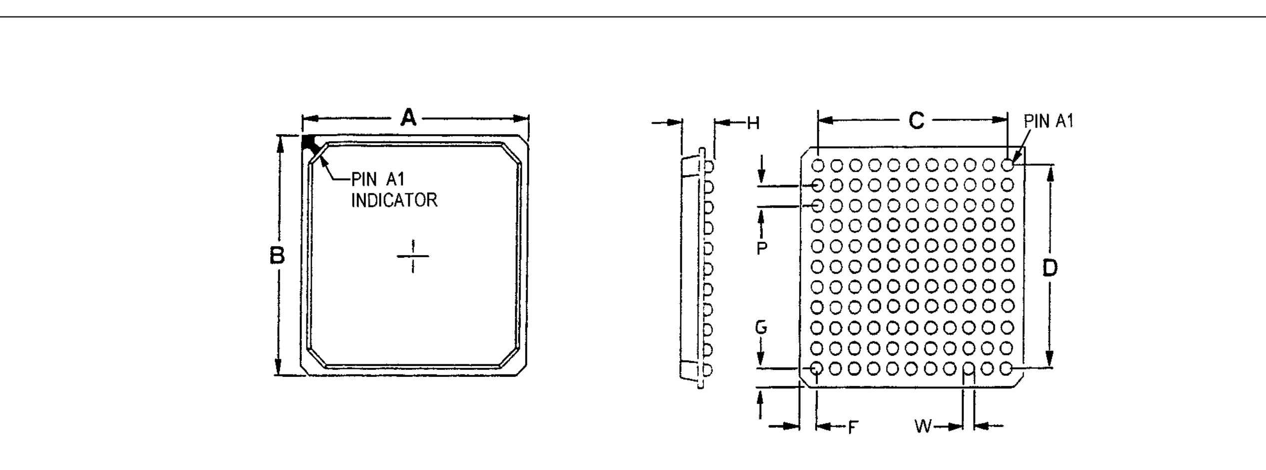
Note: The data supplied in the detail and table reflect a full matrix. Specific contact and depopulation and pin assignment must be furnished by the device manufacturer.

The dotted line in Figures 2a-2b shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



RLP	Component Identifier	Contact Array Rows x Cols.	Max. Contact Count	C	D	X	E	Placement Grid
1020	PBGA 7x7 FE16	4x4	16	4.50	4.50	0.60	1.50	16X16
1021	PBGA 7x7 FO9	3x3	9	3.00	3.00	0.60	1.50	16X16
1022	PBGA 8x8 FO25	5x5	25	6.00	6.00	0.60	1.50	18X18
1023	PBGA 8x8 FE16	4x4	16	4.50	4.50	0.60	1.50	18X18
1024	PBGA 9x9 FE36	6x6	36	7.50	7.50	0.60	1.50	20X20
1025	PBGA 9x9 FO25	5x5	25	6.00	6.00	0.60	1.50	20X20
1026	PBGA 10x10 FE36	6x6	36	7.50	7.50	0.60	1.50	22X22
1027	PBGA 10x10 FO25	5x5	25	6.00	6.00	0.60	1.50	22X22
1028	PBGA 11x11 FO49	7x7	49	9.00	9.00	0.60	1.50	24X24
1029	PBGA 11x11 FE36	6x6	36	7.50	7.50	0.60	1.50	24X24
1030	PBGA 12x12 FE64	8x8	64	10.50	10.50	0.60	1.50	26X26
1031	PBGA 12x12 FO49	7x7	49	9.00	9.00	0.60	1.50	26X26
1032	PBGA 13x13 FE64	8x8	64	10.50	10.50	0.60	1.50	28X28
1033	PBGA 13x13 FO49	7x7	49	9.00	9.00	0.60	1.50	28X28
1034	PBGA 14x14 FO81	9x9	81	12.00	12.00	0.60	1.50	30X30
1035	PBGA 14x14 FE64	8x8	64	10.50	10.50	0.60	1.50	30X30
1036	PBGA 15x15 FE100	10x10	100	13.50	13.50	0.60	1.50	32X32
1037	PBGA 15x15 FO81	9x9	81	12.00	12.00	0.60	1.50	32X32
1038	PBGA 17x17 FO121	11x11	121	15.00	15.00	0.60	1.50	36X36
1039	PBGA 17x17 FE100	10x10	100	13.50	13.50	0.60	1.50	36X36
1040	PBGA 19X19 FE144	12x12	144	16.50	16.50	0.60	1.50	40X40
1041	PBGA 19X19 FO121	11x11	121	15.00	15.00	0.60	1.50	40X40
1042	PBGA 21X21 FE196	14x14	196	19.50	19.50	0.60	1.50	44X44

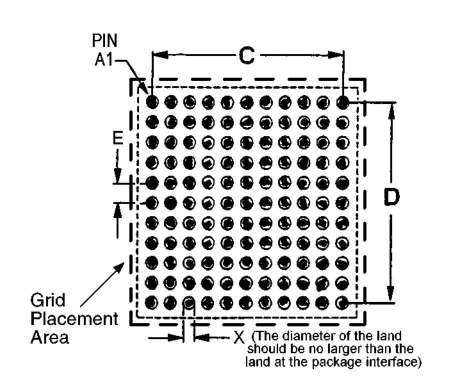
Figure 2a PBGA land pattern dimensions



FE = Full Even Matrix
FO = Full Odd Matrix

Component	Contact Array	A	B	C	D	W	P	H	F or G
Identifier	Rows x Cols.	max	max	max	max	nom.	basic	max	nom.
PBGA 21X21 FO169	13x13	21.00	21.00	18.00	18.00	0.75	1.50	3.50	1.5
PBGA 23X23 FO225	15x15	23.00	23.00	21.00	21.00	0.75	1.50	3.50	1.00
PBGA 23X23 FE196	14x14	23.00	23.00	19.50	19.50	0.75	1.50	3.50	1.75
PBGA 25X25 FE256	16x16	25.00	25.00	22.50	22.50	0.75	1.50	3.50	1.25
PBGA 25X25 FO225	15x15	25.00	25.00	21.00	21.00	0.75	1.50	3.50	2.00
PBGA 27X27 FE324	18x18	27.00	27.00	25.50	25.50	0.75	1.50	3.50	0.75
PBGA 27X27 FO289	17x17	27.00	27.00	24.00	24.00	0.75	1.50	3.50	1.50
PBGA 29X29 FO361	19x19	29.00	29.00	27.00	27.00	0.75	1.50	3.50	1.00
PBGA 29X29 FE324	18x18	29.00	29.00	25.50	25.50	0.75	1.50	3.50	1.75
PBGA 31X31 FE400	20x20	31.00	31.00	28.50	28.50	0.75	1.50	3.50	1.25
PBGA 31X31 FO361	19x19	31.00	31.00	27.00	27.00	0.75	1.50	3.50	2.00
PBGA 33X33 FE484	22x22	33.00	33.00	31.50	31.50	0.75	1.50	3.50	0.75
PBGA 33X33 FO441	21x21	33.00	33.00	30.00	30.00	0.75	1.50	3.50	1.50
PBGA 35X35 FO529	23x23	35.00	35.00	33.00	33.00	0.75	1.50	3.50	1.00
PBGA 35X35 FE484	22x22	35.00	35.00	31.50	31.50	0.75	1.50	3.50	1.75
PBGA 37.5X37.5 FO625	25x25	37.50	37.50	36.00	36.00	0.75	1.50	3.50	0.75
PBGA 37.5X37.5 FE576	24x24	37.50	37.50	34.50	34.50	0.75	1.50	3.50	1.50
PBGA 40X40 FE676	26x26	40.00	40.00	37.50	37.50	0.75	1.50	3.50	1.25
PBGA 40X40 FO625	25x25	40.00	40.00	36.00	36.00	0.75	1.50	3.50	2.00
PBGA 42.5X42.5 FE784	28x28	42.50	42.50	40.50	40.50	0.75	1.50	3.50	1.00
PBGA 42.5X42.5 FO729	27x27	42.50	42.50	39.00	39.00	0.75	1.50	3.50	1.75
PBGA 45X45 FE900	30x30	45.00	45.00	43.50	43.50	0.75	1.50	3.50	0.75
PBGA 45X45 FO841	29x29	45.00	45.00	42.00	42.00	0.75	1.50	3.50	1.50
PBGA 47.5X47.5 FO961	31x31	47.50	47.50	45.00	45.00	0.75	1.50	3.50	1.25
PBGA 47.5X47.5 FE900	30x30	47.50	47.50	43.50	43.50	0.75	1.50	3.50	2.00
PBGA 50X50 FO1089	33x33	50.00	50.00	48.00	48.00	0.75	1.50	3.50	1.00
PBGA 50X50 FE1024	32x32	50.00	50.00	46.50	46.50	0.75	1.50	3.50	1.75

Figure 1b PBGA component dimensions



For land pattern tolerance analysis, see Section 14.0, Subsection 6.

FE = Full Even Matrix
FO = Full Odd Matrix

RLP	Component Identifier	Contact Array Rows x Cols.	Max. Contact Count	C	D	X	E	Placement Grid
1043	PBGA 21X21 FO169	13x13	196	18.00	18.00	0.60	1.50	44X44
1044	PBGA 23X23 FO225	15x15	225	21.00	21.00	0.60	1.50	48X48
1045	PBGA 23X23 FE196	14x14	196	19.50	19.50	0.60	1.50	48X48
1046	PBGA 25X25 FE256	16x16	256	22.50	22.50	0.60	1.50	52X52
1047	PBGA 25X25 FO225	15x15	225	21.00	21.00	0.60	1.50	52X52
1048	PBGA 27X27 FE324	18x18	324	25.50	25.50	0.60	1.50	56X56
1049	PBGA 27X27 FO289	17x17	289	24.00	24.00	0.60	1.50	56X56
1050	PBGA 29X29 FO361	19x19	361	27.00	27.00	0.60	1.50	60X60
1051	PBGA 29X29 FE324	18x18	324	25.50	25.50	0.60	1.50	60X60
1052	PBGA 31X31 FE400	20x20	400	28.50	28.50	0.60	1.50	64X64
1053	PBGA 31X31 FO361	19x19	361	27.00	27.00	0.60	1.50	64X64
1054	PBGA 33X33 FE484	22x22	484	31.50	31.50	0.60	1.50	68X68
1055	PBGA 33X33 FO441	21x21	441	30.00	30.00	0.60	1.50	68X68
1056	PBGA 35X35 FO529	23x23	529	33.00	33.00	0.60	1.50	72X72
1057	PBGA 35X35 FE484	22x22	484	31.50	31.50	0.60	1.50	72X72
1058	PBGA 37.5X37.5 FO625	25x25	625	36.00	36.00	0.60	1.50	78X78
1059	PBGA 37.5X37.5 FE576	24x24	576	34.50	34.50	0.60	1.50	78X78
1060	PBGA 40X40 FE676	26x26	676	37.50	37.50	0.60	1.50	82X82
1061	PBGA 40X40 FO625	25x25	625	36.00	36.00	0.60	1.50	82X82
1062	PBGA 42.5X42.5 FE784	28x28	784	40.50	40.50	0.60	1.50	88X88
1063	PBGA 42.5X42.5 FO729	27x27	729	39.00	39.00	0.60	1.50	88X88
1064	PBGA 45X45 FE900	30x30	900	43.50	43.50	0.60	1.50	92X92
1065	PBGA 45X45 FO841	29x29	841	42.00	42.00	0.60	1.50	92X92
1066	PBGA 47.5X47.5 FO961	31x31	961	45.00	45.00	0.60	1.50	98X98
1067	PBGA 47.5X47.5 FE900	30x30	900	43.50	43.50	0.60	1.50	98X98
1068	PBGA 50X50 FO1089	33x33	1089	48.00	48.00	0.60	1.50	102X102
1069	PBGA 50X50 FE1024	32x32	1024	46.50	46.50	0.60	1.50	102X102

Figure 2b PBGA land pattern dimensions

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IPC-SM-782

Surface Mount Design and Land Pattern Standard

Date	Section
4/99	14.1.2
Revision	Subject
—	1.27 mm Pitch PBGA JEDEC MO-151

1.0 SCOPE

This subsection provides the component and land pattern dimensions for square 1.27 mm pitch Plastic Ball Grid Arrays (PBGA).

2.0 APPLICABLE DOCUMENTS

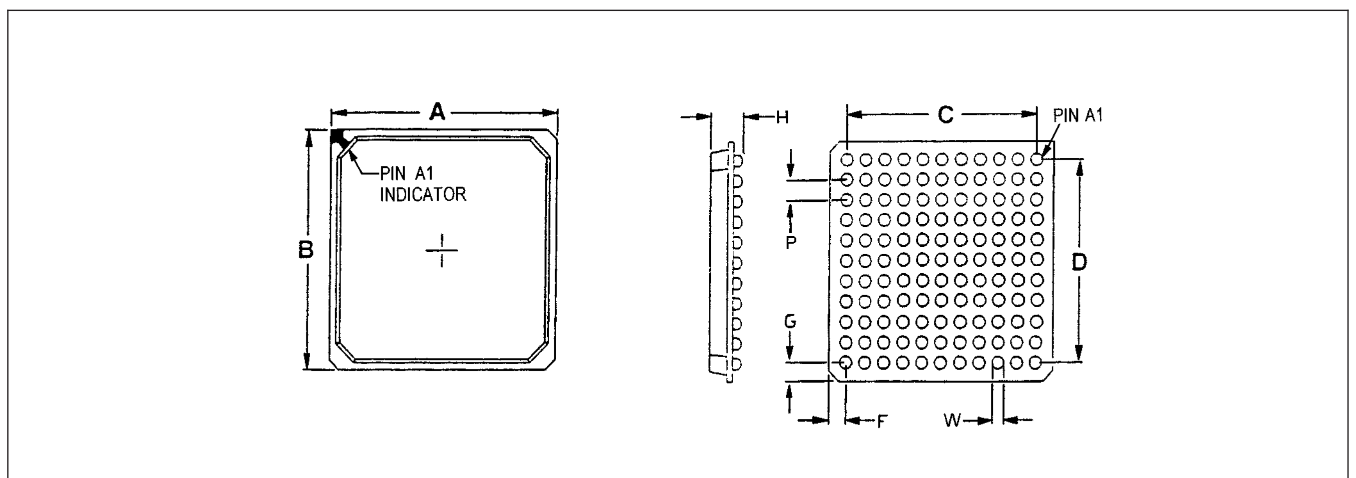
See Section 14.0 for documents applicable to the subsection.

3.0 COMPONENT DESCRIPTION

These components are all on 1.27 mm pitch. They are available in a wide variety of body sizes. The data supplied in the detail and table reflect a full matrix. Specific contact and depopulation and pin assignment must be furnished by the device manufacturer (see Section 14.0 for more information on depopulation methods).

4.0 COMPONENT DIMENSIONS

Figures 1a-1b provide the component dimensions for square PBGAs.



FE = Full Even Matrix
FO = Full Odd Matrix

Component	Contact Array	A	B	C	D	W	P	H	F or G
Identifier	Rows x Cols.	max	max	max	max	nom.	basic	max	nom.
PBGA 7x7 FO25	5x5	7.00	7.00	5.08	5.08	0.75	1.27	3.50	0.96
PBGA 7x7 FE16	4x4	7.00	7.00	3.81	3.81	0.75	1.27	3.50	1.6
PBGA 8x8 FE36	6x6	8.00	8.00	6.35	6.35	0.75	1.27	3.50	0.82
PBGA 8x8 FO25	5x5	8.00	8.00	5.08	5.08	0.75	1.27	3.50	1.46
PBGA 9x9 FE36	6x6	9.00	9.00	6.35	6.35	0.75	1.27	3.50	1.32
PBGA 9x9 FO25	5x5	9.00	9.00	5.08	5.08	0.75	1.27	3.50	1.96
PBGA 10x10 FE49	7x7	10.00	10.00	7.62	7.62	0.75	1.27	3.50	1.19
PBGA 10x 10 FO36	6x6	10.00	10.00	6.35	6.35	0.75	1.27	3.50	1.82
PBGA 11x11 FE64	8x8	11.00	11.00	8.89	8.89	0.75	1.27	3.50	1.05
PBGA 11x11 FO49	7x7	11.00	11.00	7.62	7.62	0.75	1.27	3.50	1.69
PBGA 12x12 FE81	9x9	12.00	12.00	10.16	10.16	0.75	1.27	3.50	0.92
PBGA 12x12 FO64	8x8	12.00	12.00	8.89	8.89	0.75	1.27	3.50	1.56
PBGA 13x13 FE100	10x10	13.00	13.00	11.43	11.43	0.75	1.27	3.50	0.78
PBGA 13x13 FO81	9x9	13.00	13.00	10.16	10.16	0.75	1.27	3.50	1.42
PBGA 14x14 FE100	10x10	14.00	14.00	11.43	11.43	0.75	1.27	3.50	1.28
PBGA 14x14 FO81	9x9	14.00	14.00	10.16	10.16	0.75	1.27	3.50	1.92
PBGA 15x15 FO121	11x11	15.00	15.00	12.70	12.70	0.75	1.27	3.50	1.15
PBGA 15x15 FE100	10x10	15.00	15.00	11.43	11.43	0.75	1.27	3.50	1.78
PBGA 17x17 FO169	13x13	17.00	17.00	15.24	15.24	0.75	1.27	3.50	0.88
PBGA 17x17 FE144	12x12	17.00	17.00	13.97	13.97	0.75	1.27	3.50	1.51
PBGA 19X19 FE196	14x14	19.00	19.00	16.51	16.51	0.75	1.27	3.50	1.24
PBGA 19X19 FO169	13x13	19.00	19.00	15.24	15.24	0.75	1.27	3.50	1.88
PBGA 21X21 FE256	16x16	21.00	21.00	19.05	19.05	0.75	1.27	3.50	0.971

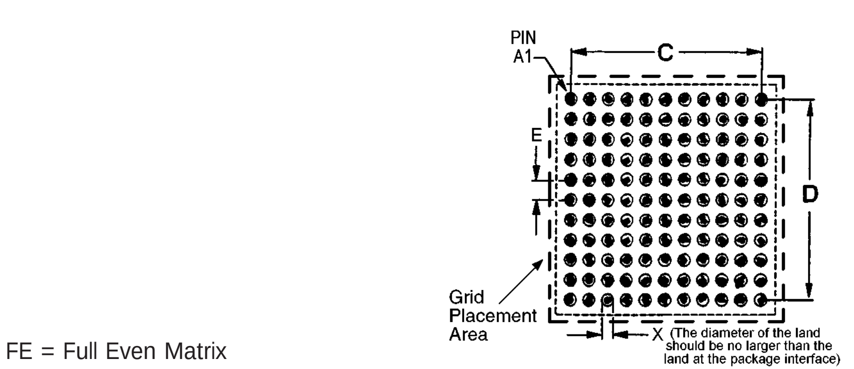
Figure 1a PBGA component dimensions

5.0 LAND PATTERN DIMENSIONS

Figures 2a-2b provide the land pattern dimensions for square PBGA components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

Note: The data supplied in the detail and table reflect a full matrix. Specific contact and depopulation and pin assignment must be furnished by the device manufacturer.

The dotted line in Figures 2a-2b shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.

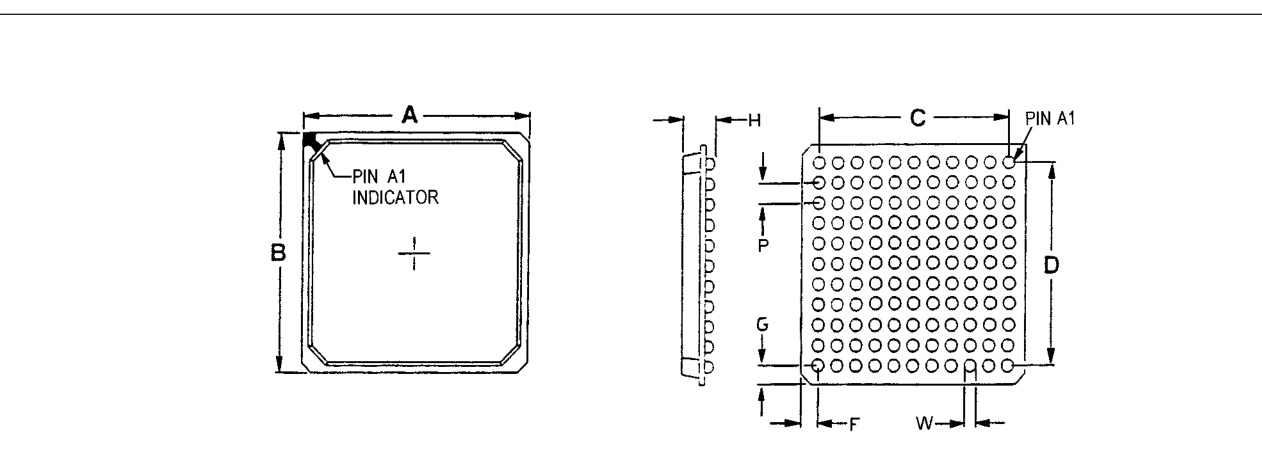


For land pattern tolerance analysis, see Section 14.0, Subsection 6.

FE = Full Even Matrix
FO = Full Odd Matrix

RLP	Component Identifier	Contact Array Rows x Cols.	Max. Contact Count	C	D	X	E	Placement Grid
960	PBGA 7x7 FO25	5x5	25	5.08	5.08	0.60	1.27	16X16
961	PBGA 7x7 FE16	4x4	16	3.81	3.81	0.60	1.27	16X16
962	PBGA 8x8 FE36	6x6	36	6.35	6.35	0.60	1.27	18X18
963	PBGA 8X8 FO25	5x5	25	5.08	5.08	0.60	1.27	18X18
964	PBGA 9x9 FE36	6x6	36	6.35	6.35	0.60	1.27	20X20
965	PBGA 9x9 FO25	5x5	25	5.08	5.08	0.60	1.27	20X20
966	PBGA 10x10 FE49	7x7	49	7.62	7.62	0.60	1.27	22X22
967	PBGA 10x10 FO36	6x6	36	6.35	6.35	0.60	1.27	22X22
968	PBGA 11x11 FE64	8x8	64	8.89	8.89	0.60	1.27	24X24
969	PBGA 11x11 FO49	7x7	49	7.62	7.62	0.60	1.27	24X24
970	PBGA 12x12 FE81	9x9	81	10.16	10.16	0.60	1.27	26X26
971	PBGA 12x12 FO64	8x8	64	8.89	8.89	0.60	1.27	26X26
972	PBGA 13x13 FE100	10x10	100	11.43	11.43	0.60	1.27	28X28
973	PBGA 13x13 FO81	9x9	81	10.16	10.16	0.60	1.27	28X28
974	PBGA 14x14 FE100	10x10	100	11.43	11.43	0.60	1.27	30X30
975	PBGA 14x14 FO81	9x9	81	10.16	10.16	0.60	1.27	30X30
976	PBGA 15x15 FO121	11x11	121	12.70	12.70	0.60	1.27	32X32
977	PBGA 15x15 FE100	10x10	100	11.43	11.43	0.60	1.27	32X32
978	PBGA 17x17 FO169	13x13	169	15.24	15.24	0.60	1.27	36X36
979	PBGA 17x17 FE144	12x12	144	13.97	13.97	0.60	1.27	36X36
980	PBGA 19X19 FE196	14x14	196	16.51	16.51	0.60	1.27	40X40
981	PBGA 19X19 FO169	13x13	169	15.24	15.24	0.60	1.27	40X40
982	PBGA 21X21 FE256	16x16	256	19.05	19.05	0.60	1.27	44X44

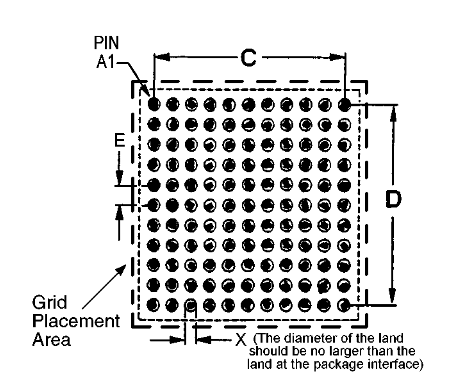
Figure 2a PBGA land pattern dimensions



FE = Full Even Matrix
FO = Full Odd Matrix

Component	Contact Array	A	B	C	D	W	P	H	F or G
Identifier	Rows x Cols.	max	max	max	max	nom.	basic	max	nom.
PBGA 21X21 FO225	15x15	21.00	21.00	17.78	17.78	0.75	1.27	3.50	1.6
PBGA 23X23 FE324	18x18	23.00	23.00	21.59	21.59	0.75	1.27	3.50	0.70
PBGA 23X23 FO289	17x17	23.00	23.00	20.32	20.32	0.75	1.27	3.50	1.34
PBGA 25X25 FO361	19x19	25.00	25.00	22.86	22.86	0.75	1.27	3.50	1.07
PBGA 25X25 FE324	18x18	25.00	25.00	21.59	21.59	0.75	1.27	3.50	1.70
PBGA 27X27 FO441	21x21	27.00	27.00	25.40	25.40	0.75	1.27	3.50	0.80
PBGA 27X27 FE400	20x20	27.00	27.00	24.13	24.13	0.75	1.27	3.50	1.43
PBGA 29X29 FE484	22x22	29.00	29.00	26.67	26.67	0.75	1.27	3.50	1.16
PBGA 29X29 FO441	21x21	29.00	29.00	25.40	25.40	0.75	1.27	3.50	1.80
PBGA 31X31 FE576	24x24	31.00	31.00	29.21	29.21	0.75	1.27	3.50	0.89
PBGA 31X31 FO529	23x23	31.00	31.00	27.94	27.94	0.75	1.27	3.50	1.53
PBGA 33X33 FO625	25x25	33.00	33.00	30.48	30.48	0.75	1.27	3.50	1.26
PBGA 33X33 FE576	24x24	33.00	33.00	29.21	29.21	0.75	1.27	3.50	1.89
PBGA 35X35 FO729	27x27	35.00	35.00	33.02	33.02	0.75	1.27	3.50	0.99
PBGA 35X35 FE676	26x26	35.00	35.00	31.75	31.75	0.75	1.27	3.50	1.62
PBGA 37.5X37.5 FO841	29x29	37.50	37.50	35.56	35.56	0.75	1.27	3.50	0.97
PBGA 37.5X37.5 FE784	28x28	37.50	37.50	34.29	34.29	0.75	1.27	3.50	1.60
PBGA 40X40 FO961	31x31	40.00	40.00	38.10	38.10	0.75	1.27	3.50	0.95
PBGA 40X40 FE900	30x30	40.00	40.00	36.83	36.83	0.75	1.27	3.50	1.58
PBGA 42.5X42.5 FO1089	33x33	42.50	42.50	40.64	40.64	0.75	1.27	3.50	0.93
PBGA 42.5X42.5 FE1024	32x32	42.50	42.50	39.37	39.37	0.75	1.27	3.50	1.56
PBGA 45X45 FO1225	35x35	45.00	45.00	43.18	43.18	0.75	1.27	3.50	0.91
PBGA 45X45 FO1156	34x34	45.00	45.00	41.91	41.91	0.75	1.27	3.50	1.54
PBGA 47.5X47.5 FO1369	37x37	47.50	47.50	45.72	45.72	0.75	1.27	3.50	0.89
PBGA 47.5X47.5 FE1296	36x36	47.50	47.50	44.45	44.45	0.75	1.27	3.50	1.52
PBGA 50X50 FO1521	39x39	50.00	50.00	48.26	48.26	0.75	1.27	3.50	0.87
PBGA 50X50 FE1444	38x38	50.00	50.00	46.99	46.99	0.75	1.27	3.50	1.50

Figure 1b PBGA component dimensions



For land pattern tolerance analysis, see Section 14.0, Subsection 6.

FE = Full Even Matrix
FO = Full Odd Matrix

RLP	Component Identifier	Contact Array Rows x Cols.	Max. Contact Count	C	D	X	E	Placement Grid
983	PBGA 21X21 FO225	15x15	225	17.78	17.78	0.60	1.27	44X44
984	PBGA 23X23 FE324	18x18	324	21.59	21.59	0.60	1.27	48X48
985	PBGA 23X23 FO289	17x17	289	20.32	20.32	0.60	1.27	48X48
986	PBGA 25X25 FO361	19x19	361	22.86	22.86	0.60	1.27	52X52
987	PBGA 25X25 FE324	18x18	324	21.59	21.59	0.60	1.27	52X52
988	PBGA 27X27 FO441	21x21	441	25.40	25.40	0.60	1.27	56X56
989	PBGA 27X27 FE400	20x20	400	24.13	24.13	0.60	1.27	56X56
990	PBGA 29X29 FE484	22x22	484	26.67	26.67	0.60	1.27	60X60
991	PBGA 29X29 FO441	21x21	441	25.40	25.40	0.60	1.27	60X60
992	PBGA 31X31 FE576	24x24	576	29.21	29.21	0.60	1.27	64X64
993	PBGA 31X31 FO529	23x23	529	27.94	27.94	0.60	1.27	64X64
994	PBGA 33X33 FO625	25x25	625	30.48	30.48	0.60	1.27	68X68
995	PBGA 33X33 FE576	24x24	576	29.21	29.21	0.60	1.27	68X68
996	PBGA 35X35 FO729	27x27	729	33.02	33.02	0.60	1.27	72X72
997	PBGA 35X35 FE676	26x26	676	31.75	31.75	0.60	1.27	72X72
998	PBGA 37.5X37.5 FO841	29x29	841	35.56	35.56	0.60	1.27	78X78
999	PBGA 37.5X37.5 FE784	28x28	784	34.29	34.29	0.60	1.27	78X78
1000	PBGA 40X40 FO961	31x31	961	38.10	38.10	0.60	1.27	82X82
1001	PBGA 40X40 FE900	30x30	900	36.83	36.83	0.60	1.27	82X82
1002	PBGA 42.5X42.5 FO1089	33x33	1089	40.64	40.64	0.60	1.27	88X88
1003	PBGA 42.5X42.5 FE1024	32x32	1024	39.37	39.37	0.60	1.27	88X88
1004	PBGA 45X45 FO1225	35x35	1225	43.18	43.18	0.60	1.27	92X92
1005	PBGA 45X45 FO1156	34x34	1156	41.91	41.91	0.60	1.27	92X92
1006	PBGA 47.5X47.5 FO1369	37x37	1369	45.72	45.72	0.60	1.27	98X98
1007	PBGA 47.5X47.5 FE1296	36x36	1296	44.45	44.45	0.60	1.27	98X98
1008	PBGA 50X50 FO1521	39x39	1521	48.26	48.26	0.60	1.27	102X102
1009	PBGA 50X50 FE1444	38x38	1444	46.99	46.99	0.60	1.27	102X102

Figure 2b PBGA land pattern dimensions

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1.0 SCOPE

This subsection provides the component and land pattern dimensions for square 1.0 mm pitch Plastic Ball Grid Arrays (PBGA).

2.0 APPLICABLE DOCUMENTS

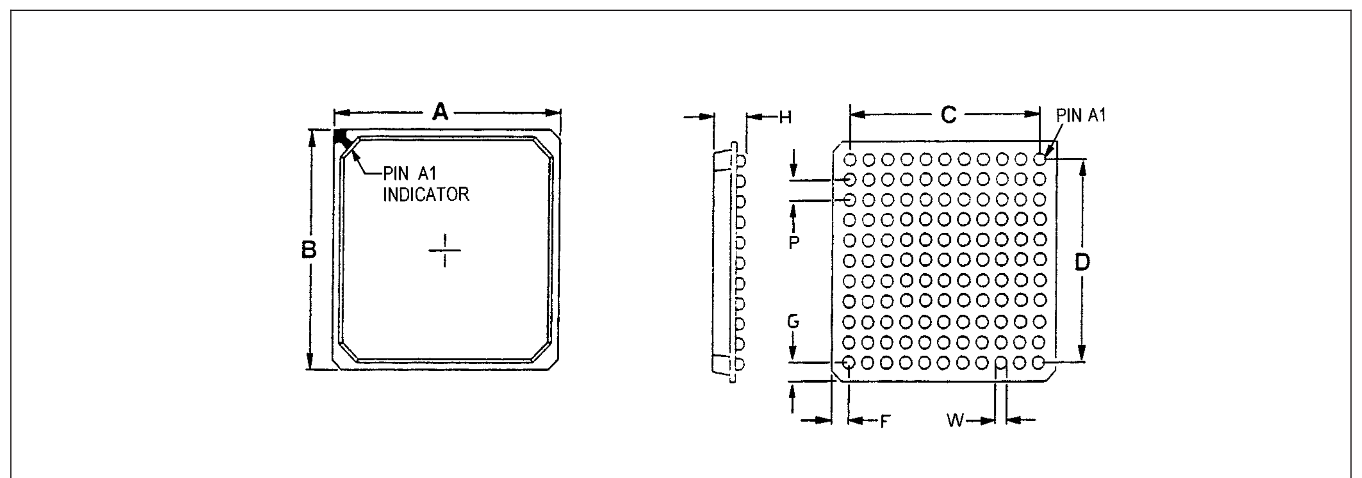
See Section 14.0 for documents applicable to the subsection.

3.0 COMPONENT DESCRIPTION

These components are all on 1.0 mm pitch. They are available in a wide variety of body sizes. The data supplied in the detail and table reflect a full matrix. Specific contact and depopulation and pin assignment must be furnished by the device manufacturer (see Section 14.0 for more information on depopulation methods).

4.0 COMPONENT DIMENSIONS

Figures 1a-1b provides the component dimensions for square PBGAs.



FE = Full Even Matrix
FO = Full Odd Matrix

Component	Contact Array	A	B	C	D	W	P	H	F or G
Identifier	Rows x Cols.	max	max	max	max	nom.	basic	max	nom.
PBGA 7x7 FE36	6x6	7.00	7.00	5.00	5.00	0.60	1.00	3.50	1.00
PBGA 7x7 FO25	5x5	7.00	7.00	4.00	4.00	0.60	1.00	3.50	1.50
PBGA 8x8 F049	7x7	8.00	8.00	6.00	6.00	0.60	1.00	3.50	1.00
PBGA 8x8 FE36	6x6	8.00	8.00	5.00	5.00	0.60	1.00	3.50	1.50
PBGA 9x9 FE64	8x8	9.00	9.00	7.00	7.00	0.60	1.00	3.50	1.00
PBGA 9x9 FO49	7x7	9.00	9.00	6.00	6.00	0.60	1.00	3.50	1.50
PBGA 10x10 FO81	9x9	10.00	10.00	8.00	8.00	0.60	1.00	3.50	1.00
PBGA 10x10 FE64	8x8	10.00	10.00	7.00	7.00	0.60	1.00	3.50	1.50
PBGA 11x11 FE100	10x10	11.00	11.00	9.00	9.00	0.60	1.00	3.50	1.00
PBGA 11x11 FO81	9x9	11.00	11.00	8.00	8.00	0.60	1.00	3.50	1.50
PBGA 12x12 FO121	11x11	12.00	12.00	10.00	10.00	0.60	1.00	3.50	1.00
PBGA 12x12 FE100	10x10	12.00	12.00	9.00	9.00	0.60	1.00	3.50	1.50
PBGA 13x13 FE144	12x12	13.00	13.00	11.00	11.00	0.60	1.00	3.50	1.00
PBGA 13x13 FO121	11x11	13.00	13.00	10.00	10.00	0.60	1.00	3.50	1.50
PBGA 14x14 FO169	13x13	14.00	14.00	12.00	12.00	0.60	1.00	3.50	1.00
PBGA 14x14 FE144	12x12	14.00	14.00	11.00	11.00	0.60	1.00	3.50	1.50
PBGA 15x15 FE196	14x14	15.00	15.00	13.00	13.00	0.60	1.00	3.50	1.00
PBGA 15x15 FO169	13x13	15.00	15.00	12.00	12.00	0.60	1.00	3.50	1.50
PBGA 17x17 FE256	16x16	17.00	17.00	15.00	15.00	0.60	1.00	3.50	1.00
PGBA 17x17 FO225	15x15	17.00	17.00	14.00	14.00	0.60	1.00	3.50	1.50
PBGA 19X19 FE324	18X18	19.00	19.00	17.00	17.00	0.60	1.00	3.50	1.00
PBGA 19x19 FO289	17x17	19.00	19.00	16.00	16.00	0.60	1.00	3.50	1.50
PBGA 21X21 FE400	20X20	21.00	21.00	19.00	19.00	0.60	1.00	3.50	1.00

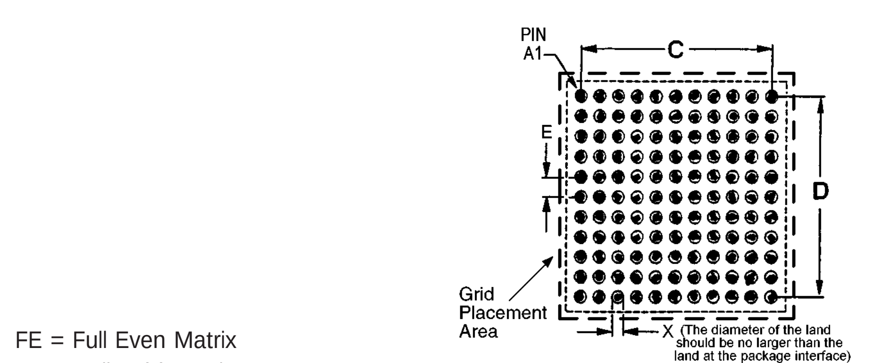
Figure 1a   PBGA component dimensions

5.0 LAND PATTERN DIMENSIONS

Figures 2a-2b provide the land pattern dimensions for square PBGA components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

Note: The data supplied in the detail and table reflect a full matrix. Specific contact and depopulation and pin assignment must be furnished by the device manufacturer.

The dotted line in Figures 2a-2b shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.

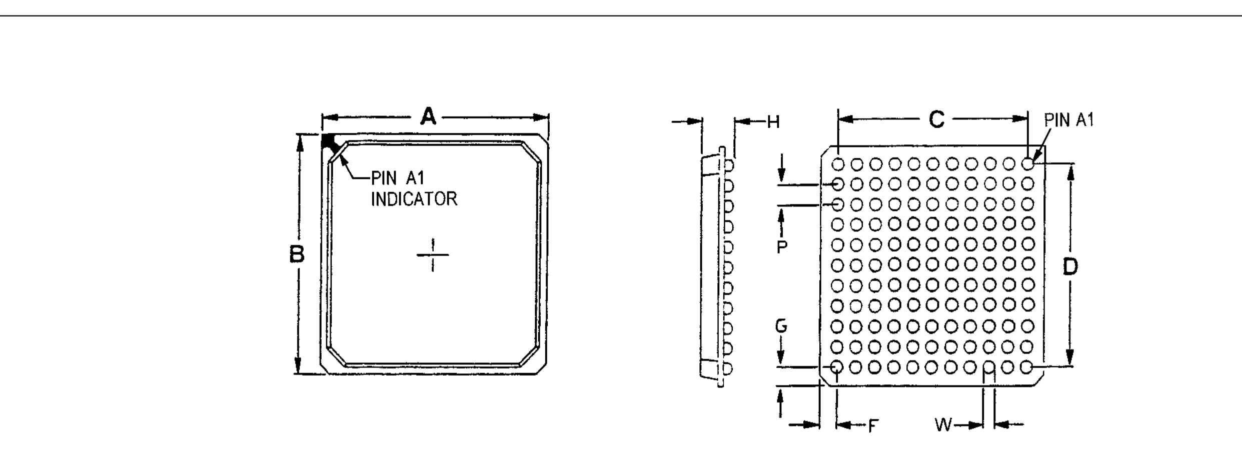


For land pattern tolerance analysis, see Section 14.0, Subsection 6.

FE = Full Even Matrix
FO = Full Odd Matrix

RLP	Component Identifier	Contact Array Rows x Cols.	Max. Contact Count	C	D	X	E	Placement Grid
900	PBGA 7x7 FE36	6x6	36	5.00	5.00	0.50	1.00	16X16
901	PBGA 7x7 FO25	5x5	25	4.00	4.00	0.50	1.00	16X16
902	PBGA 8x8 F049	7x7	49	6.00	6.00	0.50	1.00	18X18
903	PBGA 8x8 FE36	6x6	36	5.00	5.00	0.50	1.00	18X18
904	PBGA 9x9 FE64	8x8	64	7.00	7.00	0.50	1.00	20X20
905	PBGA 9x9 FO49	7x7	49	6.00	6.00	0.50	1.00	20X20
906	PBGA 10x10 FO81	9x9	81	8.00	8.00	0.50	1.00	22X22
907	PBGA 10x10 FE64	8x8	64	7.00	7.00	0.50	1.00	22X22
908	PBGA 11x11 FE100	10x10	100	9.00	9.00	0.50	1.00	24X24
909	PBGA 11x11 FO81	9x9	81	8.00	8.00	0.50	1.00	24X24
910	PBGA 12x12 FO121	11x11	121	10.00	10.00	0.50	1.00	26X26
911	PBGA 12x12 FE100	10x10	100	9.00	9.00	0.50	1.00	26X26
912	PBGA 13x13 FE144	12x12	144	11.00	11.00	0.50	1.00	28X28
913	PBGA 13x13 FO121	11x11	121	10.00	10.00	0.50	1.00	28X28
914	PBGA 14x14 FO169	13x13	169	12.00	12.00	0.50	1.00	30X30
915	PBGA 14x14 FE144	12x12	144	11.00	11.00	0.50	1.00	30X30
916	PBGA 15x15 FE196	14x14	196	13.00	13.00	0.50	1.00	32X32
917	PBGA 15x15 FO169	13x13	169	12.00	12.00	0.50	1.00	32X32
918	PBGA 17x17 FE256	16x16	256	15.00	15.00	0.50	1.00	36X36
919	PGBA 17x17 FO225	15x15	225	14.00	14.00	0.50	1.00	36X36
920	PBGA 19X19 FE324	18X18	324	17.00	17.00	0.50	1.00	40X40
921	PBGA 19x19 FO289	17x17	289	16.00	16.00	0.50	1.00	40X40
922	PBGA 21X21 FE400	20X20	400	19.00	19.00	0.50	1.00	44X44

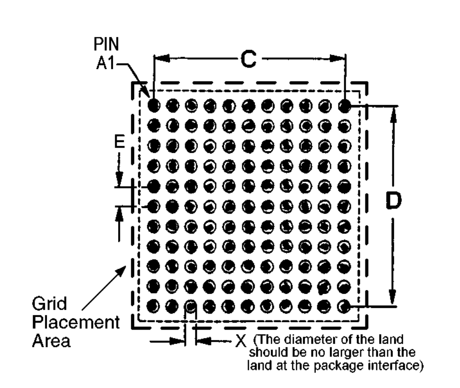
Figure 2a PBGA land pattern dimensions



FE = Full Even Matrix
FO = Full Odd Matrix

Component	Contact Array	A	B	C	D	W	P	H	F or G
Identifier	Rows x Cols.	max	max	max	max	nom.	basic	max	nom.
PBGA 21x21 FO361	19x19	21.00	21.00	18.00	18.00	0.60	1.00	3.50	1.50
PBGA 23X23 FE484	22X22	23.00	23.00	21.00	21.00	0.60	1.00	3.50	1.00
PBGA 23x23 FO441	21x21	23.00	23.00	20.00	20.00	0.60	1.00	3.50	1.50
PBGA 25X25 FE576	24X24	25.00	25.00	23.00	23.00	0.60	1.00	3.50	1.00
PBGA 25x25 FO529	23x23	25.00	25.00	22.00	22.00	0.60	1.00	3.50	1.50
PBGA 27X27 FE676	26X26	27.00	27.00	25.00	25.00	0.60	1.00	3.50	1.00
PBGA 27X27 FO625	25x25	27.00	27.00	24.00	24.00	0.60	1.00	3.50	1.50
PBGA 29X29 FE784	28X28	29.00	29.00	27.00	27.00	0.60	1.00	3.50	1.00
PBGA 29X29 FO729	27x27	29.00	29.00	26.00	26.00	0.60	1.00	3.50	1.50
PBGA 31X31 FE900	30X30	31.00	31.00	29.00	29.00	0.60	1.00	3.50	1.00
PBGA 31X31 FO841	29x29	31.00	31.00	28.00	28.00	0.60	1.00	3.50	1.50
PBGA 33X33 FE1024	32X32	33.00	33.00	31.00	31.00	0.60	1.00	3.50	1.00
PBGA 33X33 FO961	31x31	33.00	33.00	30.00	30.00	0.60	1.00	3.50	1.50
PBGA 35X35 FE1156	34X34	35.00	35.00	33.00	33.00	0.60	1.00	3.50	1.00
PBGA 35X35 FO1089	33x33	35.00	35.00	32.00	32.00	0.60	1.00	3.50	1.50
PBGA 37.5X37.5 FO1369	37X37	37.50	37.50	36.00	36.00	0.60	1.00	3.50	0.75
PBGA 37.5X37.5 FE1296	36x36	37.50	37.50	35.00	35.00	0.60	1.00	3.50	1.25
PBGA 40X40 FO1521	39X39	40.00	40.00	38.00	38.00	0.60	1.00	3.50	1.00
PBGA 40X40 FE1444	38x38	40.00	40.00	37.00	37.00	0.60	1.00	3.50	1.50
PBGA 42.5X42.5 FE1764	42X42	42.50	42.50	41.00	41.00	0.60	1.00	3.50	0.75
PBGA 42.5X42.5 FO1681	41x41	42.50	42.50	40.00	40.00	0.60	1.00	3.50	1.25
PBGA 45X45 FE1936	44X44	45.00	45.00	43.00	43.00	0.60	1.00	3.50	1.00
PBGA 45X45 FO1849	43x43	45.00	45.00	42.00	42.00	0.60	1.00	3.50	1.50
PBGA 47.5X47.5 FO2209	47X47	47.50	47.50	46.00	46.00	0.60	1.00	3.50	0.75
PBGA 47.5X47.5 FE2116	46x46	47.50	47.50	45.00	45.00	0.60	1.00	3.50	1.25
PBGA 50X50 FO2401	49X49	50.00	50.00	48.00	48.00	0.60	1.00	3.50	1.00
PBGA 50X50 FE2304	48x48	50.00	50.00	47.00	47.00	0.60	1.00	3.50	1.50

Figure 1b PBGA component dimensions



For land pattern tolerance analysis, see Section 14.0, Subsection 6.

FE = Full Even Matrix
FO = Full Odd Matrix

RLP	Component Identifier	Contact Array Rows x Cols.	Max. Contact Count	C	D	X	E	Placement Grid
923	PBGA 21x21 FO361	19x19	361	18.00	18.00	0.50	1.00	44X44
924	PBGA 23X23 FE484	22X22	484	21.00	21.00	0.50	1.00	48X48
925	PBGA 23x23 FO441	21x21	441	20.00	20.00	0.50	1.00	48X48
926	PBGA 25X25 FE576	24X24	576	23.00	23.00	0.50	1.00	52X52
927	PBGA 25x25 FO529	23x23	529	22.00	22.00	0.50	1.00	52X52
928	PBGA 27X27 FE676	26X26	676	25.00	25.00	0.50	1.00	56X56
929	PBGA 27X27 FO625	25x25	625	24.00	24.00	0.50	1.00	56X56
930	PBGA 29X29 FE784	28X28	784	27.00	27.00	0.50	1.00	60X60
931	PBGA 29X29 FO729	27x27	729	26.00	26.00	0.50	1.00	60X60
932	PBGA 31X31 FE900	30X30	900	29.00	29.00	0.50	1.00	64X64
933	PBGA 31X31 FO841	29x29	841	28.00	28.00	0.50	1.00	64X64
934	PBGA 33X33 FE1024	32X32	1024	31.00	31.00	0.50	1.00	68X68
935	PBGA 33X33 FO961	31x31	961	30.00	30.00	0.50	1.00	68X68
936	PBGA 35X35 FE1156	34X34	1156	33.00	33.00	0.50	1.00	72X72
937	PBGA 35X35 FO1089	33x33	1089	32.00	32.00	0.50	1.00	72X72
938	PBGA 37.5X37.5 FO1369	37X37	1369	36.00	36.00	0.50	1.00	78X78
939	PBGA 37.5X37.5 FE1296	36x36	1296	35.00	35.00	0.50	1.00	78X78
940	PBGA 40X40 FO1521	39X39	1521	38.00	38.00	0.50	1.00	82X82
941	PBGA 40X40 FE1444	38x38	1444	37.00	37.00	0.50	1.00	82X82
942	PBGA 42.5X42.5 FE1764	42X42	1764	41.00	41.00	0.50	1.00	88X88
943	PBGA 42.5X42.5 FO1681	41x41	1681	40.00	40.00	0.50	1.00	88X88
945	PBGA 45X45 FE1936	44X44	1936	43.00	43.00	0.50	1.00	92X92
946	PBGA 45X45 FO1849	43x43	1849	42.00	42.00	0.50	1.00	92X92
947	PBGA 47.5X47.5 FO2209	47X47	2209	46.00	46.00	0.50	1.00	98X98
948	PBGA 47.5X47.5 FE2116	46x46	2116	45.00	45.00	0.50	1.00	98X98
949	PBGA 50X50 FO2401	49X49	2401	48.00	48.00	0.50	1.00	102X102
950	PBGA 50X50 FE2304	48x48	2304	47.00	47.00	0.50	1.00	102X102

Figure 2b PBGA land pattern dimensions

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IPC-SM-782

Surface Mount Design and Land Pattern Standard

Date	Section
4/99	14.2
Revision	**Subject**
—	1.27 mm Pitch Rectangular PBGA JEDEC MS-028

1.0 SCOPE

This subsection provides the component and land pattern dimensions for rectangular 1.27 mm pitch Plastic Ball Grid Arrays (PBGA).

2.0 APPLICABLE DOCUMENTS

The following documents, of the issue in effect on the current revision date of this section, form a part of this specification to the extent specified herein.

2.1 Joint Electronic Device Engineering Council[1]

JEDEC Publication 95 Registered and Standard Outlines for Solid State and Related Products:

• Rectangular Plastic Ball Grid Array (R-PBGA), MS-028

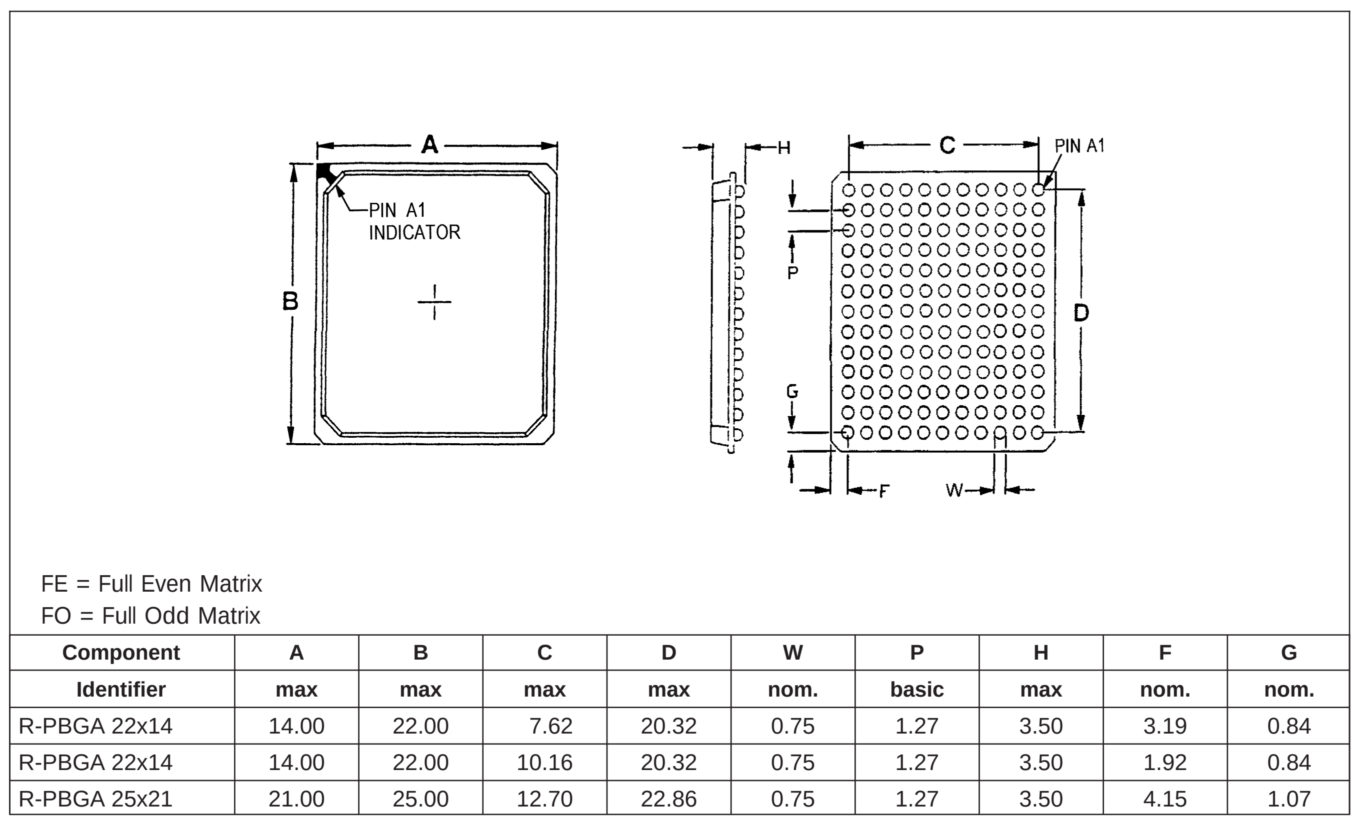
3.0 COMPONENT DESCRIPTION

These components are all on 1.27 mm pitch. They are available in a wide variety of body sizes. The data supplied in the detail and table reflect a full matrix. Specific contact and depopulation and pin assignment must be furnished by the device manufacturer (see Section 14.0 for more information on depopulation methods).

1. JEDEC: 2500 Wilson Blvd., Arlington, VA, 22201-3834, USA.

4.0 COMPONENT DIMENSIONS

Figure 1 provides the component dimensions for rectangular PBGAs.



FE = Full Even Matrix
FO = Full Odd Matrix

Component	A	B	C	D	W	P	H	F	G
Identifier	max	max	max	max	nom.	basic	max	nom.	nom.
R-PBGA 22x14	14.00	22.00	7.62	20.32	0.75	1.27	3.50	3.19	0.84
R-PBGA 22x14	14.00	22.00	10.16	20.32	0.75	1.27	3.50	1.92	0.84
R-PBGA 25x21	21.00	25.00	12.70	22.86	0.75	1.27	3.50	4.15	1.07

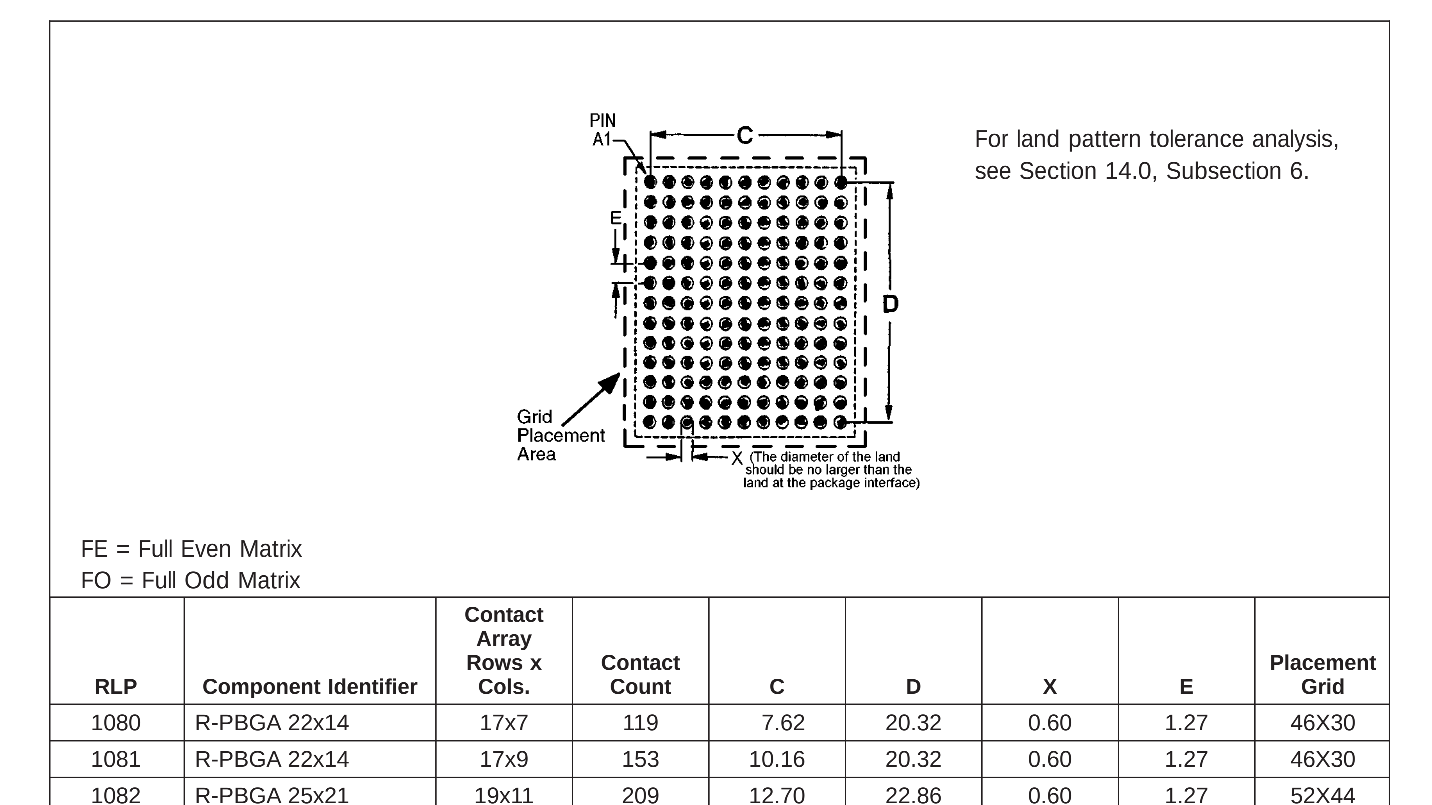
Figure 1 R-PBGA component dimensions

5.0 LAND PATTERN DIMENSIONS

Figure 2 provides the land pattern dimensions for square PBGA components. These numbers represent industry consensus on the best dimensions based on empirical knowledge of fabricated land patterns.

Note: The data supplied in the detail and table reflect a full matrix. Specific contact and depopulation and pin assignment must be furnished by the device manufacturer.

The dotted line in Figure 2 shows the grid placement courtyard which is the area required to place land patterns and their respective components in adjacent proximity without interference or shorting. Numbers in the table represent the number of grid elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97.



RLP	Component Identifier	Contact Array Rows x Cols.	Contact Count	C	D	X	E	Placement Grid
1080	R-PBGA 22x14	17x7	119	7.62	20.32	0.60	1.27	46X30
1081	R-PBGA 22x14	17x9	153	10.16	20.32	0.60	1.27	46X30
1082	R-PBGA 25x21	19x11	209	12.70	22.86	0.60	1.27	52X44

Figure 2 R-PBGA land pattern dimensions

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Appendix A
IPC-EM-782
Data Analysis Spreadsheets
for IPC-SM-782 Land Patterns

The IPC has developed a spreadsheet and user's guide for the manipulation of data that supports the concepts and methodology for developing surface mount land patterns that are identified in IPC-SM-782, ''Surface Mount Design and Land Pattern Standard.'' This product is:

IPC-EM-782, ''Data Analysis Spreadsheets for IPC-SM-782 Land Patterns''

The information contained in the various files of the disk provide the appropriate size, shape, and tolerance of surface mount land patterns that insure sufficient area for appropriate solder fillets, and allow for the inspection and testing of those solder joints.

The equations built into the spreadsheet format follow the principles delineated in IPC-SM-782. They have been organized into various columns and rows for ease of use in both understanding the principles, and allowing users of the disk to manipulate the data in a manner to achieve optimum solder joint formation for their particular projects.

The data reflects the printed and agreed to land pattern sizes. Each land pattern has been registered with its own number in a significant numbering system that correlates a land pattern to a specific surface mount component.

Although many spreadsheets exist in industry, Lotus was chosen because these concepts were relatively basic, and could be used by the majority of other spreadsheet programs. Although newer and more exotic techniques are available, the principles embodied in the ''Electronic Media (EM)'' have been kept as simple as possible so that the information can be transported to other spreadsheets with which users feel more comfortable.

Names of Files

There are numerous files on the master disc. They match the component families and their assigned section.

The following is an example of the names of the files and their descriptions related to the IPC-SM-782:

8.1 Chip Resistors	81CHPRES.WK1
8.2 Chip Depositors	82CHPCAP.WK1
8.3 Inductors	83CHPIND.WK1
8.4 Teflon Capacitors	84DANCAP.WK1
8.5 Metal Electrode Face (Components)	85MELS.WK1
8.6 Small Outline Transistor(SOD) 23	86SOD23.WK1
8.7 Small Outline Transistor (SOD) 89	87SOD89.WK1
8.8 Small Outline Diode (SOD) 123	88SOD123.WK1
8.9 Small Outline Transistors (SOD)143	89SOD143.WK1
8.10 Small Outline Transistors (SOD)	810SO223.WK1

IPC-EM-782 (Users Guide and 3 1/2 Disc) is available from IPC:

$50.00 for IPC members, $100.00 for nonmembers

Spreadsheet Zones

Each spreadsheet has been divided into 10 zones. Each of these zones serves a specific function, and is intended to help the user work through the details of the particular program analysis in which he wishes to accomplish the design of a land pattern. The following is the description and purpose of each of the zones, using the chip resistor file 81 CHPRES. WK1 as the model.

• Zone 1

Zone 1 provides the registered land pattern number in column B, and the component identification in metric in column C. It is always a good idea to fix this zone in place, so that the information is always displayed as the user is moving back and forth along the file. See Figure A-1.

• Zone 2

Zone 2 is intended to describe the finished land pattern dimension. These include the Z maximum dimension; the G minimum dimension; the X maximum dimension; and a reference for the Y dimension, which is derived by subtracting G from Z and dividing by 2. The center point of the two land patterns, and a good placement courtyard area, are intended to encompass the respective components without interference or shorting. The numbers in the table represent the number of grade elements (each element is 0.5 by 0.5 mm) in accordance with the international grid detailed in IEC publication 97. See Figure A-1.

COMPONENT IDENTIFICATION		FINISHED LAND PATTERN DIMENSIONS					
RLP NO	COMP IDENT METRIC	(Max) Z	(Min) G	(Max) X	(Ref) Y	(Ref) C/C	(Ref) PLMT GRID
100	R1005	2.20	0.40	0.80	0.90	1.30	2X6
101	R1608	2.80	0.60	1.20	1.10	1.70	4X6
102	R2012	3.20	0.60	1.40	1.30	1.90	4X8
103	R3216	4.40	1.20	1.60	1.60	2.80	4X10
104	R3225	4.40	1.20	2.60	1.60	2.80	6X10
105	R5025	6.20	2.60	2.60	1.80	4.40	6X14
106	R6332	7.40	3.80	3.20	1.80	5.60	8X16
USER PART		0.00	0.00	0.00	0.00	0.00	
USER PART		0.00	0.00	0.00	0.00	0.00	
USER PART		0.00	0.00	0.00	0.00	0.00	
RLP	MET	Z	G	X	Y	C/C	P/G
DE	DE	DT	DT	DT	DT	DT	DE
B	C	E	F	G	H	I	J
ZONE 1		ZONE 2					

Figure A-1 Zones 1 and 2

• Zone 3

Zone 3 is where the information must be entered for describing the relationship of the component dimensions to be used in the analysis. See Figure A-2.

• Zone 4

Zone 4 represents the manufacturing allowance. This allowance is for the board manufacturing tolerance, and for placement accuracy, and is contained in columns V and W of the spreadsheet for chip resistors. See Figure A-2.

• Zone 5

Zone 5 represents the solder joint design goal information. This information is entered by the user, and reflects the desired solder joint at the toe, heel and side.

The recommendations come from empirical information that has been determined over the years for the derivation of process proven land patterns. See Figure A-2.

COMPONENT DIMENSIONS									MANUFACTURING ALLOWANCE		SOLDER JOINT DESIGN GOAL		
L MIN LGTH	L MAX LGTH	S MIN SPACE	S MAX SPACE	W MIN WIDTH	W MAX WIDTH	T MIN TERM	T MAX TERM	H MAX HEIGHT	F FAB TOL	P PLACE ACRCY	J/T TOE MIN	J/H HEEL MIN	J/S SIDE MIN
1.00	1.10	0.40	0.70	0.48	0.60	0.10	0.30	0.40	0.20	0.20	0.40	0.10	0.00
1.50	1.70	0.70	1.11	0.70	0.95	0.15	0.40	0.60	0.20	0.20	0.40	0.10	0.00
1.85	2.15	0.55	1.32	1.10	1.40	0.15	0.65	0.65	0.20	0.20	0.40	0.10	0.00
3.05	3.35	1.55	2.32	1.45	1.75	0.25	0.75	0.71	0.20	0.20	0.40	0.10	0.00
3.05	3.35	1.55	2.32	2.34	2.64	0.25	0.75	0.71	0.20	0.20	0.40	0.10	0.00
4.85	5.15	3.15	3.92	2.35	2.65	0.35	0.85	0.71	0.20	0.20	0.40	0.10	0.00
6.15	6.45	4.45	5.22	3.05	3.35	0.35	0.85	0.71	0.20	0.20	0.40	0.10	0.00
		0.00	0.00										
		0.00	0.00										
		0.00	0.00										
L/mn	L/mx	S/mn	S/mx	W/mn	W/mx	T/mn	T/mx	H/mx	F/t	P/t	JT/s	JH/s	JS/s
DE	DE	DT	DT	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE
L	M	N	O	P	Q	R	S	T	V	W	Y	Z	AA
ZONE 3									ZONE 4		ZONE 5		

Figure A-2 Zones 3, 4, and 5

• Zone 6

Zone 6 is the most important part of the analysis. It is in this area where the user has the opportunity to fine tune the land pattern through the adjustment factor to enhance the pattern for both solder joint formation and characteristics that can be used by the CAD systems. See Figure A-3.

• Zone 7

Zone 7 provides information as to what has been accomplished for the toe, heel, and side fillets. This zone is divided into three segments. See Figure A-4.

LAND PATTERN CALCULATIONS (PG 1 of 2) &

Z MIN FIN	Z MAX FIN	Z MAX CAL	Z ADJ FACT	G MAX FIN	G MIN FIN	G MIN CAL	G ADJ FACT
2.00	2.20	2.100	0.100	0.60	0.40	0.088	0.312
2.60	2.80	2.646	0.154	0.80	0.60	0.411	0.189
3.00	3.20	3.062	0.138	0.80	0.60	0.300	0.300
4.20	4.40	4.262	0.138	1.40	1.20	1.300	-0.100
4.20	4.40	4.262	0.138	1.40	1.20	1.300	-0.100
6.00	6.20	6.062	0.138	2.80	2.60	2.900	-0.300
7.20	7.40	7.362	0.038	4.00	3.80	4.200	-0.400
0.00	0.00	0.000		0.00	0.00	0.000	
0.00	0.00	0.000		0.00	0.00	0.000	
0.00	0.00	0.000		0.00	0.00	0.000	
Z/mnf	Z/mxf	Z/mxc	Z/aj	G/mxf	G/mnf	G/mnc	G/aj
CI	CT	CI	DE	CI	CT	CI	DE
AC	AD	AE	AF	AH	AI	AJ	AK

ZONE 6, (PART 1 of 2)

LAND PATTERN CALCULATIONS (PG 2 of 2)

X MIN FIN	X MAX FIN	X MAX CAL	X ADJ FACT	Y REF CAL	C/C REF CAL	C/C ADJ FACT
0.60	0.80	0.787	0.013	0.90	1.30	
1.00	1.20	1.077	0.123	1.10	1.70	
1.20	1.40	1.512	-0.112	1.30	1.90	
1.40	1.60	1.862	-0.262	1.60	2.80	
2.40	2.60	2.752	-0.152	1.60	2.80	
2.40	2.60	2.762	-0.162	1.80	4.40	
3.00	3.20	3.462	-0.262	1.80	5.60	
0.00	0.00	0.000		0.00	0.00	
0.00	0.00	0.000		0.00	0.00	
0.00	0.00	0.000		0.00	0.00	
X/mnf	X/mxf	X/mxc	X/aj	Y/c	CC/c	CC/aj
CT	CT	CI	DE	CT	CT	DE
AM	AN	AO	AP	AR	AT	AU

ZONE 6, (PART 2 of 2)

Figure A-3 Zone 6

SOLDER JOINT ANALYSIS

TOE			HEEL			SIDE		
DESIGN GOAL	STATIS MIN	STATIS MAX	DESIGN GOAL	STATIS MIN	STATIS MAX	DESIGN GOAL	STATIS MIN	STATIS MAX
0.40	0.45	0.60	0.10	-0.06	0.15	0.00	0.01	0.16
0.40	0.48	0.65	0.10	0.01	0.25	0.00	0.06	0.25
0.40	0.47	0.68	0.10	-0.05	0.36	0.00	-0.06	0.15
0.40	0.47	0.68	0.10	0.15	0.56	0.00	-0.13	0.08
0.40	0.47	0.68	0.10	0.15	0.56	0.00	-0.08	0.13
0.40	0.47	0.68	0.10	0.25	0.66	0.00	-0.08	0.13
0.40	0.42	0.63	0.10	0.30	0.71	0.00	-0.13	0.08
0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
JT/s	JT/mna	JT/mxa	JH/s	JH/mna	JH/mxa	JS/s	JS/mna	JS/mxa
DT	CI	CI	DT	CI	CI	DT	CI	CI
AW	AX	AY	BA	BB	BC	BE	BF	BG

ZONE 7

Figure A-4 Zone 7

• Zone 8

Zone 8 is the tolerance calculation for toe, heel and side tolerance, and is kept to the side of the spreadsheet because this is where the calculations are accomplished. See Figure A-5.

• Zone 9

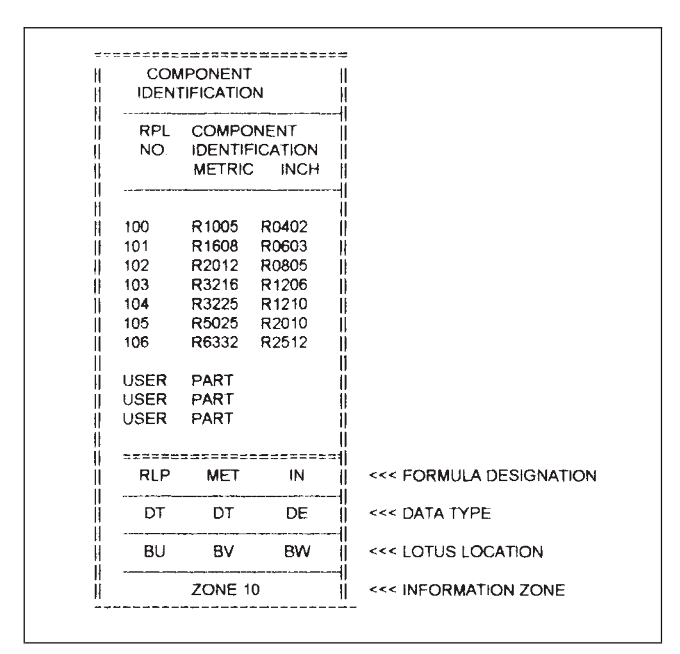
Zone 9 is where all the component dimension calculations are derived. These are mostly calculated information, although columns BR and BS provide calculated information that is transferred to another zone. See Figure A-5.

• Zone 10

Zone 10 again provides information on the component identification. See Figure A-6.

TOLERANCE CALCULATION			COMPONENT DIMENSION CALCULATIONS						
J TOE TOL	J HEEL TOL	J SIDE TOL	L TOL RNG	S TOL RNG	W TOL RNG	T TOL RNG	RMS ACUM TOL	S MIN CAL	S MAX CAL
0.300	0.412	0.307	0.100	0.300	0.120	0.200	0.300	0.400	0.700
0.346	0.495	0.377	0.200	0.406	0.250	0.250	0.406	0.700	1.106
0.412	0.819	0.412	0.300	0.768	0.300	0.500	0.768	0.550	1.318
0.412	0.819	0.412	0.300	0.768	0.300	0.500	0.768	1.550	2.318
0.412	0.819	0.412	0.300	0.768	0.300	0.500	0.768	1.550	2.318
0.412	0.819	0.412	0.300	0.768	0.300	0.500	0.768	3.150	3.918
0.412	0.819	0.412	0.300	0.768	0.300	0.500	0.768	4.450	5.218
0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000
0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000
0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000
JT/t	JH/t	JS/t	W/tr	L/tr	W/tr	T/tr	RMS	S/mn	S/mx
CI	CI	CI	CI	CI	CI	CI	CI	CT	CT
BI	BJ	BK	BM	BN	BO	BP	BQ	BR	BS
ZONE 8			ZONE 9						

Figure A-5 Zones 8 and 9



COMPONENT IDENTIFICATION		
RPL NO	COMPONENT IDENTIFICATION METRIC	INCH
100	R1005	R0402
101	R1608	R0603
102	R2012	R0805
103	R3216	R1206
104	R3225	R1210
105	R5025	R2010
106	R6332	R2512
USER	PART	
USER	PART	
USER	PART	
RLP	MET	IN
DT	DT	DE
BU	BV	BW
ZONE 10		

Figure A-6 Zone 10



Standard Improvement Form

IPC-SM-782A

The purpose of this form is to provide the Technical Committee of IPC with input from the industry regarding usage of the subject standard.

Individuals or companies are invited to submit comments to IPC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

IPC
2215 Sanders Road
Northbrook, IL 60062-6135
Fax 847 509.9798

1. I recommend changes to the following:

___ Requirement, paragraph number __________

___ Test Method number __________, paragraph number __________

The referenced paragraph number has proven to be:

___ Unclear ___ Too Rigid ___ In Error

___ Other ____

2. Recommendations for correction:

____

____

____

____

3. Other suggestions for document improvement:

____

____

____

____

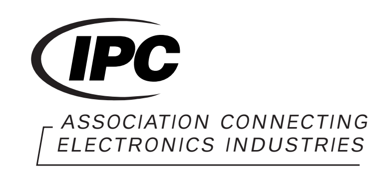
Submitted by:

Name ______________________ Telephone ______________________

Company ______________________ E-mail ______________________

Address ____

City/State/Zip ______________________ Date ______________________



ANSI/IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits Definition Submission/Approval Sheet

The purpose of this form is to keep current with terms routinely used in the industry and their definitions. Individuals or companies are invited to comment. Please complete this form and return to:

IPC
2215 Sanders Road
Northbrook, IL 60062-6135
Fax: 847 509.9798

SUBMITTOR INFORMATION:

Name: ____________________

Company: ____________________

City: ____________________

State/Zip: ____________________

Telephone: ____________________

Date: ____________________

❑ This is a **NEW** term and definition being submitted.
❑ This is an **ADDITION** to an existing term and definition(s).
❑ This is a **CHANGE** to an existing definition.

Term	Definition

If space not adequate, use reverse side or attach additional sheet(s).

Artwork: ❑ Not Applicable ❑ Required ❑ To be supplied
❑ Included: Electronic File Name: ____________________

Document(s) to which this term applies: ____________________

Committees affected by this term: ____________________

Office Use

IPC Office

Date Received: ____________________
Comments Collated: ____________________
Returned for Action: ____________________
Revision Inclusion: ____________________

Committee 2-30

Date of Initial Review: ____________________
Comment Resolution: ____________________
Committee Action: ❑ Accepted ❑ Rejected
❑ Accept Modify

IEC Classification

Classification Code • Serial Number

Terms and Definition Committee Final Approval Authorization:
Committee 2-30 has approved the above term for release in the next revision.

Name: ____________________ Committee: IPC 2-30 Date: ____________________

Revision History for IPC-SM-782 Standard

The following is a listing of major alterations and additions to the IPC-SM-782 Standard since its initial publication in March 1987. The standard went through a comprehensive revision in August 1993, followed by an amendment in October 1996.

Changes addressed within Revision A:

- Complete revision of document to establish independent sections (8.0 - 13.0) representing requirements for families of surface-mountable components. Each section, in turn, was broken down into four subsections highlighting component description, component dimensions, land pattern dimensions, and finally, tolerance analysis.
- Listing of all registered land pattern numbers for component types in both existing and future sections.
- Inclusion of a dedicated section (3.3) establishing dimensional criteria for components, land patterns, and positional accuracy of component placement capabilities. Also contains examples of typical package styles and their respective double letter designators.
- Inclusion of a dedicated section (3.5) highlighting environmental constraints. Addresses worst-case use environments for surface mount electronic assemblies in nine major use categories. Includes discussion of both design service life and acceptable cumulative failure probability for each of these categories.

Changes addressed within Amendment 1:

- Alteration of formulas within Section 3.3.1 on Component Tolerancing.
- Corrections to technical and typographical errors throughout Section 3.6 on Component Spacing.
- Corrections to technical and typographical errors throughout Section 3.7 on Outer Layer Finishes.
- Replacement of 15 figures throughout the first seven sections, as well as a subsequent replacement of 39 tables in Sections 8 through 13 that address corrections to component and land pattern dimensions for various component families.

Changes addressed within Amendment 2:

- Inclusion of Section 14.0 addressing land patterns for components with ball grid array contacts.



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